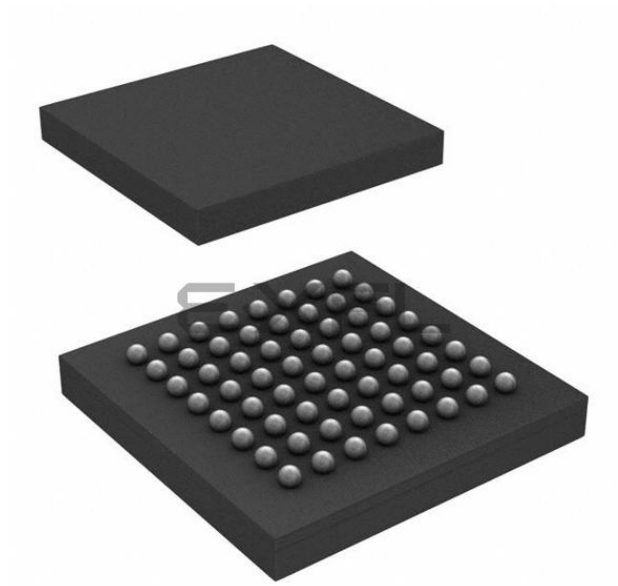

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 19x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-UFBGA |
| Supplier Device Package | 64-UFBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072rbh6 |

# 2 Description

The STM32F072x8/xB microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (two $I^2C$s, two SPI/$I^2S$, one HDMI CEC and four USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F072x8/xB microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F072x8/xB microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F072x8/xB microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

**Figure 1. Block diagram**

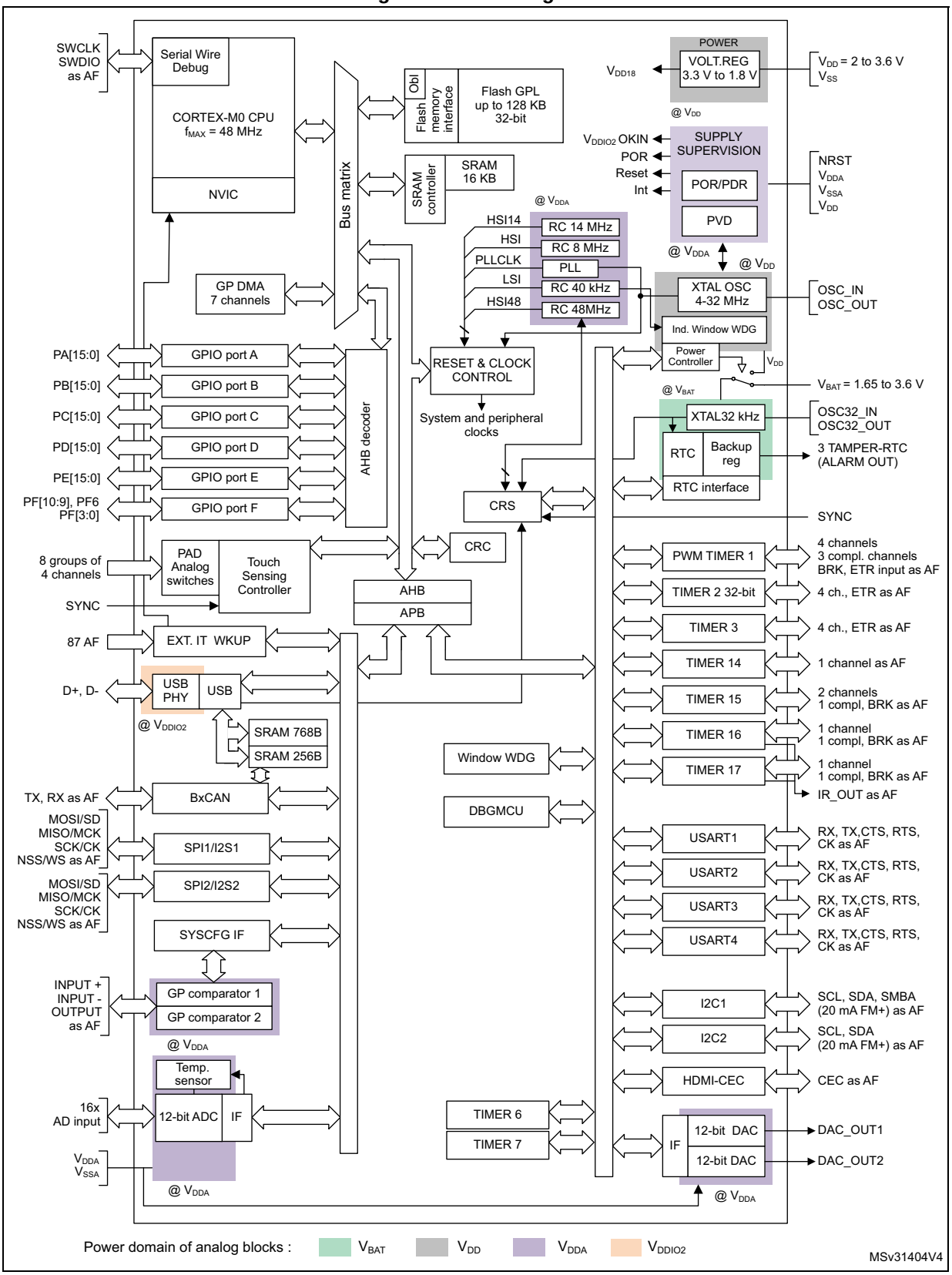


**Table 6. Number of capacitive sensing channels available on STM32F072x8/xB devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F072Vx | STM32F072Rx | STM32F072Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

*Table 7* compares the features of the different timers.

**Table 7. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16 TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6 TIM7 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| D11 | 67 | D7 | 41 | 29 | D1 | PA8 | I/O | FT | (3) | USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC | - |
| D10 | 68 | C7 | 42 | 30 | D2 | PA9 | I/O | FT | (3) | USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1 | - |
| C12 | 69 | C6 | 43 | 31 | C2 | PA10 | I/O | FT | (3) | USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2 | - |
| B12 | 70 | C8 | 44 | 32 | C1 | PA11 | I/O | FT | (3) | CAN_RX, USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT | USB_DM |
| A12 | 71 | B8 | 45 | 33 | C3 | PA12 | I/O | FT | (3) | CAN_TX, USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT | USB_DP |
| A11 | 72 | A8 | 46 | 34 | B3 | PA13 | I/O | FT | (3) (4) | IR_OUT, SWDIO, USB_NOE | - |
| C11 | 73 | - | - | - | - | PF6 | I/O | FT | (3) | - | - |
| F11 | 74 | D6 | 47 | 35 | B1 | VSS | S | - | - | Ground | |
| G11 | 75 | E6 | 48 | 36 | B2 | VDDIO2 | S | - | - | Digital power supply | |
| A10 | 76 | A7 | 49 | 37 | A1 | PA14 | I/O | FT | (3) (4) | USART2_TX, SWCLK | - |
| A9 | 77 | A6 | 50 | 38 | A2 | PA15 | I/O | FT | (3) | SPI1_NSS, I2S1_WS, USART2_RX, USART4_RTS, TIM2_CH1_ETR, EVENTOUT | - |
| B11 | 78 | B7 | 51 | - | - | PC10 | I/O | FT | (3) | USART3_TX, USART4_TX | - |

Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| C10 | 79 | B6 | 52 | - | - | PC11 | I/O | FT | (3) | USART3_RX, USART4_RX | - |
| B10 | 80 | C5 | 53 | - | - | PC12 | I/O | FT | (3) | USART3_CK, USART4_CK | - |
| C9 | 81 | - | - | - | - | PD0 | I/O | FT | (3) | SPI2_NSS, I2S2_WS, CAN_RX | - |
| B9 | 82 | - | - | - | - | PD1 | I/O | FT | (3) | SPI2_SCK, I2S2_CK, CAN_TX | - |
| C8 | 83 | B5 | 54 | - | - | PD2 | I/O | FT | (3) | USART3_RTS, TIM3_ETR | - |
| B8 | 84 | - | - | - | - | PD3 | I/O | FT | - | SPI2_MISO, I2S2_MCK, USART2_CTS | - |
| B7 | 85 | - | - | - | - | PD4 | I/O | FT | - | SPI2_MOSI, I2S2_SD, USART2_RTS | - |
| A6 | 86 | - | - | - | - | PD5 | I/O | FT | - | USART2_TX | - |
| B6 | 87 | - | - | - | - | PD6 | I/O | FT | - | USART2_RX | - |
| A5 | 88 | - | - | - | - | PD7 | I/O | FT | - | USART2_CK | - |
| A8 | 89 | A5 | 55 | 39 | A3 | PB3 | I/O | FT | - | SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT | - |
| A7 | 90 | A4 | 56 | 40 | A4 | PB4 | I/O | FT | - | SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT | - |
| C5 | 91 | C4 | 57 | 41 | B4 | PB5 | I/O | FT | - | SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2 | WKUP6 |
| B5 | 92 | D3 | 58 | 42 | C4 | PB6 | I/O | FTf | - | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03 | - |

**Table 18. Alternate functions selected through GPIOE_AFR registers for port E**

| Pin name | AF0 | AF1 |
|---|---|---|
| PE0 | TIM16_CH1 | EVENTOUT |
| PE1 | TIM17_CH1 | EVENTOUT |
| PE2 | TIM3_ETR | TSC_G7_IO1 |
| PE3 | TIM3_CH1 | TSC_G7_IO2 |
| PE4 | TIM3_CH2 | TSC_G7_IO3 |
| PE5 | TIM3_CH3 | TSC_G7_IO4 |
| PE6 | TIM3_CH4 | - |
| PE7 | TIM1_ETR | - |
| PE8 | TIM1_CH1N | - |
| PE9 | TIM1_CH1 | - |
| PE10 | TIM1_CH2N | - |
| PE11 | TIM1_CH2 | - |
| PE12 | TIM1_CH3N | SPI1_NSS, I2S1_WS |
| PE13 | TIM1_CH3 | SPI1_SCK, I2S1_CK |
| PE14 | TIM1_CH4 | SPI1_MISO, I2S1_MCK |
| PE15 | TIM1_BKIN | SPI1_MOSI, I2S1_SD |

**Table 19. Alternate functions available on port F**

| Pin name | AF |
|---|---|
| PF0 | CRS_SYNC |
| PF1 | - |
| PF2 | EVENTOUT |
| PF3 | EVENTOUT |
| PF6 | - |
| PF9 | TIM15_CH1 |
| PF10 | TIM15_CH2 |

**Table 20. STM32F072x8/xB peripheral register boundary addresses**

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| | 0x4800 1800 - 0x5FFF FFFF | ~384 MB | Reserved |
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1 KB | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1 KB | GPIOE |
| | 0x4800 0C00 - 0x4800 0FFF | 1 KB | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1 KB | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1 KB | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1 KB | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 MB | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 KB | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 KB | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 KB | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 KB | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 KB | Flash memory interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 KB | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 KB | RCC |
| | 0x4002 0400 - 0x4002 0FFF | 3 KB | Reserved |
| | 0x4002 0000 - 0x4002 03FF | 1 KB | DMA |
| | 0x4001 8000 - 0x4001 FFFF | 32 KB | Reserved |
| APB | 0x4001 5C00 - 0x4001 7FFF | 9 KB | Reserved |
| | 0x4001 5800 - 0x4001 5BFF | 1 KB | DBGMCU |
| | 0x4001 4C00 - 0x4001 57FF | 3 KB | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 KB | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 KB | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 KB | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 KB | Reserved |
| | 0x4001 3800 - 0x4001 3BFF | 1 KB | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 KB | Reserved |
| | 0x4001 3000 - 0x4001 33FF | 1 KB | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | 1 KB | TIM1 |
| | 0x4001 2800 - 0x4001 2BFF | 1 KB | Reserved |
| | 0x4001 2400 - 0x4001 27FF | 1 KB | ADC |
| | 0x4001 0800 - 0x4001 23FF | 7 KB | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 KB | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 KB | SYSCFG + COMP |
| | 0x4000 8000 - 0x4000 FFFF | 32 KB | Reserved |

## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics* and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 21. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage | - 0.3 | 4.0 | V |
| $V_{DDIO2}$–$V_{SS}$ | External I/O supply voltage | - 0.3 | 4.0 | V |
| $V_{DDA}$–$V_{SS}$ | External analog supply voltage | - 0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.4 | V |
| $V_{BAT}$–$V_{SS}$ | External backup supply voltage | - 0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on FT and FTf pins | $V_{SS}$ - 0.3 | $V_{DDIOx}$ + 4.0(3) | V |
| | Input voltage on TTa pins | $V_{SS}$ - 0.3 | 4.0 | V |
| | BOOT0 | 0 | 9.0 | V |
| | Input voltage on any other pin | $V_{SS}$ - 0.3 | 4.0 | V |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSx} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | mV |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.12: Electrical sensitivity characteristics* | | - |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.

**Table 25. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | - | 0 | ∞ | |
| | $V_{DDA}$ fall time rate | | 20 | ∞ | |

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

**Table 26. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR/PDR}$(1) | Power on/power down reset threshold | Falling edge(2) | 1.80 | 1.88 | 1.96(3) | V |
| | | Rising edge | 1.84(3) | 1.92 | 2.00 | V |
| $V_{PDRhyst}$ | PDR hysteresis | - | - | 40 | - | mV |
| $t_{RSTTEMPO}$(4) | Reset temporization | - | 1.50 | 2.50 | 4.50 | ms |

1. The PDR detector monitors $V_{DD}$ and also $V_{DDA}$ (if kept enabled in the option bytes). The POR detector monitors only $V_{DD}$.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

**Table 27. Programmable voltage detector characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD0}$ | PVD threshold 0 | Rising edge | 2.1 | 2.18 | 2.26 | V |
| | | Falling edge | 2 | 2.08 | 2.16 | V |
| $V_{PVD1}$ | PVD threshold 1 | Rising edge | 2.19 | 2.28 | 2.37 | V |
| | | Falling edge | 2.09 | 2.18 | 2.27 | V |
| $V_{PVD2}$ | PVD threshold 2 | Rising edge | 2.28 | 2.38 | 2.48 | V |
| | | Falling edge | 2.18 | 2.28 | 2.38 | V |
| $V_{PVD3}$ | PVD threshold 3 | Rising edge | 2.38 | 2.48 | 2.58 | V |
| | | Falling edge | 2.28 | 2.38 | 2.48 | V |

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 35*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 21: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 35*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

**Table 35. Peripheral current consumption**

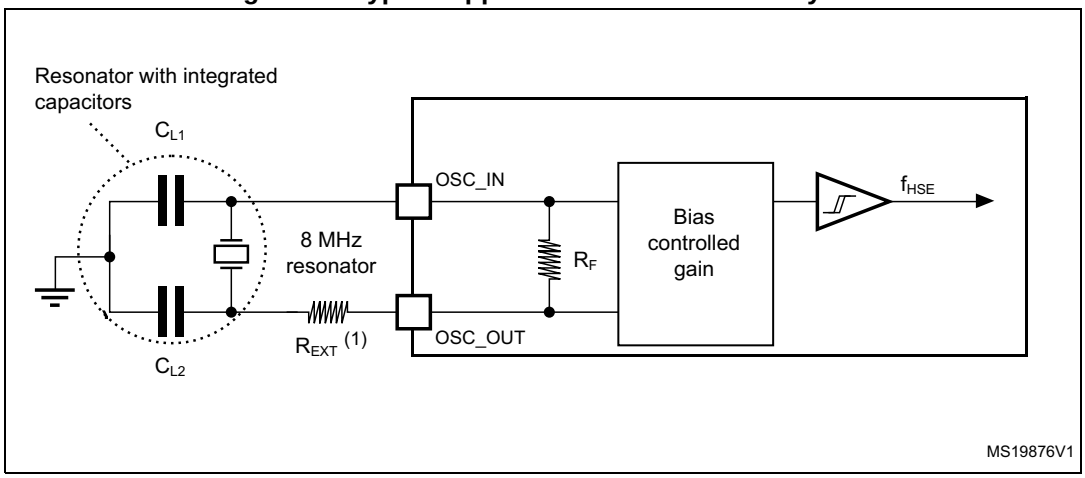
| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB | BusMatrix(1) | 2.2 | µA/MHz |
| | CRC | 1.6 | |
| | DMA | 5.7 | |
| | Flash memory interface | 13.0 | |
| | GPIOA | 8.2 | |
| | GPIOB | 8.5 | |
| | GPIOC | 2.3 | |
| | GPIOD | 1.9 | |
| | GPIOE | 2.2 | |
| | GPIOF | 1.2 | |
| | SRAM | 0.9 | |
| | TSC | 5.0 | |
| | **All AHB peripherals** | **52.6** | |

**Table 35. Peripheral current consumption (continued)**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB | APB-Bridge(2) | 2.8 | µA/MHz |
| | ADC(3) | 4.1 | |
| | CAN | 12.4 | |
| | CEC | 1.5 | |
| | CRS | 0.8 | |
| | DAC(3) | 4.7 | |
| | DEBUG (MCU debug feature) | 0.1 | |
| | I2C1 | 3.9 | |
| | I2C2 | 4.0 | |
| | PWR | 1.3 | |
| | SPI1 | 8.7 | |
| | SPI2 | 8.5 | |
| | SYSCFG & COMP | 1.7 | |
| | TIM1 | 14.9 | |
| | TIM2 | 15.5 | |
| | TIM3 | 11.4 | |
| | TIM6 | 2.5 | |
| | TIM7 | 2.3 | |
| | TIM14 | 5.3 | |
| | TIM15 | 9.1 | |
| | TIM16 | 6.6 | |
| | TIM17 | 6.8 | |
| | USART1 | 17.0 | |
| | USART2 | 16.7 | |
| | USART3 | 5.4 | |
| | USART4 | 5.4 | |
| | USB | 7.2 | |
| | WWDG | 1.4 | |
| | **All APB peripherals** | **182** | |

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part ($I_{DDA}$) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

**Figure 17. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

## Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | low drive capability | - | 0.5 | 0.9 | µA |
| | | medium-low drive capability | - | - | 1 | |
| | | medium-high drive capability | - | - | 1.3 | |
| | | high drive capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | low drive capability | 5 | - | - | µA/V |
| | | medium-low drive capability | 8 | - | - | |
| | | medium-high drive capability | 15 | - | - | |
| | | high drive capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DDIOx}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

**Software recommendations**

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 49. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/48 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -2 | dBµV |
| | | | 30 to 130 MHz | 27 | |
| | | | 130 MHz to 1 GHz | 17 | |
| | | | EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 57. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{TRIG}$ (2) | External trigger frequency | $f_{ADC}$ = 14 MHz, 12-bit resolution | - | - | 823 | kHz |
| | | 12-bit resolution | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | - | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$ (2) | External input impedance | See *Equation 1* and *Table 58* for details | - | - | 50 | kΩ |
| $R_{ADC}$ (2) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$ (2) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$ (2)(3) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $W_{LATENCY}$ (2)(4) | ADC_DR register ready latency | ADC clock = HSI14 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$ (2) | Trigger conversion latency | $f_{ADC} = f_{PCLK}/2 = 14$ MHz | 0.196 | | | µs |
| | | $f_{ADC} = f_{PCLK}/2$ | 5.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{PCLK}/4 = 12$ MHz | 0.219 | | | µs |
| | | $f_{ADC} = f_{PCLK}/4$ | 10.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{HSI14}$ = 14 MHz | 0.179 | - | 0.250 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC} = f_{HSI14}$ | - | 1 | - | $1/f_{HSI14}$ |
| $t_S$ (2) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$ (2) | Stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{CONV}$ (2) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz, 12-bit resolution | 1 | - | 18 | µs |
| | | 12-bit resolution | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on $I_{DDA}$ and 60 µA on $I_{DD}$ should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

### 6.3.19 Temperature sensor characteristics

**Table 62. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$ (1) | $V_{SENSE}$ linearity with temperature | - | ± 1 | ± 2 | °C |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{30}$ | Voltage at 30 °C (± 5 °C)(2) | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$ (1) | ADC_IN16 buffer startup time | - | - | 10 | µs |
| $t_{S\_temp}$ (1) | ADC sampling time when reading the temperature | 4 | - | - | µs |

1. Guaranteed by design, not tested in production.
2. Measured at $V_{DDA}$ = 3.3 V ± 10 mV. The $V_{30}$ ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 3: Temperature sensor calibration values*.

### 6.3.20 $V_{BAT}$ monitoring characteristics

**Table 63. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 2 x 50 | - | kΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 2 | - | - |
| Er(1) | Error on Q | –1 | - | +1 | % |
| $t_{S\_vbat}$ (1) | ADC sampling time when reading the $V_{BAT}$ | 4 | - | - | µs |

1. Guaranteed by design, not tested in production.

### 6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 64. TIMx characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48 MHz | - | 20.8 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | - | $f_{TIMxCLK}/2$ | - | MHz |
| | | $f_{TIMxCLK}$ = 48 MHz | - | 24 | - | MHz |
| $t_{MAX\_COUNT}$ | 16-bit timer maximum period | - | - | $2^{16}$ | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48 MHz | - | 1365 | - | µs |
| | 32-bit counter maximum period | - | - | $2^{32}$ | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48 MHz | - | 89.48 | - | s |

Table 71. UFBGA100 package mechanical data (continued)

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| b | 0.240 | 0.290 | 0.340 | 0.0094 | 0.0114 | 0.0134 |
| D | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| D1 | - | 5.500 | - | - | 0.2165 | - |
| E | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| E1 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| Z | - | 0.750 | - | - | 0.0295 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. Recommended footprint for UFBGA100 package

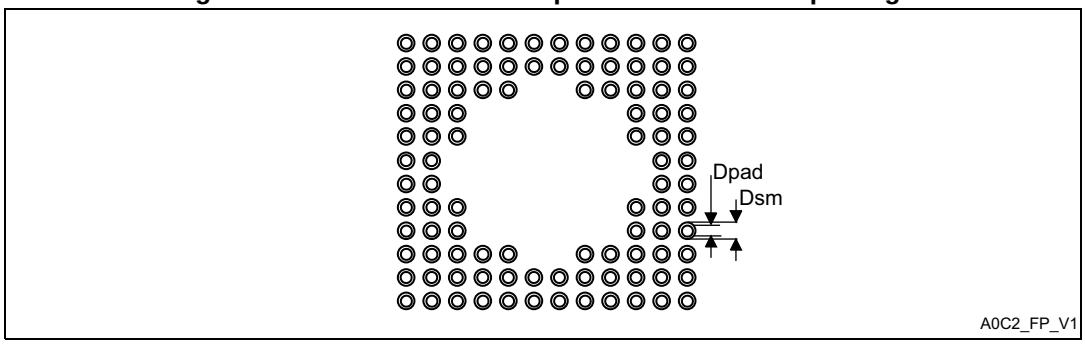



Table 72. UFBGA100 recommended PCB design rules

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the solder mask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |

Table 74. UFBGA64 package mechanical data (continued)

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. Recommended footprint for UFBGA64 package

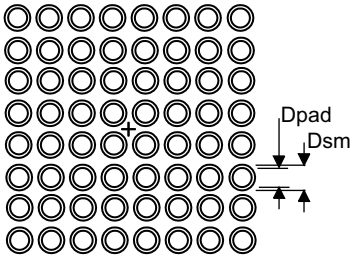



Table 75. UFBGA64 recommended PCB design rules

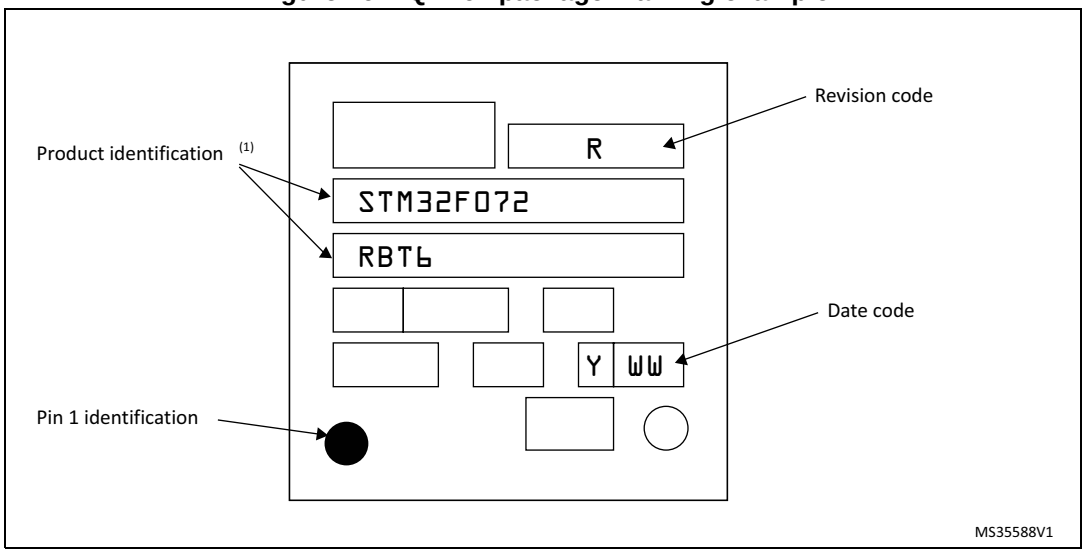
| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 46. LQFP64 package marking example**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 77. WLCSP49 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 3.242 | 3.277 | 3.312 | 0.1276 | 0.1290 | 0.1304 |
| E | 3.074 | 3.109 | 3.144 | 0.1210 | 0.1224 | 0.1238 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 2.400 | - | - | 0.0945 | - |
| e2 | - | 2.400 | - | - | 0.0945 | - |
| F | - | 0.4385 | - | - | 0.0173 | - |
| G | - | 0.3545 | - | - | 0.0140 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

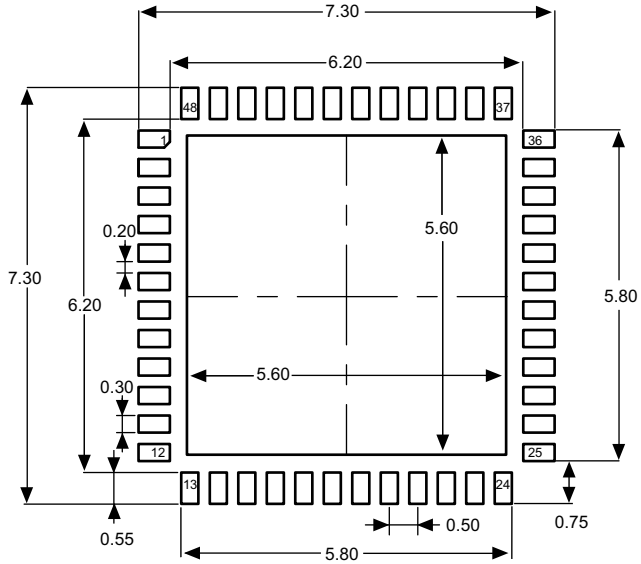
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Table 79. UFQFPN48 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 53. Recommended footprint for UFQFPN48 package**




1. Dimensions are expressed in millimeters.