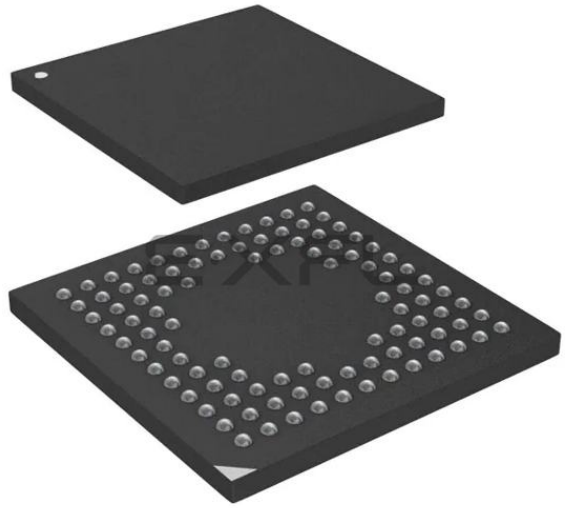


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 87 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072v8h6 |

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F072x8/xB microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

### 3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 87 GPIOs can be connected to the 16 external interrupt lines.

## 3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

### 3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 3. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA}$= 3.3 V (± 10 mV) | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA}$= 3.3 V (± 10 mV) | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 3.10.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. The

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

## 3.13 Touch sensing controller (TSC)

The STM32F072x8/xB devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

**Table 5. Capacitive sensing GPIOs available on STM32F072x8/xB devices**

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|---|---|---|---|---|---|
| 1 | TSC_G1_IO1 | PA0 | 5 | TSC_G5_IO1 | PB3 |
| | TSC_G1_IO2 | PA1 | | TSC_G5_IO2 | PB4 |
| | TSC_G1_IO3 | PA2 | | TSC_G5_IO3 | PB6 |
| | TSC_G1_IO4 | PA3 | | TSC_G5_IO4 | PB7 |
| 2 | TSC_G2_IO1 | PA4 | 6 | TSC_G6_IO1 | PB11 |
| | TSC_G2_IO2 | PA5 | | TSC_G6_IO2 | PB12 |
| | TSC_G2_IO3 | PA6 | | TSC_G6_IO3 | PB13 |
| | TSC_G2_IO4 | PA7 | | TSC_G6_IO4 | PB14 |
| 3 | TSC_G3_IO1 | PC5 | 7 | TSC_G7_IO1 | PE2 |
| | TSC_G3_IO2 | PB0 | | TSC_G7_IO2 | PE3 |
| | TSC_G3_IO3 | PB1 | | TSC_G7_IO3 | PE4 |
| | TSC_G3_IO4 | PB2 | | TSC_G7_IO4 | PE5 |
| 4 | TSC_G4_IO1 | PA9 | 8 | TSC_G8_IO1 | PD12 |
| | TSC_G4_IO2 | PA10 | | TSC_G8_IO2 | PD13 |
| | TSC_G4_IO3 | PA11 | | TSC_G8_IO3 | PD14 |
| | TSC_G4_IO4 | PA12 | | TSC_G8_IO4 | PD15 |

**Table 6. Number of capacitive sensing channels available on STM32F072x8/xB devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F072Vx | STM32F072Rx | STM32F072Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.14 Timers and watchdogs

The STM32F072x8/xB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

*Table 7* compares the features of the different timers.

**Table 7. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|---|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM3 | 16-bit | Up, down, up/down | integer from 1 to 65536 | Yes | 4 | - |
| | TIM14 | 16-bit | Up | integer from 1 to 65536 | No | 1 | - |
| | TIM15 | 16-bit | Up | integer from 1 to 65536 | Yes | 2 | 1 |
| | TIM16 TIM17 | 16-bit | Up | integer from 1 to 65536 | Yes | 1 | 1 |
| Basic | TIM6 TIM7 | 16-bit | Up | integer from 1 to 65536 | Yes | - | - |

overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

## 3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

## 3.21 Universal serial bus (USB)

The STM32F072x8/xB embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 byte are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

## 3.22 Clock recovery system (CRS)

The STM32F072x8/xB embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

## 3.23 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

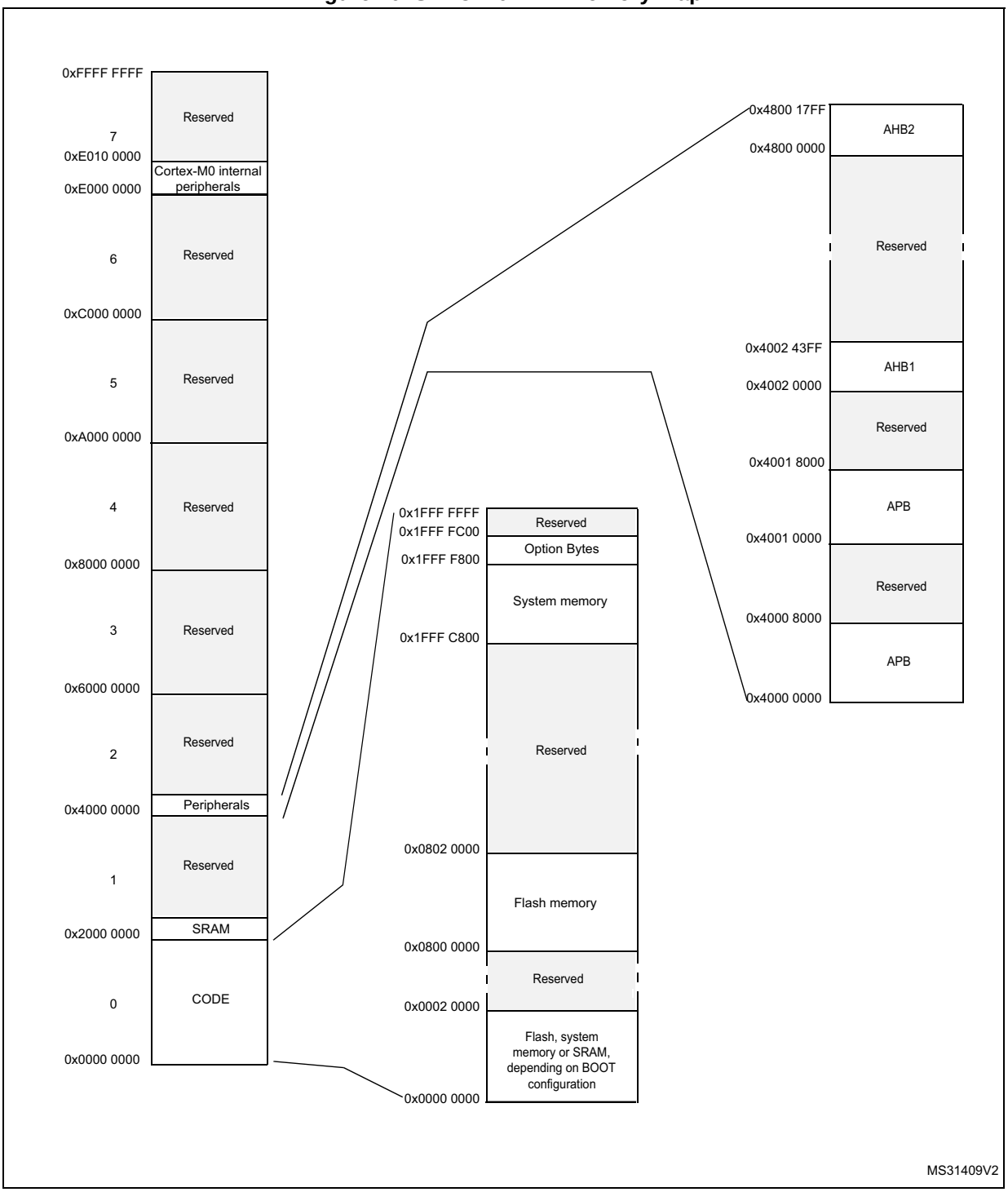
Table 13. STM32F072x8/xB pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | LQFP48/UFQFPN48 | WLCSP49 | | | | | Alternate functions | Additional functions |
| M2 | 24 | H2 | 15 | 11 | G7 | PA1 | I/O | TTa | - | USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT | ADC_IN1, COMP1_INP |
| K3 | 25 | F3 | 16 | 12 | E5 | PA2 | I/O | TTa | - | USART2_TX, COMP2_OUT, TIM2_CH3, TIM15_CH1, TSC_G1_IO3 | ADC_IN2, COMP2_INM6, WKUP4 |
| L3 | 26 | G3 | 17 | 13 | E4 | PA3 | I/O | TTa | - | USART2_RX,TIM2_CH4, TIM15_CH2, TSC_G1_IO4 | ADC_IN3, COMP2_INP |
| D3 | 27 | C2 | 18 | - | - | VSS | S | - | - | Ground | |
| H3 | 28 | D2 | 19 | - | - | VDD | S | - | - | Digital power supply | |
| M3 | 29 | H3 | 20 | 14 | G6 | PA4 | I/O | TTa | - | SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK | COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1 |
| K4 | 30 | F4 | 21 | 15 | F5 | PA5 | I/O | TTa | - | SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2 | COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2 |
| L4 | 31 | G4 | 22 | 16 | F4 | PA6 | I/O | TTa | - | SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS | ADC_IN6 |
| M4 | 32 | H4 | 23 | 17 | F3 | PA7 | I/O | TTa | - | SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT | ADC_IN7 |

# 5 Memory mapping

To the difference of STM32F072xB memory map in *Figure 10*, the two bottom code memory spaces of STM32F072x8 end at 0x0000 FFFF and 0x0800 FFFF, respectively.

**Figure 10. STM32F072xB memory map**



All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 29* to *Table 31* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

**Table 29. Typical and maximum current consumption from $V_{DD}$ supply at $V_{DD}$ = 3.6 V**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | All peripherals enabled(1) | | | | All peripherals disabled | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$(2) | | | Typ | Max @ $T_A$(2) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$ | Supply current in Run mode, code executing from Flash memory | HSI48 | 48 MHz | 24.3 | 26.9 | 27.2 | 27.9 | 13.1 | 14.8 | 14.9 | 15.5 | mA |
| | | HSE bypass, PLL on | 48 MHz | 24.1 | 26.8 | 27.0 | 27.7 | 13.0 | 14.6 | 14.8 | 15.4 | |
| | | | 32 MHz | 16.0 | 18.3 | 18.6 | 19.2 | 8.76 | 9.56 | 9.73 | 10.6 | |
| | | | 24 MHz | 12.3 | 13.7 | 14.3 | 14.7 | 7.36 | 7.94 | 8.37 | 8.81 | |
| | | HSE bypass, PLL off | 8 MHz | 4.52 | 5.25 | 5.28 | 5.61 | 2.89 | 3.17 | 3.26 | 3.34 | |
| | | | 1 MHz | 1.25 | 1.39 | 1.58 | 1.87 | 0.93 | 1.06 | 1.15 | 1.34 | |
| | | HSI clock, PLL on | 48 MHz | 24.1 | 27.1 | 27.6 | 27.8 | 12.9 | 14.7 | 14.9 | 15.5 | |
| | | | 32 MHz | 16.1 | 18.2 | 18.9 | 19.3 | 8.82 | 9.69 | 9.83 | 10.7 | |
| | | | 24 MHz | 12.4 | 14.0 | 14.4 | 14.8 | 7.31 | 7.92 | 8.34 | 8.75 | |
| | | HSI clock, PLL off | 8 MHz | 4.52 | 5.25 | 5.35 | 5.61 | 2.87 | 3.16 | 3.25 | 3.33 | |

**Table 47. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Min(1) | Unit |
|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = –40 to +105 °C | 10 | kcycle |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Year |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 10 kcycle(2) at $T_A$ = 55 °C | 20 | |

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

## 6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 48. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25°C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-4 | 4B |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Table 53. I/O static characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current(2) | TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$ | - | - | ± 0.1 | µA |
| | | TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$ | - | - | 1 | |
| | | TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$ | - | - | ± 0.2 | |
| | | FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V | - | - | 10 | |
| $R_{PU}$ | Weak pull-up equivalent resistor (3) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(3) | $V_{IN} = - V_{DDIOx}$ | 25 | 40 | 55 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 52: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

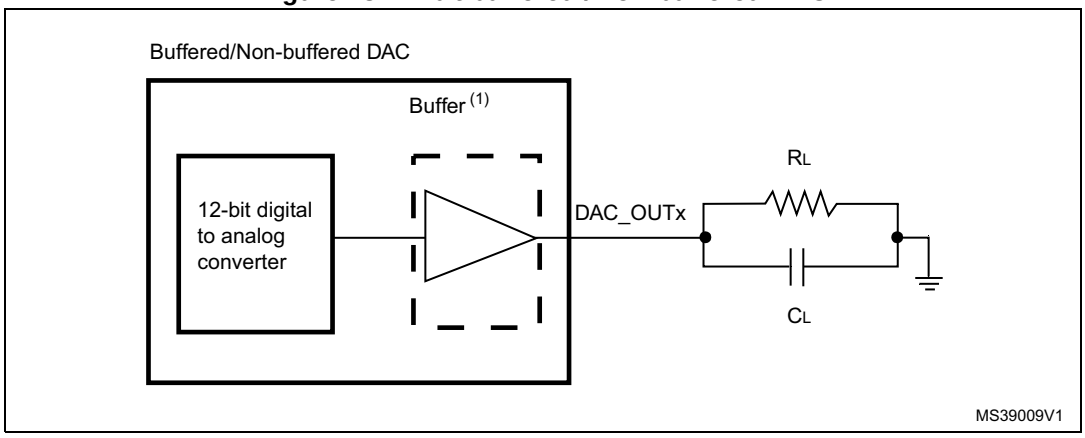
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

**Table 60. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Gain error(3) | Gain error | - | - | ±0.5 | % | Given for the DAC in 12-bit configuration |
| $t_{SETTLING}$(3) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | - | 3 | 4 | µs | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ |
| Update rate(3) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ |
| $t_{WAKEUP}$(3) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD}$ ≤ 50 pF, $R_{LOAD}$ ≥ 5 kΩ input code between lowest and highest possible ones. |
| PSRR+ (1) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

**Figure 28. 12-bit buffered / non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

### USB characteristics

The STM32F072x8/xB USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

**Table 70. USB electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDIO2}$ | USB transceiver operating voltage | - | 3.0(1) | - | 3.6 | V |
| $t_{STARTUP}$(2) | USB transceiver startup time | - | - | - | 1.0 | µs |
| $R_{PUI}$ | Embedded USB_DP pull-up value during idle | - | 1.1 | 1.26 | 1.5 | kΩ |
| $R_{PUR}$ | Embedded USB_DP pull-up value during reception | - | 2.0 | 2.26 | 2.6 | |
| $Z_{DRV}$(2) | Output driver impedance(3) | Driving high and low | 28 | 40 | 44 | Ω |

1. The STM32F072x8/xB USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design, not tested in production.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

### CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

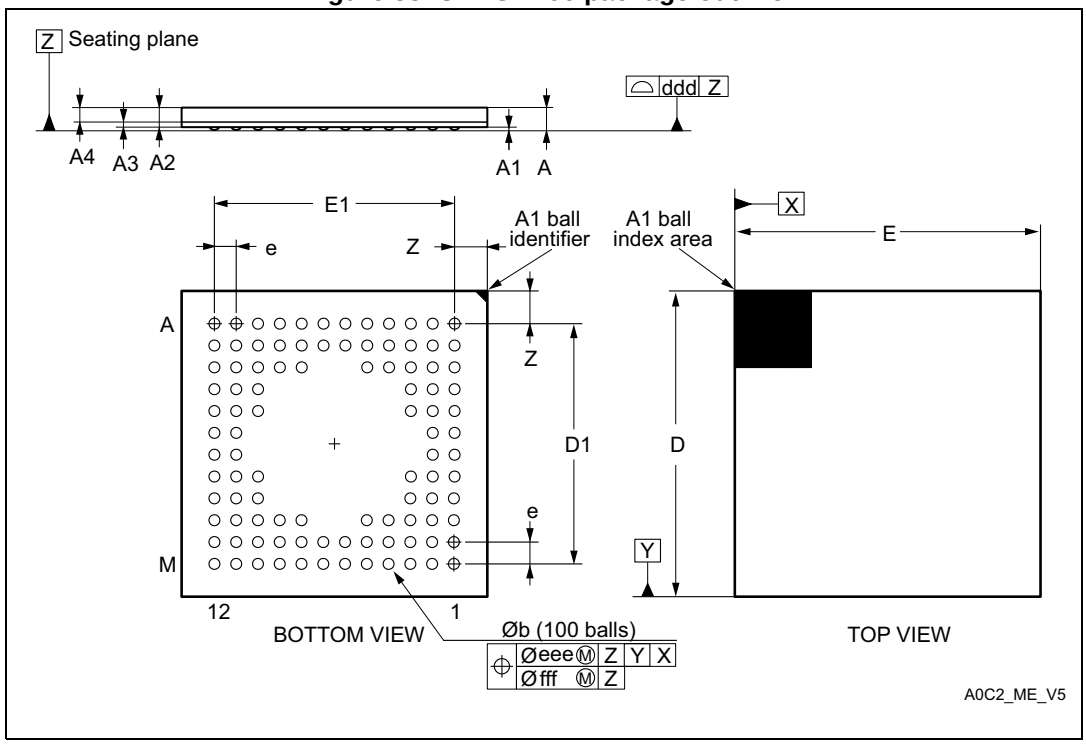
# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 UFBGA100 package information

**UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra-fine-profile ball grid array package.**

**Figure 35. UFBGA100 package outline**




1. Drawing is not to scale.

**Table 71. UFBGA100 package mechanical data**

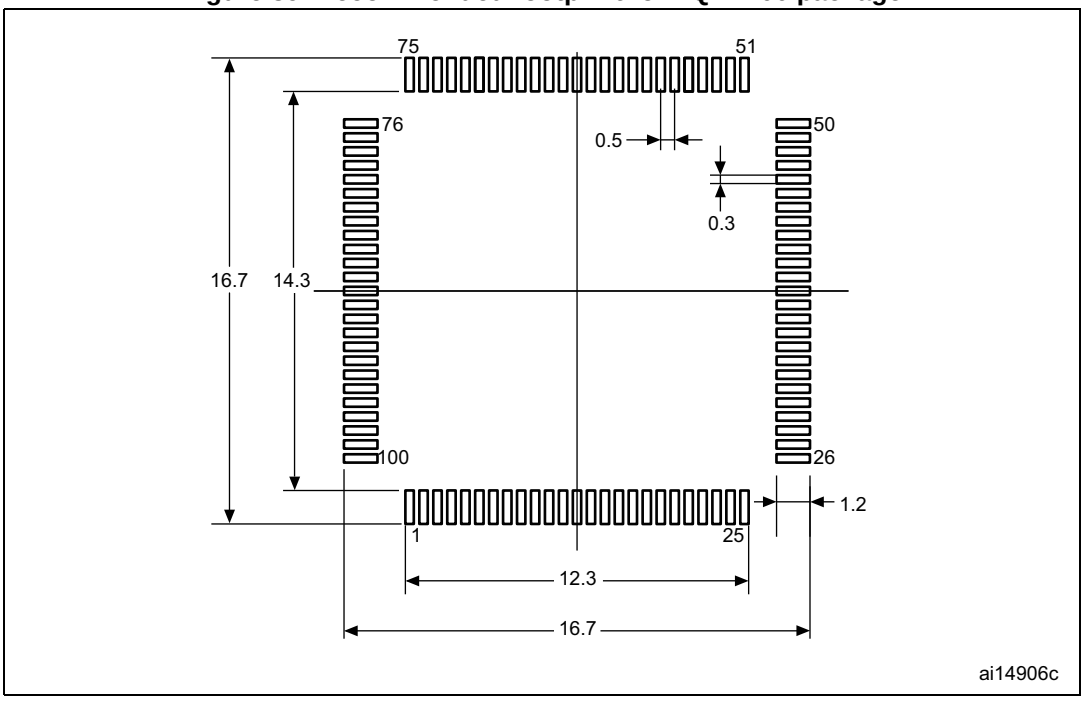
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 0.600 | - | - | 0.0236 |
| A1 | - | - | 0.110 | - | - | 0.0043 |
| A2 | - | 0.450 | - | - | 0.0177 | - |
| A3 | - | 0.130 | - | - | 0.0051 | 0.0094 |
| A4 | - | 0.320 | - | - | 0.0126 | - |

**Table 73. LQPF100 package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. Recommended footprint for LQFP100 package**



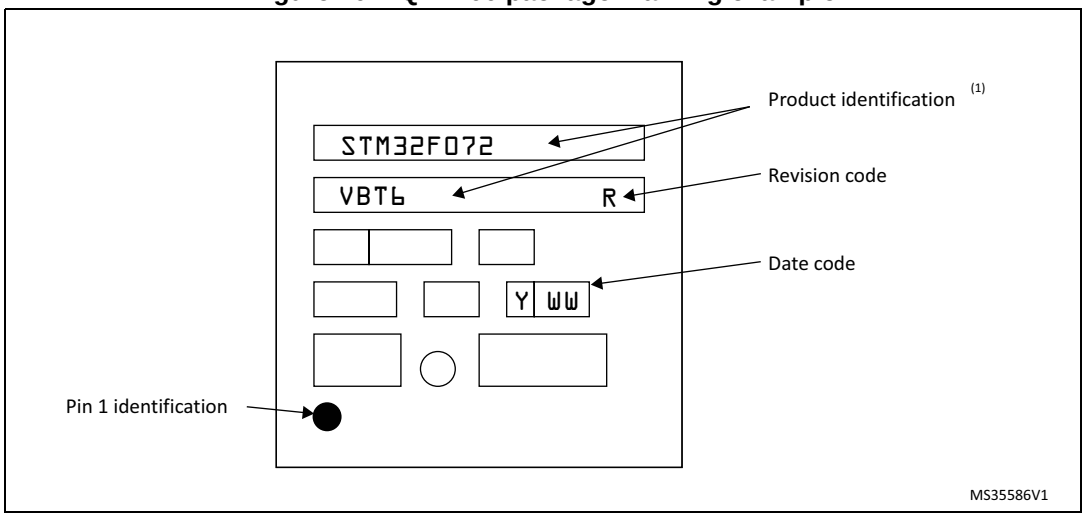

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 40. LQFP100 package marking example**



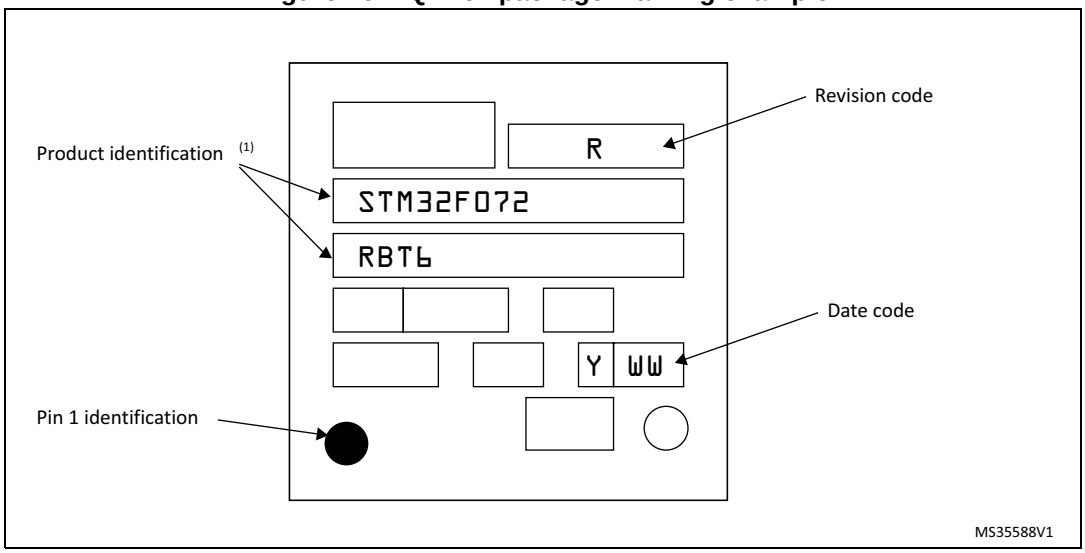

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 46. LQFP64 package marking example**

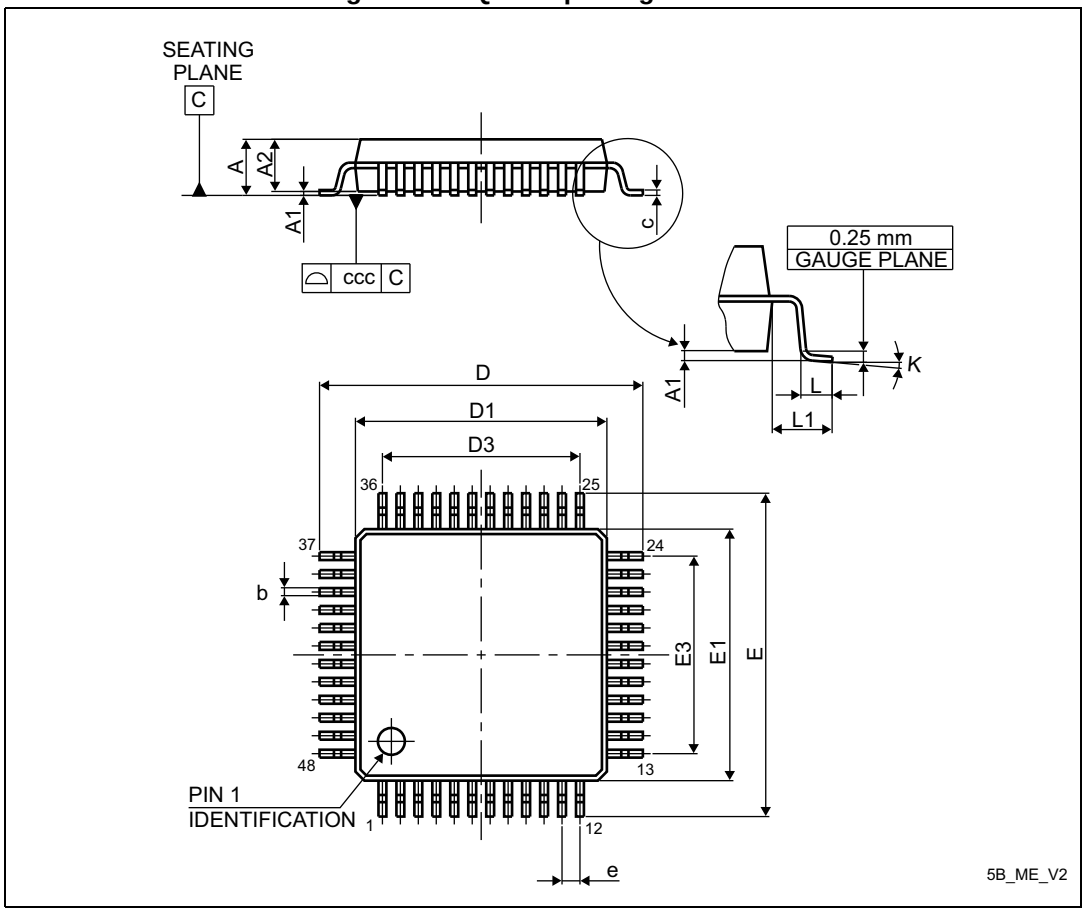



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.6 LQFP48 package information

**LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.**

**Figure 49. LQFP48 package outline**



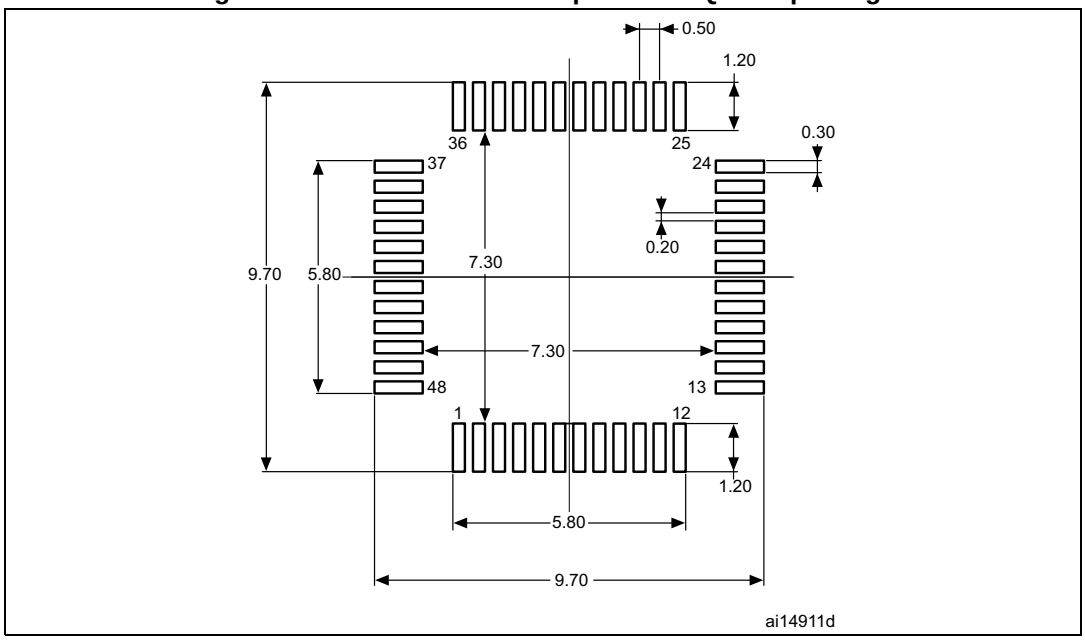

1. Drawing is not to scale.

**Table 78. LQFP48 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 50. Recommended footprint for LQFP48 package**



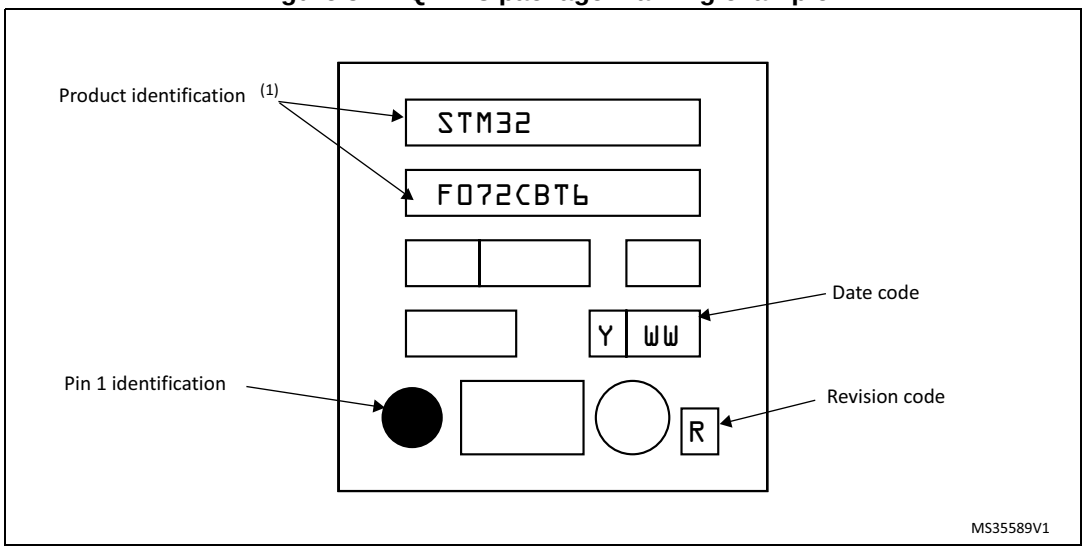

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 51. LQFP48 package marking example**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.