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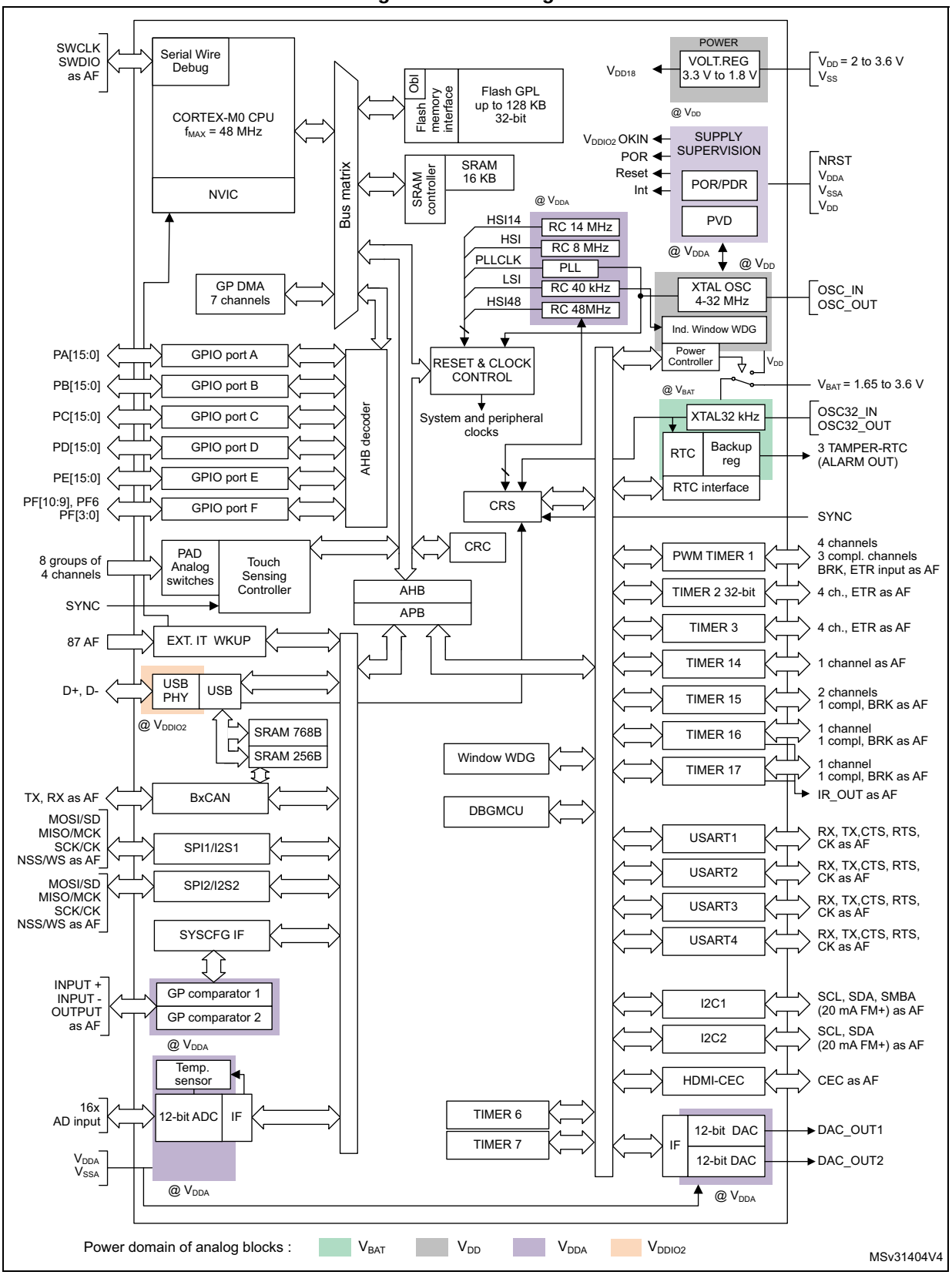
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

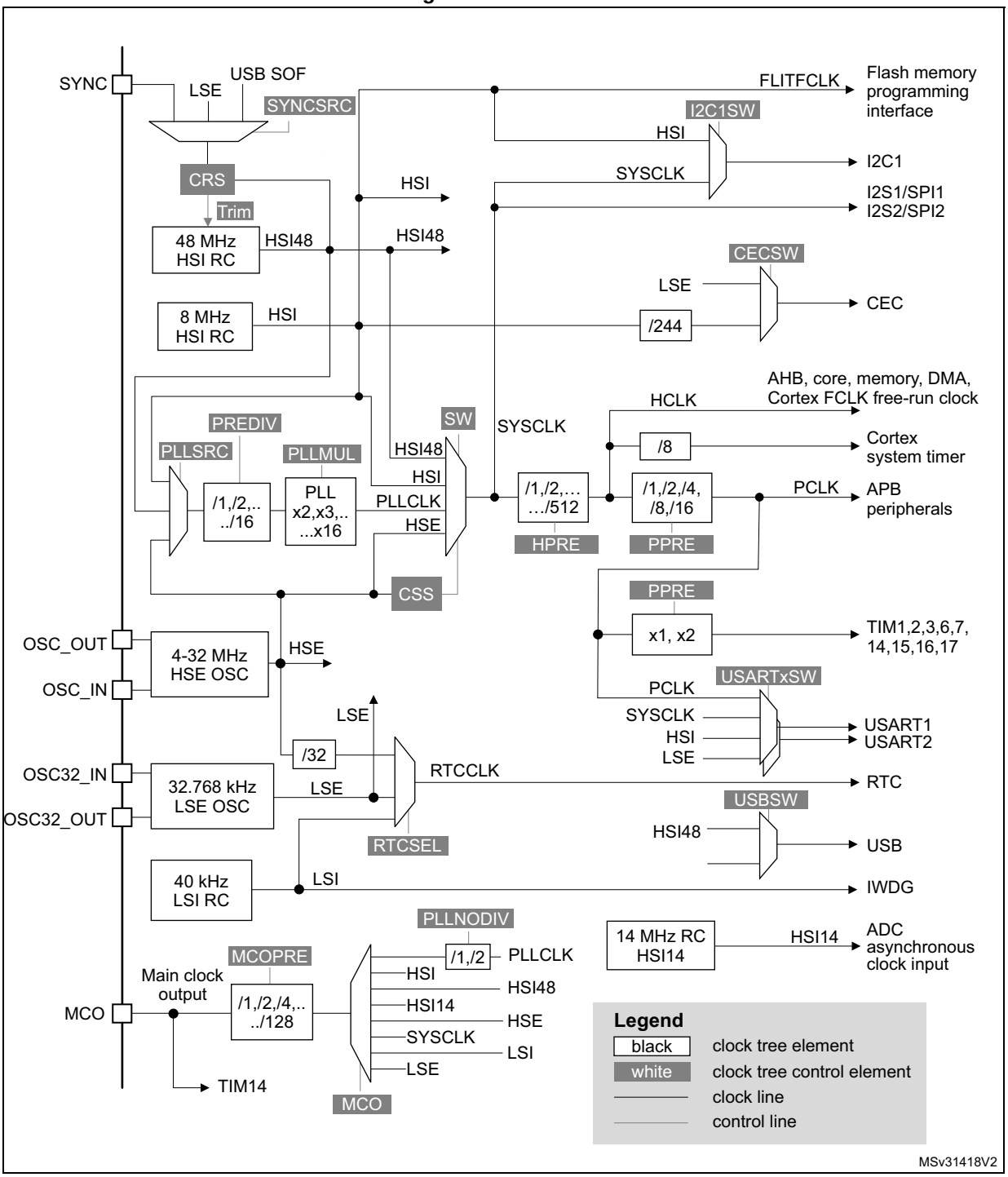
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	87
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f072v8t6

Figure 1. Block diagram



back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Figure 2. Clock tree



Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Table 10. STM32F072x8/xB USART implementation (continued)

USART modes/features(1)	USART1 and USART2	USART3 and USART4
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I^2S interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F072x8/xB SPI/I^2S implementation

SPI features(1)	SPI1 and SPI2
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I^2S mode	X
TI mode	X

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory

overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.21 Universal serial bus (USB)

The STM32F072x8/xB embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 byte are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.22 Clock recovery system (CRS)

The STM32F072x8/xB embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.23 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Figure 4. LQFP100 package pinout

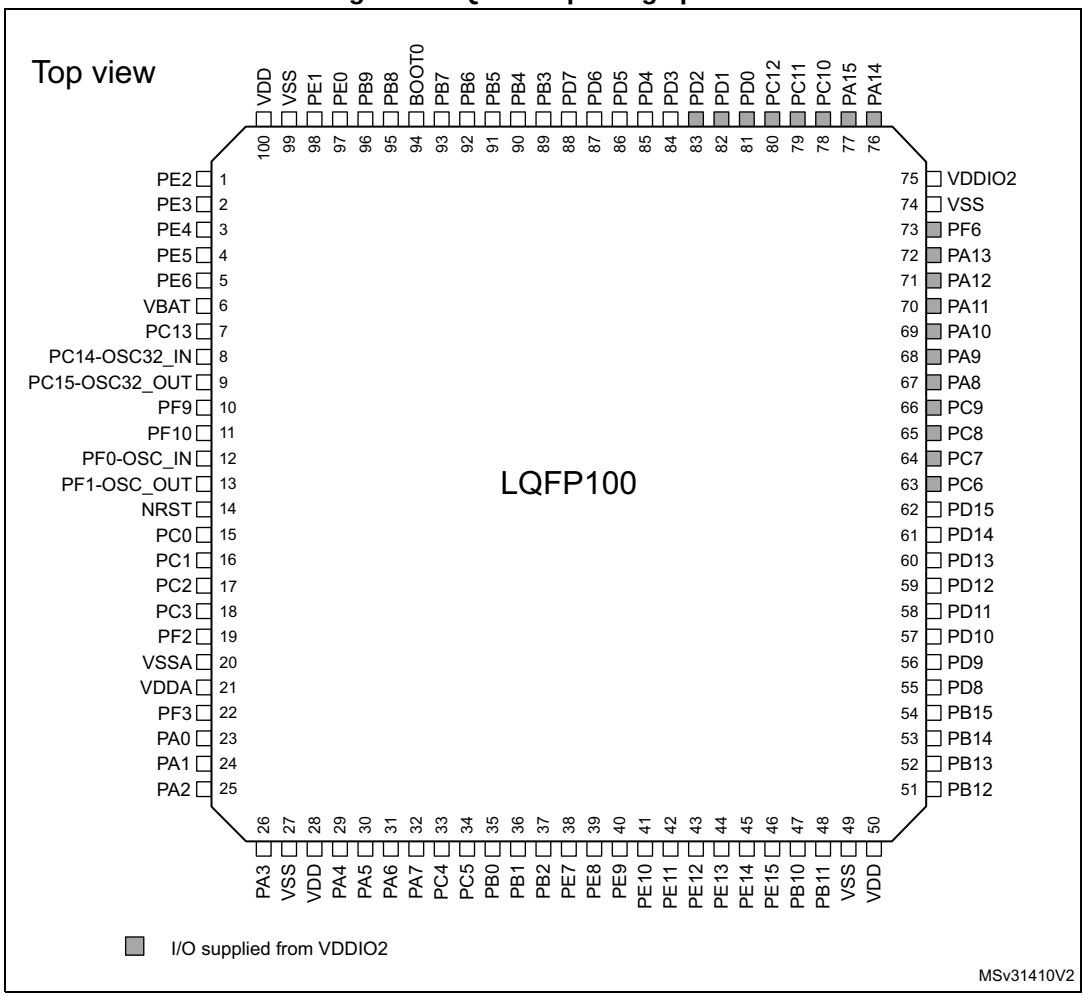


Table 13. STM32F072x8/xB pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
C10	79	B6	52	-	-	PC11	I/O	FT	(3)	USART3_RX, USART4_RX	-
B10	80	C5	53	-	-	PC12	I/O	FT	(3)	USART3_CK, USART4_CK	-
C9	81	-	-	-	-	PD0	I/O	FT	(3)	SPI2_NSS, I2S2_WS, CAN_RX	-
B9	82	-	-	-	-	PD1	I/O	FT	(3)	SPI2_SCK, I2S2_CK, CAN_TX	-
C8	83	B5	54	-	-	PD2	I/O	FT	(3)	USART3_RTS, TIM3_ETR	-
B8	84	-	-	-	-	PD3	I/O	FT	-	SPI2_MISO, I2S2_MCK, USART2_CTS	-
B7	85	-	-	-	-	PD4	I/O	FT	-	SPI2_MOSI, I2S2_SD, USART2_RTS	-
A6	86	-	-	-	-	PD5	I/O	FT	-	USART2_TX	-
B6	87	-	-	-	-	PD6	I/O	FT	-	USART2_RX	-
A5	88	-	-	-	-	PD7	I/O	FT	-	USART2_CK	-
A8	89	A5	55	39	A3	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
A7	90	A4	56	40	A4	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
C5	91	C4	57	41	B4	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
B5	92	D3	58	42	C4	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-

Table 14. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	USART4_TX	-	-	COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	USART4_RX	TIM15_CH1N	-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART2_CK	-	TSC_G2_IO1	TIM14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC	-	-	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1	-	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	-	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX	-	-	COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX	-	-	COMP2_OUT
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS	-	-	-

Table 20. STM32F072x8/xB peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21: Voltage characteristics*, *Table 22: Current characteristics* and *Table 23: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	- 0.3	4.0	V
V_{DDIO2}–V_{SS}	External I/O supply voltage	- 0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{BAT}–V_{SS}	External backup supply voltage	- 0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DDIOx} + 4.0(3)	V
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	V_{SS} - 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 30. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Para-meter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSI48	48 MHz	311	326	334	343	322	337	345	354	µA
		HSE bypass, PLL on	48 MHz	152	170(3)	178	182(3)	165	184(3)	196	200(3)	
			32 MHz	105	121	126	128	113	129	136	138	
			24 MHz	81.9	95.9	99.5	101	88.7	102	107	108	
		HSE bypass, PLL off	8 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
			1 MHz	2.7	3.8	4.3	4.6	3.6	4.7	5.2	5.5	
		HSI clock, PLL on	48 MHz	223	244	255	260	245	265	279	284	
			32 MHz	176	195	203	206	193	212	221	224	
			24 MHz	154	171	178	181	168	185	192	195	
		HSI clock, PLL off	8 MHz	74.2	83.4	86.4	87.3	83.4	92.5	95.3	96.6	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 33. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from V_{DD} supply	48 MHz	24.1	13.5	14.6	3.5	mA
		36 MHz	18.3	10.5	11.1	2.9	
		32 MHz	16.5	9.6	10.0	2.7	
		24 MHz	12.9	7.6	7.8	2.2	
		16 MHz	8.9	5.3	5.5	1.7	
		8 MHz	4.8	3.1	3.1	1.2	
		4 MHz	3.1	2.1	2.2	1.1	
		2 MHz	2.1	1.6	1.6	1.0	
		1 MHz	1.6	1.3	1.4	1.0	
		500 kHz	1.3	1.2	1.2	1.0	
I_{DDA}	Current consumption from V_{DDA} supply	48 MHz	163.3				µA
		36 MHz	124.3				
		32 MHz	111.9				
		24 MHz	87.1				
		16 MHz	62.5				
		8 MHz	2.5				
		4 MHz	2.5				
		2 MHz	2.5				
		1 MHz	2.5				
		500 kHz	2.5				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

Table 34. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3 V C =C_{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V_{DDIOx} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DDIOx} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V_{DDIOx} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DDIOx} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V_{DDIOx} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V_{DDIOx} = 2.4 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

Figure 22. TC and TTa I/O input characteristics

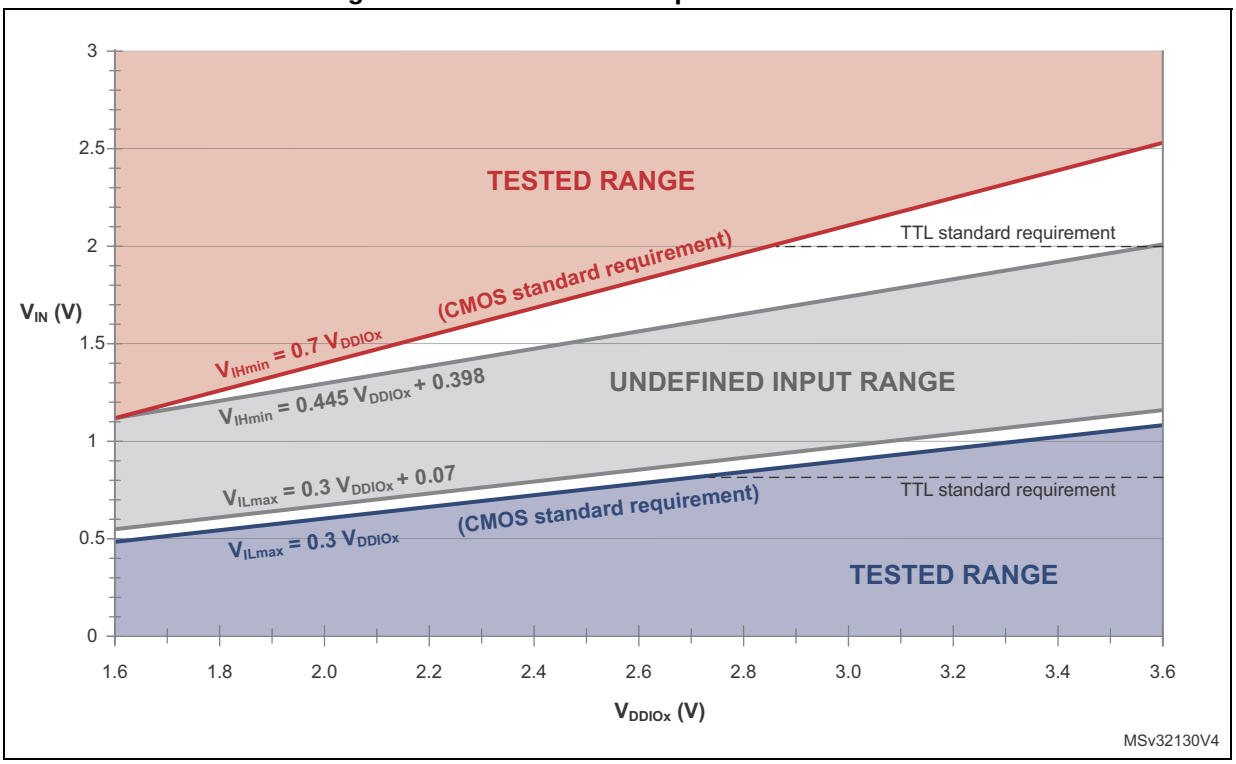


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

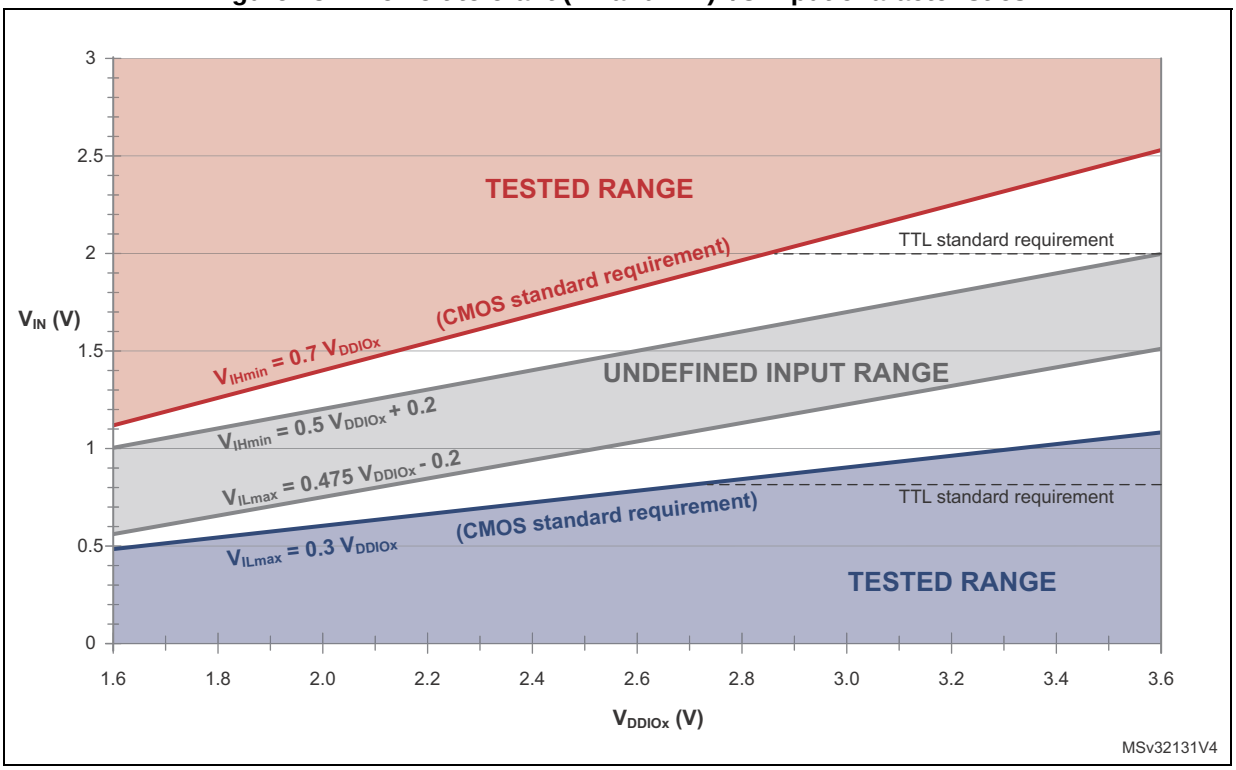


Table 57. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (2)	External input impedance	See *Equation 1* and *Table 58* for details	-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Table 67. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 68* for SPI or in *Table 69* for I²S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 68. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 30. SPI timing diagram - slave mode and CPHA = 0

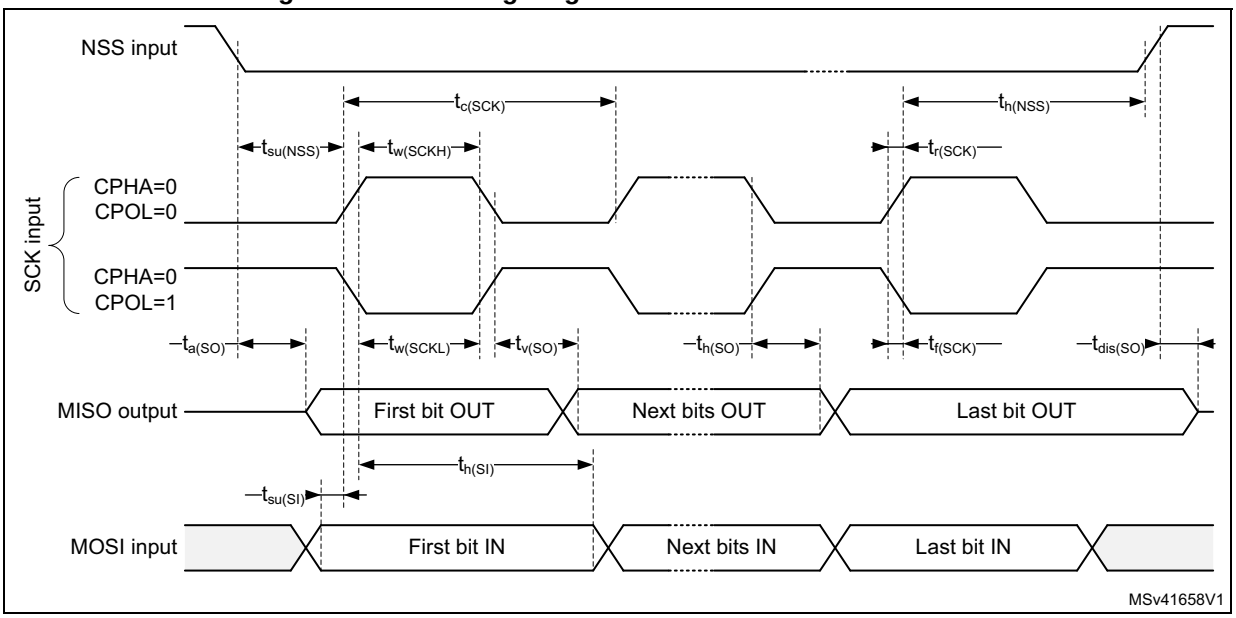
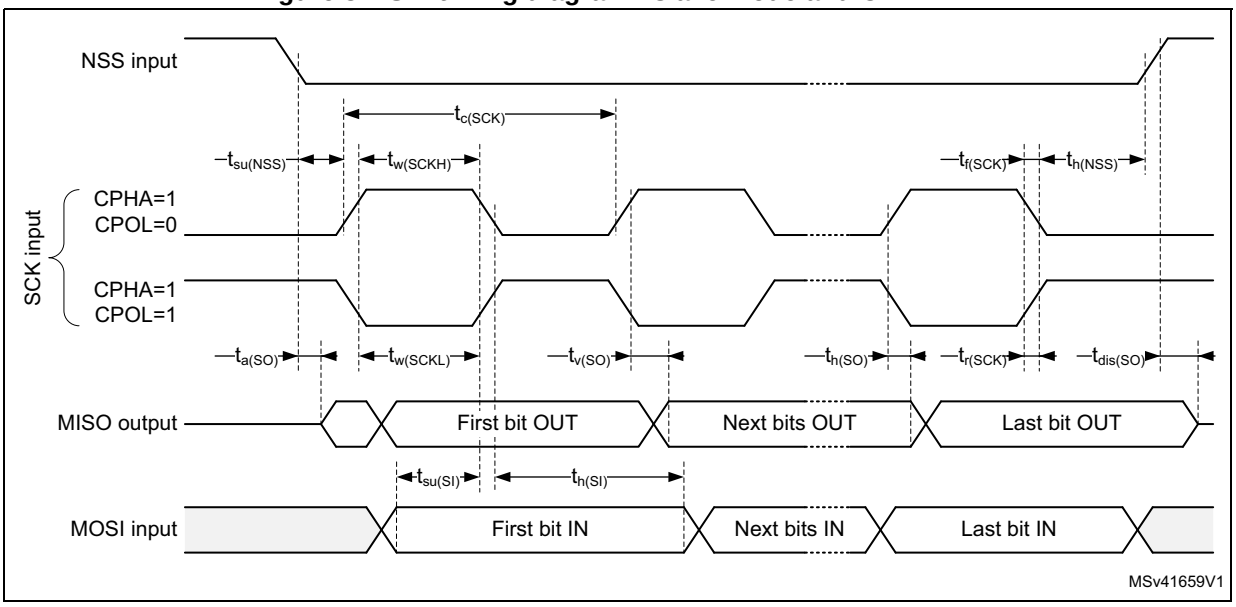


Figure 31. SPI timing diagram - slave mode and CPHA = 1



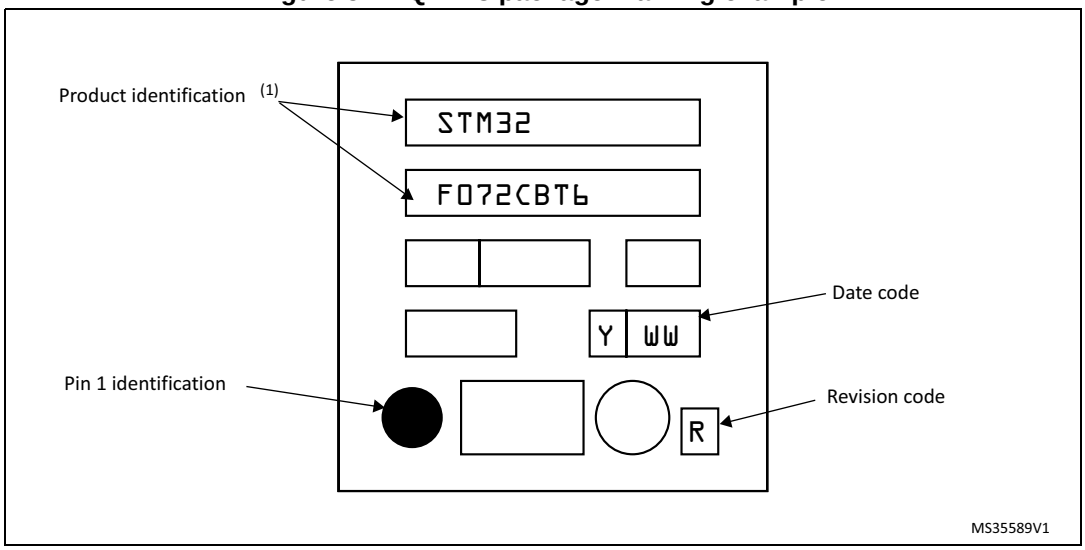
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 51. LQFP48 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 81. Ordering information scheme

Example: STM32 F 072 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

072 = STM32F072xx

Pin count

C = 48/49 pins

R = 64 pins

V = 100 pins

User code memory size

8 = 64 Kbyte

B = 128 Kbyte

Package

H = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = –40 to 85 °C

7 = –40 to 105 °C

Options

xxx = code ID of programmed parts (includes packing type)

TR = tape and reel packing

blank = tray packing

Table 82. Document revision history (continued)

Date	Revision	Changes
10-Jan-2017	5	***Section 6: Electrical characteristics*:** – *Table 40: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 28: Embedded internal reference voltage* - V_{REFINT} values – *Table 60: DAC characteristics* - min. R_{LOAD} to V_{DDA} defined – *Figure 30: SPI timing diagram - slave mode and CPHA = 0* and *Figure 31: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information*:** – The name of the section changed from the previous “Part numbering”