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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90usb1287-mu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Note: The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

2. Overview

The Atmel® AVR® AT90USB64/128 is a low-power CMOS 8-bit microcontroller based on the Atmel® AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90USB64/128 achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel AT90USB64/128 provides the following features: 64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 2K/4Kbytes EEPROM, 4K/8K bytes SRAM, 48 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), four flexible Timer/Counters with compare modes and PWM, one USART, a byte oriented 2-wire Serial Interface, a 8-channels, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using the Atmel high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the AT90USB64/128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90USB64/128 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Pin descriptions

- 2.2.1 VCC Digital supply voltage.
- 2.2.2 GND

Ground.

2.2.3 AVCC

Analog supply voltage.

2.2.4 Port A (PA7..PA0)

Port A is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel AT90USB64/128 as listed on page 78.

2.2.5 Port B (PB7..PB0)

Port B is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the AT90USB64/128 as listed on page 79.

2.2.6 Port C (PC7..PC0)

Port C is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the AT90USB64/128 as listed on page 82.

2.2.7 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90USB64/128 as listed on page 83.

2.2.8 Port E (PE7..PE0)

Port E is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the AT90USB64/128 as listed on page 86.

2.2.9 Port F (PF7..PF0)

Port F serves as analog inputs to the A/D Converter.

Port F also serves as an 8-bit bidirectional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.2.10	D-	USB Full speed / Low Speed Negative Data Upstream Port. Should be connected to the USB D-connector pin with a serial 22Ω resistor.
2.2.11	D+	USB Full speed / Low Speed Positive Data Upstream Port. Should be connected to the USB D+ connector pin with a serial 22 Ω resistor.
2.2.12	UGND	USB Pads Ground.
2.2.13	UVCC	USB Pads Internal Regulator Input supply voltage.
2.2.14	UCAP	USB Pads Internal Regulator Output supply voltage. Should be connected to an external capacitor (1 μ F).
2.2.15	VBUS	USB VBUS monitor and OTG negociations.
2.2.16	RESET	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 9-1 on page 58. Shorter pulses are not guaranteed to generate a reset.
2.2.17	XTAL1	Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.2.18	XTAL2	
		Output from the inverting oscillator amplifier.
2.2.19	AVCC	
		AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.
2.2.20	AREF	
		This is the analog reference pin for the A/D Converter.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

5. Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	-	-	-	-	-	-	-	-	
(0xFE)	Reserved	-	-	-	-	-	-	-	-	
(0xFD)	Reserved	-	-	-	-	-	-	-	-	
(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(0xFB)	Reserved	-	-	-	-	-	-	-	-	
(0xFA)	Reserved	-	-	-	-	-	-	-	-	
(0xF9)	OTGTCON		PA	GE				VA	LUE	
(0xF8)	UPINT				PII	NT7:0				
(0xF7)	UPBCHX	-	-	-	-	-		PBYCT10:8		
(0xF6)	UPBCLX				PB	/CT7:0				
(0xF5)	UPERRX	-	COUN	TER1:0	CRC16	TIMEOUT	PID	DATAPID	DATATGL	
(0xF4)	UEINT					EPINT6:0				
(0xF3)	UEBCHX	-	-	-	-	-		BYCT10:8		
(0xF2)	UEBCLX				BY	CT7:0				
(0xF1)	UEDATX				DA	AT7:0	•		n	
(0xF0)	UEIENX	FLERRE	NAKINE	-	NAKOUTE	RXSTPE	RXOUTE	STALLEDE	TXINE	
(0xEF)	UESTA1X	-	-	-	-	-	CTRLDIR	CURF	RBK1:0	
(0xEE)	UESTA0X	CFGOK	OVERFI	UNDERFI	-	DTSE	EQ1:0	NBUS	YBK1:0	
(0xED)	UECFG1X			EPSIZE2:0		EPB	3K1:0	ALLOC		
(0xEC)	UECFG0X	EPTY	'PE1:0				-	-	EPDIR	
(0xEB)	UECONX			STALLRQ	STALLRQC	RSTDT			EPEN	
(0xEA)	UERST					EPRST6:0				
(0xE9)	UENUM							EPNUM2:0		
(0xE8)	UEINTX	FIFOCON	NAKINI	RWAL	NAKOUTI	RXSTPI	RXOUTI	STALLEDI	TXINI	
(0xE7)	Reserved			-	-	-	-			
(0xE6)	UDMFN				FNCERR					
(0xE5)	UDFNUMH							FNUM10:8		
(0xE4)	UDFNUML		r		FN	UM7:0				
(0xE3)	UDADDR	ADDEN	UBBONE	FORME		UADD6:0	0055	1	011075	
(0xE2)	UDIEN		UPRSME	EORSME	WAKEUPE	EORSTE	SOFE		SUSPE	
(0xE1)	UDINI		UPRSMI	EORSMI	WAKEUPI	EORSTI	SOFI		SUSPI	
(0xE0)	ODCON			CTOI				NREPRI	DETACH	
(UXDF)	OTGINI			STOL	HNPERRI		BCERRI	VBERRI	SRPI	
(0xDE)	OTGIEN						NUCLINIC	VBUODEO	VELICEOC	
(0xDD) (0xDC)	Becariod			HINPREQ	SRPREQ	SRPSEL	VBUSHWC	VBUSREQ	VBUSRQU	
	Reserved									
	LISBINT							IDTI	VBUSTI	
(0xDA) (0xD9)						SPEED			VBUS	
(0xD8)	USBCON	USBE	HOST	EBZCLK	OTGPADE	OF EED		IDTE	VBUSTE	
(0xD7)	LIHWCON		LIDE	THEOLIN	LIVCONE			IDTE	UVBEGE	
(0xD6)	Reserved	Childe	0.02		0100112				o the de	
(0xD5)	Reserved									
(0xD4)	Reserved									
(0xD3)	Reserved									
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	Reserved	-	-	-	-	-	-	-	-	
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	UDR1				USART1 I/C	Data Register				
(0xCD)	UBRR1H	-	-	-	-	U U	SART1 Baud Rat	te Register High B	lyte	
(0xCC)	UBRR1L		•		JSART1 Baud Ra	ate Register Low I	Byte		-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	UCSR1C	UMSEL11	UMSEL10	UPM11	UPM10	USBS1	UCSZ11	UCSZ10	UCPOL1	
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	PE1	U2X1	MPCM1	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	Reserved	-	-	-	-	-	-	-	-	
(0xC5)	Reserved	-	-	-	-	-	-	-	-	
(0xC4)	Reserved	-	-	-	-	-	-	-	-	
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	Reserved	-	-	-	-	-	-	-	-	
(0xC1)	Reserved	-	-	-	-	-	-	-	-	
(0xC0)	Reserved	-	-	-	-	-	-	-	-	
(0xBF)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	
(0x7B)	ADCSRB	ADHSM	ACME	-	-	-	ADTS2	ADTS1	ADTS0	
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
(0x79)	ADCH				ADC Data Re	egister High byte				
(0x78)	ADCL		-	-	ADC Data R	egister Low byte	-		-	
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	XMCRB	XMBK	-	-	-	-	XMM2	XMM1	XMM0	
(0x74)	XMCRA	SRE	SRL2	SRL1	SRL0	SRW11	SRW10	SRW01	SRW00	
(0x73)	Reserved	-	-	-	-	-	-	-	-	
(0x72)	Reserved	-	-	-	-	-			-	
(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIESA	TOIE3	
(0x70)	TIMSK2	-	-		-				TOIE2	4
(0x6E)	TIMSKI			ICILI		OCILIC			TOIET	
	Beserved						OCILOB	OCILOA	TOILU	
(0x6C)	Reserved	-	-	-	-		-		-	
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	
(0x6A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	
(0x69)	EICRA	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	
(0x68)	PCICR	-	-	-	-	-	-	-	PCIE0	
(0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x66)	OSCCAL				Oscillator Cal	ibration Register	•		•	
(0x65)	PRR1	PRUSB	-	-	-	PRTIM3	-	-	PRUSART1	
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	-	PRADC	
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
0x3F (0x5F)	SREG	I	Т	н	S	V	N	Z	С	
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	RAMPZ	-	-	-	-	-	-	RAMPZ1	RAMPZ0	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	SPMCSP	- SDMIE	- D\\/\\/SB		- D\\/\\/SDE	- BI BSET	- PGW/PT	- PCEPS	- SDMEN	
0x37 (0x57)	Beconvod	SF WILL	HWW3B	SIGILD	nww.sni	DEDGET	FOWIT	FGENS	SP WILIN	
0x35 (0x55)	MCUCB	- ITD			PUD			IVSEI	IVCE	
0x34 (0x54)	MCUSB	-	-	-	JTBE	WDBE	BORE	EXTRE	POBE	
0x33 (0x53)	SMCB	-	-	-	-	SM2	SM1	SM0	SE	
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
	OCDR/	OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	
0x31 (0x51)	MONDR		1		Monitor D	Data Register				
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR				SPI Da	ta Register				
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	
0x2B (0x4B)	GPIOR2				General Purpo	ose I/O Register 2				
0x2A (0x4A)	GPIOR1				General Purpo	ose I/O Register 1				
0x29 (0x49)	PLLCSR	-	-	-	PLLP2	PLLP1	PLLP0	PLLE	PLOCK	
0x28 (0x48)	OCR0B			Tim	ner/Counter0 Out	put Compare Reg	ister B			
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								
0x26 (0x46)	TCNT0				Timer/Co	unter0 (8 Bit)				
0x25 (0x45)	TCCR0B	FOCOA	FOCOB	-	-	WGM02	CS02	CS01	CS00	
0x24 (0x44)	ICCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	
0x23 (0x43)	GICCR	ISM	-	-	-	-	-	PSRASY	PSRSYNC	
0x22 (0x42)	EEARH	-	-	-		Pagiotar Law D	LEPHOM Addres	s Register High B	yte	
0x21 (0x41)	EEAKL					os riegisier LOW B	yıe			
0x1E (0x2E)	FECP		_	EEDM1	EEPMO		FEMDE	FEDE	FEDE	+
0x1F (0x3F)	GPIORO	-			General Purpo	se I/O Begister 0				1
0x1D (0x3D)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	
0x1C (0x3C)	EIFR	INTF7	INTF6	INTE5	INTF4	INTF3	INTF2	INTF1	INTFO	1
								· · · · · · · · · · · · · · · · · · ·		

6. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
	ARITHME	TIC AND LOGIC INSTRUCTIONS			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Z,C,N,V,H	1	
SUBI	Rd, K	Subtract Constant from Register	Z,C,N,V,H	1	
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF - Rd	Z,C,N,V	1
NEG	Rd	I wo's Complement		Z,C,N,V,H	1
SBR	Ra,K	Clear Bit(s) in Register		Z,N,V	1
UBR	Ru,r		$Rd \leftarrow Rd \bullet (0XFF - K)$	Z,IN,V	1
	Ra	Increment		Z,N,V	1
DEC	Ru	Toot for Zoro or Minus	$Ru \leftarrow Ru - I$	Z,IN, V	1
CLP	Pd	Clear Bogister		Z,N,V	1
SEB	Bd	Set Bogister		None	1
MUI	Bd Br	Multiply Linsigned	$B1:B0 \leftarrow Bd \times Br$	ZC	2
MULS	Bd Br	Multiply Signed	$B1:B0 \leftarrow Bd \times Br$	Z,0	2
MULSU	Bd Br	Multiply Signed	$B1:B0 \leftarrow Bd \times Br$	Z,0	2
FMUI	Bd Br	Fractional Multiply Unsigned	$B1:B0 \leftarrow (Bd \times Br) << 1$	Z,0	2
FMULS	Bd Br	Fractional Multiply Signed	$B1:B0 \leftarrow (Bd \times Br) << 1$	Z,0	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$B1:B0 \leftarrow (Bd \times Br) << 1$	Z.C	2
	BI	RANCH INSTRUCTIONS	•		
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
EIJMP		Extended Indirect Jump to (Z)	PC ←(EIND:Z)	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	4
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	4
EICALL		Extended Indirect Call to (Z)	$PC \leftarrow (EIND:Z)$	None	4
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	5
RET		Subroutine Return	$PC \leftarrow STACK$	None	5
RETI		Interrupt Return	$PC \leftarrow STACK$	1	5
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate Rd – K		Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(\operatorname{Rr}(b)=0)$ PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(\text{Rr}(b)=1) \text{ PC} \leftarrow \text{PC} + 2 \text{ or } 3$	None	1/2/3
SBIC	P,D	Skip II BIT IN I/O Register Cleared	ii $(P(b)=0) PO \leftarrow PO + 2 \text{ or } 3$	None	1/2/3
	г, D	Branch if Status Elas Sat	if $(PEC(c) = 1)$ then $PC \in PC + 2$ of 3 if $(PEC(c) = 1)$ then $PC \in PC + 1$	None	1/2/3
BPBC	5, K	Branch if Status Flag Oleared	if $(SREG(s) = 1)$ then $PC \leftarrow PC + K + 1$ if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREO	k s, n	Branch if Foual	if $(7 = 1)$ then PC \leftarrow PC + k + 1	None	1/2
BRNF	k	Branch if Not Foual	if $(Z = 0)$ then PC \leftarrow PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then PC \leftarrow PC + k + 1	None	1/2
BRCC	 k	Dranch if Carry ClearedIf $(C = 1)$ then PC \leftarrow PC + k + 1Branch if Carry Clearedif $(C = 0)$ then PC \leftarrow PC + k + 1		None	1/2
BRSH	k	Branch if Same or Higher if $(C = 0)$ then PC \leftarrow PC + K + 1		None	1/2
BRLO	k	Branch if LowerIf $(C = 0)$ then $PC \leftarrow PC + k + 1$		None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V= 0) then PC \leftarrow PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC \leftarrow PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC \leftarrow PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC \leftarrow PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC \leftarrow PC + k + 1	None	1/2

7.2 Atmel AT90USB647

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB647-AU AT90USB647-MU	USB OTG	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 × 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

7.4 Atmel AT90USB1287

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB1287-AU AT90USB1287-MU	Host (OTG)	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 × 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

6. VBUS session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

5. UBS signal rate

The average USB signal rate may sometime be measured out of the USB specifications $(12MHz \pm 30kHz)$ with short frames. When measured on a long period, the average signal rate value complies with the specifications. This bit rate deviation does not generates communication or functional errors.

Problem fix/workaround

None.

4. VBUS residual level

In USB device and host mode, once a 5V level has been detected to the VBUS pad, a residual level (about 3V) can be measured on the VBUS pin.

Problem fix/workaround

None.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

9.1.3 Atmel AT90USB1287/6 second release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- VBUS Session valid threshold voltage
- Spike on TWI pins when TWI is enabled
- · High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

7. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

6. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

5. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

4. VBUS session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

9.1.4 Atmel AT90USB1287/6 Third Release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- · Async timer interrupt wake up from sleep generate multiple interrupts

5. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable AT90USB64/128 TWI first, before the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from sleep mode should be disabled.

Asynchronous timer interrupt wake up from sleep generates multiple interrupts
 If the CPU core is in sleep mode and wakes-up from an asynchronous timer interrupt and
 then goes back into sleep mode, it may wake up multiple times.

Problem fix/workaround

A software workaround is to wait before performing the sleep instruction: until TCNT2>OCR2+1.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

9.2.3 Atmel AT90USB646/7 Second Release.

- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

5. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

10. Datasheet revision history for Atmel AT90USB64/128

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

10.1 Changes from 7593A to 7593B

- 1. Changed default configuration for fuse bytes and security byte.
- 2. Suppression of timer 4,5 registers which does not exist.
- 3. Updated typical application schematics in USB section

10.2 Changes from 7593B to 7593C

1. Update to package drawings, MQFP64 and TQFP64.

10.3 Changes from 7593C to 7593D

 For further product compatibility, changed USB PLL possible prescaler configurations. Only 8MHz and 16MHz crystal frequencies allows USB operation (see Table 7-11 on page 50).

10.4 Changes from 7593D to 7593E

- 1. Updated PLL Prescaler table: configuration words are different between AT90USB64x and AT90USB128x to enable the PLL with a 16MHz source.
- 2. Cleaned up some bits from USB registers, and updated information about OTG timers, remote wake-up, reset and connection timings.
- 3. Updated clock distribution tree diagram (USB prescaler source and configuration register).
- 4. Cleaned up register summary.
- 5. Suppressed PCINT23:8 that do not exist from External Interrupts.
- 6. Updated Electrical Characteristics.
- 7. Added Typical Characteristics.
- 8. Update Errata section.

10.5 Changes from 7593E to 7593F

- 1. Removed 'Preliminary' from document status.
- 2. Clarification in Stand by mode regarding USB.

10.6 Changes from 7593F to 7593G

1. Updated Errata section.

10.7 Changes from 7593G to 7593H

- 1. Added Signature information for 64K devices.
- 2. Fixed figure for typical bus powered application
- 3. Added min/max values for BOD levels
- 4. Added ATmega32U6 product
- 5. Update Errata section
- 6. Modified descriptions for HWUPE and WAKEUPE interrupts enable (these interrupts should be enabled only to wake up the CPU core from power down mode).

10.8 Changes from 7593H to 7593I

1. Updated Table 9-2 in "Brown-out detection" on page 60. Unused BOD levels removed.

10.9 Changes from 7593I to 7593J

- 1. Updated Table 9-2 in "Brown-out detection" on page 60. BOD level 100 removed.
- 2. Updated "Ordering information" on page 18.
- 3. Removed ATmega32U6 errata section.

10.10 Changes from 7593J to 7593K

- 1. Corrected Figure 6-7 on page 34, Figure 6-8 on page 34 and Figure 6-9 on page 35.
- Corrected ordering information for Section 7.3 "Atmel AT90USB1286" on page 20, Section 7.4 "Atmel AT90USB1287" on page 21 and Section 7.2 "Atmel AT90USB647" on page 19.
- 3. Removed the ATmega32U6 device and updated the datasheet accordingly.
- 4. Updated Assembly Code Example in "Watchdog reset" on page 61.

10.11 Changes from 7593K to 7593L

- 1. Updated the "Ordering information" on page 18. Changed the speed from 20MHz to 16MHz.
- 2. Replaced ATmegaAT90USBxxxx by AT90USBxxxx through the datasheet.
- 3. Updated the first paragraph of "Overview" on page 307. Port A replaced by Port F.
- 4. Updated ADC equation in "ADC conversion result" on page 318. The equation has 1024 instead of 1023.
- 5. Created "Packaging Information" chapter.
- 6. Replaced the "QFN64" Packaging by an updated QFN64 Packaging drawing.
- 7. Updated "Errata" on page 26. AT90USB1286/7 has a fourth release, while AT90USB646/7 updated with a second release.
- 8. In Section "Overview" on page 307, "Port A" has been replaced by "Port F" in the first section.
- 9. In Section "Atmel AT90USB647" on page 19 the USB interface has been changed to USB OTG.
- 10. In Section "Atmel AT90USB1286" on page 20 the USB interface has been changed to Device.
- 11. In Section "Atmel AT90USB1287" on page 21 the USB interface has been changed to Host OTG.
- 12. General update according to new template.

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