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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

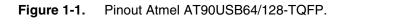
Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90usb646-au

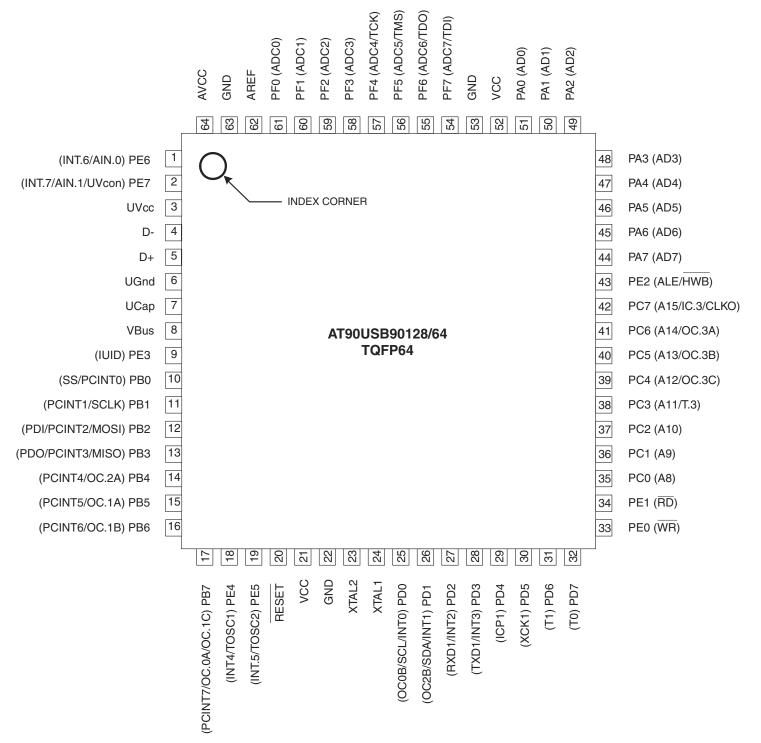
Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Real time counter with separate oscillator
- Four 8-bit PWM channels
- Six PWM channels with programmable resolution from 2 to 16 bits
- Output compare modulator
- 8-channels, 10-bit ADC
- Programmable serial USART
- Master/slave SPI serial interface
- Byte oriented 2-wire serial interface
- Programmable watchdog timer with separate on-chip oscillator
- On-chip analog comparator
- Interrupt and wake-up on pin change
- Special microcontroller features
 - Power-on reset and programmable brown-out detection
 - Internal calibrated oscillator
 - External and internal interrupt sources
 - Six sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and packages
 - 48 programmable I/O lines
 - 64-lead TQFP and 64-lead QFN
- Operating voltages
 - 2.7 5.5V
- Operating temperature
- Industrial (-40°C to +85°C)
- Maximum frequency
 - 8MHz at 2.7V industrial range
 - 16MHz at 4.5V industrial range

1. Pin configurations





2. Overview

The Atmel® AVR® AT90USB64/128 is a low-power CMOS 8-bit microcontroller based on the Atmel® AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90USB64/128 achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel AT90USB64/128 provides the following features: 64/128Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 2K/4Kbytes EEPROM, 4K/8K bytes SRAM, 48 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), four flexible Timer/Counters with compare modes and PWM, one USART, a byte oriented 2-wire Serial Interface, a 8-channels, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using the Atmel high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the AT90USB64/128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90USB64/128 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Pin descriptions

- 2.2.1 VCC Digital supply voltage.
- 2.2.2 GND

Ground.

2.2.3 AVCC

Analog supply voltage.

2.2.4 Port A (PA7..PA0)

Port A is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel AT90USB64/128 as listed on page 78.

2.2.5 Port B (PB7..PB0)

Port B is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the AT90USB64/128 as listed on page 79.

2.2.6 Port C (PC7..PC0)

Port C is an 8-bit bidirectional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the AT90USB64/128 as listed on page 82.

2.2.7 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90USB64/128 as listed on page 83.

5. Register summary

										_
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	-	-	-	-	-	-	-	-	
(0xFE)	Reserved	-	-	-	-	-	-	-	-	
(0xFD)	Reserved	-	-	-	-	-	-	-	-	
(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(0xFB)	Reserved	-	-	-	-	-	-	-	-	
(0xFA)	Reserved	-	-	-	-	-	-	-	-	
(0xF9)	OTGTCON		PA	AGE				VA	LUE	
(0xF8)	UPINT				PII	NT7:0				
(0xF7)	UPBCHX	-	-	-	-	-		PBYCT10:8		
(0xF6)	UPBCLX		0.011	TEDIA	1	/CT7:0	212	DATADID	DATATO	
(0xF5)	UPERRX	-	COUN	ITER1:0	CRC16	TIMEOUT	PID	DATAPID	DATATGL	
(0xF4)	UEINT	-		-		EPINT6:0	1	DVCT10.0		
(0xF3)	UEBCHX UEBCLX		-	-	- PV			BYCT10:8		
(0xF2) (0xF1)	UEDATX	<u> </u>				AT7:0				
(0xF0)	UEIENX	FLERRE	NAKINE	-	NAKOUTE	RXSTPE	RXOUTE	STALLEDE	TXINE	
(0xEF)	UESTA1X	-	-	-	-	-	CTRLDIR		RBK1:0	
(0xEE)	UESTAOX	CFGOK	OVERFI	UNDERFI	-		EQ1:0		SYBK1:0	
(0xED)	UECFG1X	ordore	OVENIT	EPSIZE2:0			SK1:0	ALLOC	JI DICT.0	
(0xEC)	UECFG0X	FPTY	YPE1:0	L. C.LLL.U			-	-	EPDIR	
(0xEB)	UECONX		1	STALLRQ	STALLRQC	RSTDT			EPEN	
(0xEA)	UERST					EPRST6:0		1		
(0xE9)	UENUM							EPNUM2:0		
(0xE8)	UEINTX	FIFOCON	NAKINI	RWAL	NAKOUTI	RXSTPI	RXOUTI	STALLEDI	TXINI	
(0xE7)	Reserved			-	-	-	-	-		
(0xE6)	UDMFN				FNCERR					
(0xE5)	UDFNUMH							FNUM10:8		
(0xE4)	UDFNUML				FN	UM7:0				
(0xE3)	UDADDR	ADDEN				UADD6:0				
(0xE2)	UDIEN		UPRSME	EORSME	WAKEUPE	EORSTE	SOFE		SUSPE	
(0xE1)	UDINT		UPRSMI	EORSMI	WAKEUPI	EORSTI	SOFI		SUSPI	
(0xE0)	UDCON						LSM	RMWKUP	DETACH	
(0xDF)	OTGINT			STOI	HNPERRI	ROLEEXI	BCERRI	VBERRI	SRPI	
(0xDE)	OTGIEN			STOE	HNPERRE	ROLEEXE	BCERRE	VBERRE	SRPE	
(0xDD)	OTGCON			HNPREQ	SRPREQ	SRPSEL	VBUSHWC	VBUSREQ	VBUSRQC	
(0xDC)	Reserved									
(0xDB)	Reserved									
(0xDA)	USBINT							IDTI	VBUSTI	
(0xD9)	USBSTA					SPEED		ID	VBUS	
(0xD8)	USBCON	USBE	HOST	FRZCLK	OTGPADE			IDTE	VBUSTE	
(0xD7)	UHWCON	UIMOD	UIDE		UVCONE				UVREGE	
(0xD6)	Reserved									
(0xD5)	Reserved		<u> </u>		-					
(0xD4)	Reserved									
(0xD3)	Reserved									
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0) (0xCF)	Reserved Reserved	-	-	-	-	-	-	-	-	
(0xCF) (0xCE)	UDR1			-		- Data Register	-	-	-	
(0xCE) (0xCD)	UBRR1H	-	-	-	- USARTTI/C		ISART1 Raud Pot	te Register High E	Byte	
(0xCD) (0xCC)	UBRR1L				JSART1 Baud Ra			io negister might E	5310	
(0xCB)	Reserved	-	-	-	-		-	-	-	
(0xCB)	UCSR1C	- UMSEL11	- UMSEL10	- UPM11	- UPM10	- USBS1	UCSZ11	UCSZ10	UCPOL1	
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	PE1	U2X1	MPCM1	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	Reserved	-	-	-	-	-	-	-	-	
(0xC5)	Reserved	-	-	-	-	-	-	-	-	
(0xC4)	Reserved	-	-	-	-	-	-	-	-	
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	Reserved	-	-	-	-	-	-	-	-	
									-	
(0xC1)	Reserved	-	-	-	-	-	-	-	-	
	Reserved Reserved	-	-	-	-	-	-	-	-	

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2
	BIT AN	D BIT-TEST INSTRUCTIONS		-	
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd Rd	Rotate Left Through Carry Rotate Right Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$\frac{Rd(7)\leftarrow C,Rd(n)\leftarrow Rd(n+1),C\leftarrow Rd(0)}{Rd(n)\leftarrow Rd(n+1), n=06}$	Z,C,N,V Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	s	Flag Set	SREG(s) $\leftarrow 1$	SREG(s)	1
BCLR	S	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	C ← 0	С	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	Ν	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	←1	1	1
CLI		Global Interrupt Disable		1	1
SES		Set Signed Test Flag	<u>S</u> ← 1	s	1
CLS SEV		Clear Signed Test Flag	S ← 0 V ← 1	S V	1
CLV		Set Twos Complement Overflow. Clear Twos Complement Overflow	$V \leftarrow 1$ $V \leftarrow 0$	v	1
SET		Set T in SREG	T ← 1	т	1
CLT		Clear T in SREG	T ← 0	Т	1
SEH		Set Half Carry Flag in SREG	H ← 1	Н	1
CLH		Clear Half Carry Flag in SREG	H ← 0	н	1
	DATA	TRANSFER INSTRUCTIONS			
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD LDD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q Rd, Z	Load Indirect with Displacement Load Indirect	$Rd \leftarrow (Y + q)$ $Rd \leftarrow (Z)$	None	2
LD	Ru, Z Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
STD	7 0	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z, Rr		$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST ST	Z+, Rr	Store Indirect and Post-Inc.			~
ST ST ST	Z+, Rr -Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1$, (Z) $\leftarrow Rr$	None	2
ST ST ST STD	Z+, Rr -Z, Rr Z+q,Rr	Store Indirect and Pre-Dec. Store Indirect with Displacement	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$	None	2
ST ST ST STD STS	Z+, Rr -Z, Rr	Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM	$\begin{array}{c} Z \leftarrow Z \cdot 1, (Z) \leftarrow Rr \\ (Z + q) \leftarrow Rr \\ (k) \leftarrow Rr \end{array}$	None None	2 2
ST ST ST STD STS LPM	Z+, Rr -Z, Rr Z+q,Rr k, Rr	Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory	$\begin{array}{c} Z\leftarrow Z-1, (Z)\leftarrow Rr\\ (Z+q)\leftarrow Rr\\ (k)\leftarrow Rr\\ R0\leftarrow (Z) \end{array}$	None None None	2 2 3
ST ST STD STD STS LPM LPM	Z+, Rr -Z, Rr Z+q,Rr k, Rr Rd, Z	Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory	$\begin{array}{c} Z \leftarrow Z - 1, (Z) \leftarrow Rr \\ (Z + q) \leftarrow Rr \\ \hline \\ (k) \leftarrow Rr \\ \hline \\ R0 \leftarrow (Z) \\ \hline \\ Rd \leftarrow (Z) \end{array}$	None None None None	2 2 3 3
ST ST STD STD STS LPM LPM LPM	Z+, Rr -Z, Rr Z+q,Rr k, Rr	Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory Load Program Memory and Post-Inc	$\begin{array}{c c} Z \leftarrow Z - 1, (Z) \leftarrow Rr \\ (Z + q) \leftarrow Rr \\ \hline \\ (k) \leftarrow Rr \\ \hline \\ R0 \leftarrow (Z) \\ \hline \\ Rd \leftarrow (Z) \\ \hline \\ Rd \leftarrow (Z), Z \leftarrow Z+1 \end{array}$	None None None None None	2 2 3 3 3 3
ST ST STD STD STS LPM LPM	Z+, Rr -Z, Rr Z+q,Rr k, Rr Rd, Z	Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory	$\begin{array}{c} Z \leftarrow Z - 1, (Z) \leftarrow Rr \\ (Z + q) \leftarrow Rr \\ \hline \\ (k) \leftarrow Rr \\ \hline \\ R0 \leftarrow (Z) \\ \hline \\ Rd \leftarrow (Z) \end{array}$	None None None None	2 2 3 3

7.2 Atmel AT90USB647

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB647-AU AT90USB647-MU	USB OTG	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 × 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

7.3 Atmel AT90USB1286

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB1286-AU AT90USB1286-MU	Device	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

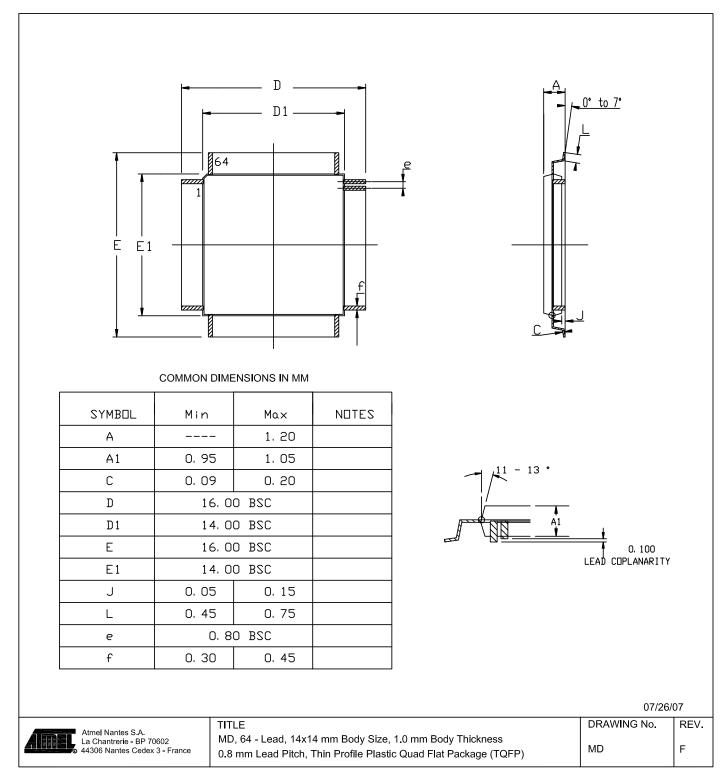
2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

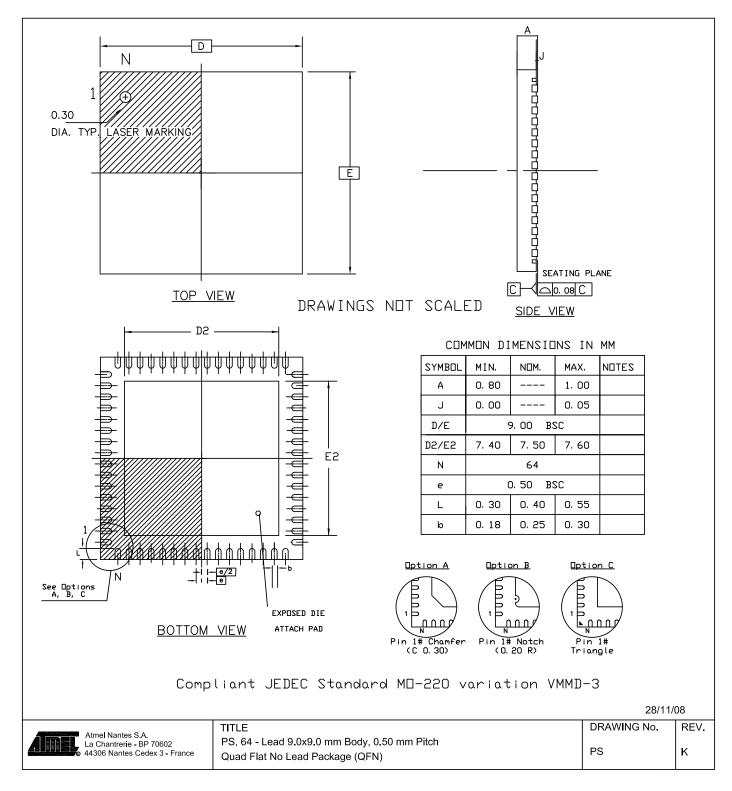
3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 \times 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

8. Packaging information

8.1 TQFP64





NOTES: QFN STANDARD NOTES

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1994.

2. DIMENSION & APPLIES TO METALLIZED TERMINAL AND IS MEASURED

BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION & SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

3. MAX. PACKAGE WARPAGE IS 0.05mm.

4. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

5. PIN #1 ID ON TOP WILL BE LASER MARKED.

6. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220.

7. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.30 mm

8. THE TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER BE EITHER A MOLD OR MARKED FEATURE

9. Errata

9.1 Atmel AT90USB1287/6 errata

9.1.1 AT90USB1287/6 errata history

Silicon Release	90USB1286-16MU	90USB1287-16AU	90USB1287-16MU
First Release	Date Code up to 0648	Date Code up to 0714 and lots 0735 6H2726 ⁽¹⁾	Date Code up to 0701
Second Release	Date Code from 0709 to 0801 except lots 0801 7H5103 ⁽¹⁾	from Date Code 0722 to 0806 except lots 0735 6H2726 ⁽¹⁾	Date Code from 0714 to 0810 except lots 0748 7H5103 ⁽¹⁾
Third Release	Lots 0801 7H5103 ⁽¹⁾ and Date Code from 0814	Date Code from 0814	Lots 0748 7H5103 ⁽¹⁾ and Date Code from 0814
Fourth Release	TBD	TBD	TBD

Notes: 1. A blank or any alphanumeric string.

9.1.2 AT90USB1287/6 first release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- VBUS Session valid threshold voltage
- USB signal rate
- VBUS residual level
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- · Async timer interrupt wake up from sleep generate multiple interrupts

9. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

8. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

7. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep again it may wake up multiple times.

Problem fix/workaround

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep again it may wake up multiple times.

Problem fix/workaround

9.1.4 Atmel AT90USB1287/6 Third Release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- · Async timer interrupt wake up from sleep generate multiple interrupts

5. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable AT90USB64/128 TWI first, before the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from sleep mode should be disabled.

Asynchronous timer interrupt wake up from sleep generates multiple interrupts
 If the CPU core is in sleep mode and wakes-up from an asynchronous timer interrupt and
 then goes back into sleep mode, it may wake up multiple times.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem fix/workaround

9.2.3 Atmel AT90USB646/7 Second Release.

- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

5. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem fix/workaround

10. Datasheet revision history for Atmel AT90USB64/128

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

10.1 Changes from 7593A to 7593B

- 1. Changed default configuration for fuse bytes and security byte.
- 2. Suppression of timer 4,5 registers which does not exist.
- 3. Updated typical application schematics in USB section

10.2 Changes from 7593B to 7593C

1. Update to package drawings, MQFP64 and TQFP64.

10.3 Changes from 7593C to 7593D

 For further product compatibility, changed USB PLL possible prescaler configurations. Only 8MHz and 16MHz crystal frequencies allows USB operation (see Table 7-11 on page 50).

10.4 Changes from 7593D to 7593E

- 1. Updated PLL Prescaler table: configuration words are different between AT90USB64x and AT90USB128x to enable the PLL with a 16MHz source.
- 2. Cleaned up some bits from USB registers, and updated information about OTG timers, remote wake-up, reset and connection timings.
- 3. Updated clock distribution tree diagram (USB prescaler source and configuration register).
- 4. Cleaned up register summary.
- 5. Suppressed PCINT23:8 that do not exist from External Interrupts.
- 6. Updated Electrical Characteristics.
- 7. Added Typical Characteristics.
- 8. Update Errata section.

10.5 Changes from 7593E to 7593F

- 1. Removed 'Preliminary' from document status.
- 2. Clarification in Stand by mode regarding USB.

10.6 Changes from 7593F to 7593G

1. Updated Errata section.

10.7 Changes from 7593G to 7593H

- 1. Added Signature information for 64K devices.
- 2. Fixed figure for typical bus powered application
- 3. Added min/max values for BOD levels
- 4. Added ATmega32U6 product
- 5. Update Errata section
- 6. Modified descriptions for HWUPE and WAKEUPE interrupts enable (these interrupts should be enabled only to wake up the CPU core from power down mode).

10.8 Changes from 7593H to 7593I

1. Updated Table 9-2 in "Brown-out detection" on page 60. Unused BOD levels removed.

10.9 Changes from 7593I to 7593J

- 1. Updated Table 9-2 in "Brown-out detection" on page 60. BOD level 100 removed.
- 2. Updated "Ordering information" on page 18.
- 3. Removed ATmega32U6 errata section.

10.10 Changes from 7593J to 7593K

- 1. Corrected Figure 6-7 on page 34, Figure 6-8 on page 34 and Figure 6-9 on page 35.
- Corrected ordering information for Section 7.3 "Atmel AT90USB1286" on page 20, Section 7.4 "Atmel AT90USB1287" on page 21 and Section 7.2 "Atmel AT90USB647" on page 19.
- 3. Removed the ATmega32U6 device and updated the datasheet accordingly.
- 4. Updated Assembly Code Example in "Watchdog reset" on page 61.

10.11 Changes from 7593K to 7593L

- 1. Updated the "Ordering information" on page 18. Changed the speed from 20MHz to 16MHz.
- 2. Replaced ATmegaAT90USBxxxx by AT90USBxxxx through the datasheet.
- 3. Updated the first paragraph of "Overview" on page 307. Port A replaced by Port F.
- 4. Updated ADC equation in "ADC conversion result" on page 318. The equation has 1024 instead of 1023.
- 5. Created "Packaging Information" chapter.
- 6. Replaced the "QFN64" Packaging by an updated QFN64 Packaging drawing.
- 7. Updated "Errata" on page 26. AT90USB1286/7 has a fourth release, while AT90USB646/7 updated with a second release.
- 8. In Section "Overview" on page 307, "Port A" has been replaced by "Port F" in the first section.
- 9. In Section "Atmel AT90USB647" on page 19 the USB interface has been changed to USB OTG.
- 10. In Section "Atmel AT90USB1286" on page 20 the USB interface has been changed to Device.
- 11. In Section "Atmel AT90USB1287" on page 21 the USB interface has been changed to Host OTG.
- 12. General update according to new template.