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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90usb646-mu

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Real time counter with separate oscillator
- Four 8-bit PWM channels
- Six PWM channels with programmable resolution from 2 to 16 bits
- Output compare modulator
- 8-channels, 10-bit ADC
- Programmable serial USART
- Master/slave SPI serial interface
- Byte oriented 2-wire serial interface
- Programmable watchdog timer with separate on-chip oscillator
- On-chip analog comparator
- Interrupt and wake-up on pin change
- Special microcontroller features
 - Power-on reset and programmable brown-out detection
 - Internal calibrated oscillator
 - External and internal interrupt sources
 - Six sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and packages
 - 48 programmable I/O lines
 - 64-lead TQFP and 64-lead QFN
- Operating voltages
 - 2.7 5.5V
- Operating temperature
- Industrial (-40°C to +85°C)
- Maximum frequency
 - 8MHz at 2.7V industrial range
 - 16MHz at 4.5V industrial range

2. Overview

The Atmel® AVR® AT90USB64/128 is a low-power CMOS 8-bit microcontroller based on the Atmel® AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90USB64/128 achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

5. Register summary

										_
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	-	-	-	-	-	-	-	-	
(0xFE)	Reserved	-	-	-	-	-	-	-	-	
(0xFD)	Reserved	-	-	-	-	-	-	-	-	
(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(0xFB)	Reserved	-	-	-	-	-	-	-	-	
(0xFA)	Reserved	-	-	-	-	-	-	-	-	
(0xF9)	OTGTCON		PA	AGE				VA	LUE	
(0xF8)	UPINT				PII	NT7:0				
(0xF7)	UPBCHX	-	-	-	-	-		PBYCT10:8		
(0xF6)	UPBCLX		0.00	TEDIA	1	/CT7:0	212	DATADID	DATATO	
(0xF5)	UPERRX	-	COUN	ITER1:0	CRC16	TIMEOUT	PID	DATAPID	DATATGL	
(0xF4)	UEINT	-		-		EPINT6:0	1	DVCT10.0		
(0xF3)	UEBCHX UEBCLX		-	-	- PV	 CT7:0		BYCT10:8		
(0xF2) (0xF1)	UEDATX	<u> </u>				AT7:0				
(0xF0)	UEIENX	FLERRE	NAKINE	-	NAKOUTE	RXSTPE	RXOUTE	STALLEDE	TXINE	
(0xEF)	UESTA1X	-	-	-	-	-	CTRLDIR		RBK1:0	
(0xEE)	UESTAOX	CFGOK	OVERFI	UNDERFI	-		EQ1:0		SYBK1:0	
(0xED)	UECFG1X	ordore	OVENIT	EPSIZE2:0			SK1:0	ALLOC	JI DICT.0	
(0xEC)	UECFG0X	FPTY	YPE1:0	L. C.LLL.U			-	-	EPDIR	
(0xEB)	UECONX		1	STALLRQ	STALLRQC	RSTDT			EPEN	
(0xEA)	UERST					EPRST6:0		1		
(0xE9)	UENUM							EPNUM2:0		
(0xE8)	UEINTX	FIFOCON	NAKINI	RWAL	NAKOUTI	RXSTPI	RXOUTI	STALLEDI	TXINI	
(0xE7)	Reserved			-	-	-	-	-		
(0xE6)	UDMFN				FNCERR					
(0xE5)	UDFNUMH							FNUM10:8		
(0xE4)	UDFNUML				FN	UM7:0				
(0xE3)	UDADDR	ADDEN				UADD6:0				
(0xE2)	UDIEN		UPRSME	EORSME	WAKEUPE	EORSTE	SOFE		SUSPE	
(0xE1)	UDINT		UPRSMI	EORSMI	WAKEUPI	EORSTI	SOFI		SUSPI	
(0xE0)	UDCON						LSM	RMWKUP	DETACH	
(0xDF)	OTGINT			STOI	HNPERRI	ROLEEXI	BCERRI	VBERRI	SRPI	
(0xDE)	OTGIEN			STOE	HNPERRE	ROLEEXE	BCERRE	VBERRE	SRPE	
(0xDD)	OTGCON			HNPREQ	SRPREQ	SRPSEL	VBUSHWC	VBUSREQ	VBUSRQC	
(0xDC)	Reserved									
(0xDB)	Reserved									
(0xDA)	USBINT							IDTI	VBUSTI	
(0xD9)	USBSTA					SPEED		ID	VBUS	
(0xD8)	USBCON	USBE	HOST	FRZCLK	OTGPADE			IDTE	VBUSTE	
(0xD7)	UHWCON	UIMOD	UIDE		UVCONE				UVREGE	
(0xD6)	Reserved		<u> </u>							
(0xD5)	Reserved		<u> </u>		-					
(0xD4)	Reserved									
(0xD3)	Reserved									
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0) (0xCF)	Reserved Reserved	-	-	-	-	-	-	-	-	
(0xCF) (0xCE)	UDR1			-		- Data Register	-	-	-	
(0xCE) (0xCD)	UBRR1H	-	-	-	- USARTTI/C		ISART1 Raud Pot	te Register High E	Byte	
(0xCD) (0xCC)	UBRR1L				JSART1 Baud Ra			io negister might E	5310	
(0xCB)	Reserved	-	-	-	-		-	-	-	
(0xCB)	UCSR1C	- UMSEL11	- UMSEL10	- UPM11	- UPM10	- USBS1	UCSZ11	UCSZ10	UCPOL1	
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	PE1	U2X1	MPCM1	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	Reserved	-	-	-	-	-	-	-	-	
(0xC5)	Reserved	-	-	-	-	-	-	-	-	
(0xC4)	Reserved	-	-	-	-	-	-	-	-	
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	Reserved	-	-	-	-	-	-	-	-	
									-	
(0xC1)	Reserved	-	-	-	-	-	-	-	-	
	Reserved Reserved	-	-	-	-	-	-	-	-	

Address (0xBE) (0xBD) (0xBC) (0xBB) (0xBA) (0xBA) (0xB8) (0xB8) (0xB8) (0xB7) (0xB6)	Name Reserved TWAMR TWCR TWDR	Bit 7 - TWAM6 TWINT	Bit 6 - TWAM5	Bit 5 - TWAM4	Bit 4 - TWAM3	Bit 3 - TWAM2	Bit 2	Bit 1	Bit 0	Page
(0xBD) (0xBC) (0xBB) (0xBA) (0xB9) (0xB9) (0xB8) (0xB7)	TWAMR TWCR TWDR	TWAM6	TWAM5		- TWAM3	-	-		-	
(0xBC) (0xBB) (0xBA) (0xB9) (0xB8) (0xB7)	TWCR TWDR			TWAM4	TWAM3	T14/4140	T14/4844			
(0xBB) (0xBA) (0xB9) (0xB8) (0xB7)	TWDR	TWINT					TWAM1	TWAM0	-	
(0xBA) (0xB9) (0xB8) (0xB7)			TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	
(0xB9) (0xB8) (0xB7)					2-wire Serial Inte	-				
(0xB8) (0xB7)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	
(0xB7)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	
	TWBR				-wire Serial Interfa	ace Bit Rate Reg	Ister			
(UXB6)	Reserved	-	-	-	- TCN2UB	-	- OCR2BUB	- TCR2AUB	-	
(0xB5)	ASSR Reserved	-	EXCLK -	AS2 -		OCR2AUB	- UCR2BUB	-	TCR2BUB	
(0xB3) (0xB4)	OCR2B	-	-		er/Counter2 Outp			-	-	
(0xB3)	OCR2A				ner/Counter2 Outp					
(0xB2)	TCNT2					unter2 (8 Bit)				
(0xB1)	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	
(0xAF)	UPDATX					AT7:0		-		
(0xAE)	UPIENX	FLERRE	NAKEDE	-	PERRE	TXSTPE	TXOUTE	RXSTALLE	RXINE	
(0xAD)	UPCFG2X	ı			INTF	RQ7:0				
(0xAC)	UPSTAX	CFGOK	OVERFI	UNDERFI		DTSI	EQ1:0	NBUS	SYBK1:0	
(0xAB)	UPCFG1X			PSIZE2:0	•	PBI	K1:0	ALLOC		
(0xAA)	UPCFG0X	PTYF	PE1:0	PTOK	EN1:0		PEPI	NUM3:0		
(0xA9)	UPCONX		PFREEZE	INMODE		RSTDT			PEN	
(0xA8)	UPRST					PRST6:0				
(0xA7)	UPNUM							PNUM2:0		
(0xA6)	UPINTX	FIFOCON	NAKEDI	RWAL	PERRI	TXSTPI	TXOUTI	RXSTALLI	RXINI	
(0xA5)	UPINRQX				INF	RQ7:0				
(0xA4)	UHFLEN				FLE	N7:0				
(0xA3)	UHFNUMH							FNUM10:8		
(0xA2)	UHFNUML				FNU	JM7:0				
(0xA1)	UHADDR			i		HADD6:0	1		-	
(0xA0)	UHIEN		HWUPE	HSOFE	RXRSME	RSMEDE	RSTE	DDISCE	DCONNE	
(0x9F)	UHINT		HWUPI	HSOFI	RXRSMI	RSMEDI	RSTI	DDISCI	DCONNI	
(0x9E)	UHCON						RESUME	RESET	SOFEN	
(0x9D)	OCR3CH				unter3 - Output Co		• •			
(0x9C)	OCR3CL				unter3 - Output C					
(0x9B) (0x9A)	OCR3BH OCR3BL				unter3 - Output Counter3 - Output Counter3 - Output Counter	· •	\$,			
(0x9A) (0x99)	OCR36L				unter3 - Output C					
(0x99) (0x98)	OCR3AL				unter3 - Output C					
(0x98) (0x97)	ICR3H				Counter3 - Input C					
(0x96)	ICR3L				Counter3 - Input C					
(0x95)	TCNT3H				er/Counter3 - Cou					
(0x94)	TCNT3L				er/Counter3 - Cou	· ·				
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	TCCR3C	FOC3A	FOC3B	FOC3C	-	-	-	-	-	
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	OCR1CH			Timer/Co	unter1 - Output Co	ompare Register	C High Byte			
(0x8C)	OCR1CL		Timer/Counter1 - Output Compare Register C High Byte Timer/Counter1 - Output Compare Register C Low Byte							
(0x8B)	OCR1BH			Timer/Co	unter1 - Output C	ompare Register	B High Byte			
(0x8A)	OCR1BL			Timer/Co	unter1 - Output C	ompare Register	B Low Byte			
(0x89)	OCR1AH			Timer/Co	unter1 - Output C	ompare Register	A High Byte			
(0x88)	OCR1AL		Timer/Counter1 - Output Compare Register A Low Byte							
(0x87)	ICR1H			Timer/0	Counter1 - Input C	Capture Register	High Byte			
(0x86)	ICR1L				Counter1 - Input (, ,	F			
	TCNT1H				er/Counter1 - Cou					
(0x85)	TCNT1L				er/Counter1 - Cou		-			
(0x84)	Reserved	-	-	-	-	-	-	-	-	
(0x84) (0x83)		FOC1A	FOC1B	FOC1C	-	-	-	-	-	
(0x84) (0x83) (0x82)	TCCR1C									
(0x84) (0x83) (0x82) (0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	
(0x84) (0x83) (0x82) (0x81) (0x80)	TCCR1B TCCR1A	ICNC1 COM1A1	ICES1 COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	
(0x84) (0x83) (0x82) (0x81)	TCCR1B	ICNC1	ICES1							

A dalama a a	N	D:: 7	Dit o	D'4 5	Dit 4	Dit o	Dit o	Dist	Dit o	Dawa
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	
(0x7B)	ADCSRB	ADHSM	ACME	-	-	-	ADTS2	ADTS1	ADTS0	
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
(0x79)	ADCH					egister High byte				
(0x78)	ADCL					egister Low byte	r	T	T	
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	XMCRB	XMBK	-	-	-	-	XMM2	XMM1	XMM0	
(0x74)	XMCRA	SRE	SRL2	SRL1	SRL0	SRW11	SRW10 -	SRW01	SRW00	
(0x73)	Reserved	-	-	-	-	-	-	-	-	
(0x72)	Reserved	-	-		-					
(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3	
(0x70)	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2	
(0x6F)	TIMSK1	-	-	ICIE1		OCIE1C	OCIE1B	OCIE1A	TOIE1	
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	
(0x6D)	Reserved Reserved	-	-	-	-	-	-	-	-	
(0x6C)										
(0x6B) (0x6A)	PCMSK0 EICRB	PCINT7 ISC71	PCINT6 ISC70	PCINT5 ISC61	PCINT4 ISC60	PCINT3 ISC51	PCINT2 ISC50	PCINT1 ISC41	PCINT0 ISC40	
(0x6A) (0x69)	EICRA	ISC31	ISC30	ISC01	ISC80	ISC31	ISC30	ISC41	ISC00	
(0x69) (0x68)	PCICR	-	-	-	-	-	-	-	PCIE0	
(0x68) (0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x67) (0x66)	OSCCAL	-	-	-		ibration Register	-	-	-	
(0x65)	PRR1	PRUSB	-	-		PRTIM3	-		PRUSART1	
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0		PRTIM3	PRSPI		PRADC	
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	_	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
0x3F (0x5F)	SREG	1	T	Н	S	V	N	Z	C	
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	RAMPZ	-	-	-	-	-	-	RAMPZ1	RAMPZ0	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE	
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0+01 (0+51)	OCDR/	OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	
0x31 (0x51)	MONDR		•		Monitor D	ata Register	•	·		
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR				SPI Da	ta Register				
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	
0x2B (0x4B)	GPIOR2				General Purpo	ose I/O Register 2				
0x2A (0x4A)	GPIOR1				General Purpo	ose I/O Register 1				
0x29 (0x49)	PLLCSR	-	-	-	PLLP2	PLLP1	PLLP0	PLLE	PLOCK	
0x28 (0x48)	OCR0B			Tin	ner/Counter0 Out	put Compare Reg	ister B			
0x27 (0x47)	OCR0A			Tin	ner/Counter0 Out		ister A			
0x26 (0x46)	TCNT0				Timer/Co	unter0 (8 Bit)				
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC	
0x22 (0x42)	EEARH	-	-	-	-			s Register High B	yte	
0x21 (0x41)	EEARL				EEPROM Addres	-	yte			
0x20 (0x40)	EEDR					Data Register				
0x1F (0x3F)	EECR	-	-	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	
					Conorol Burno	se I/O Register 0				
0x1E (0x3E)	GPIOR0					-	1			
	GPIOR0 EIMSK EIFR	INT7 INTF7	INT6 INTF6	INT5 INTF5	INT4 INTF4	INT3 INT5	INT2 INTF2	INT1 INTF1	INT0 INTF0	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1B (0x3B)	PCIFR	-	-	-	-	-	-	-	PCIF0	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	
0x18 (0x38)	TIFR3	-	-	ICF3	-	OCF3C	OCF3B	OCF3A	TOV3	
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	
0x16 (0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1	
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The Atmel AT90USB64/128 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$1FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Mnemonics	Operands	nds Description Operation		Flags	#Clocks
SPM		Store Program Memory	(Z) ← R1:R0	None	
IN	Rd, P	In Port	$Rd \leftarrow P$	None 1	
OUT	P, Rr	Out Port	P ← Rr	None 1	
PUSH	Rr	Push Register on Stack	ter on Stack STACK		2
POP	Rd	Pop Register from Stack $Rd \leftarrow STACK$		None	2
	MCU	CONTROL INSTRUCTIONS			
NOP		No Operation		None	1
SLEEP		Sleep (see specific descr. for Sleep function)		None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None 1	
BREAK		Break	For On-chip Debug Only	None N	

7. Ordering information

7.1 Atmel AT90USB646

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB646-AU AT90USB646-MU	Device	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 × 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

7.3 Atmel AT90USB1286

Speed [MHz]	Power supply [V]	Ordering code ⁽²⁾	USB interface	Package (1)	Operating range
16 ⁽³⁾	2.7-5.5	AT90USB1286-AU AT90USB1286-MU	Device	MD PS	Industrial (-40° to +85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

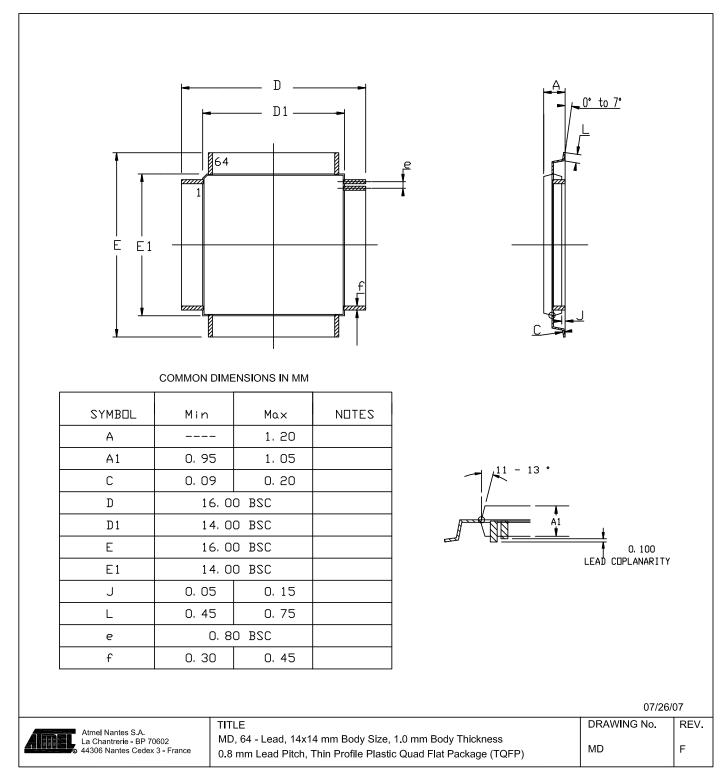
2. Pb-free packaging complies to the European directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully green.

3. See "Maximum speed vs. VCC" on page 392.

MD	64 - lead, 14×14 mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
PS	64 - lead, 9 \times 9mm body size, 0.50mm pitch Quad flat no lead package (QFN)

8. Packaging information

8.1 TQFP64



NOTES: STANDARD NOTES FOR PQFP/VQFP/TQFP/DQFP

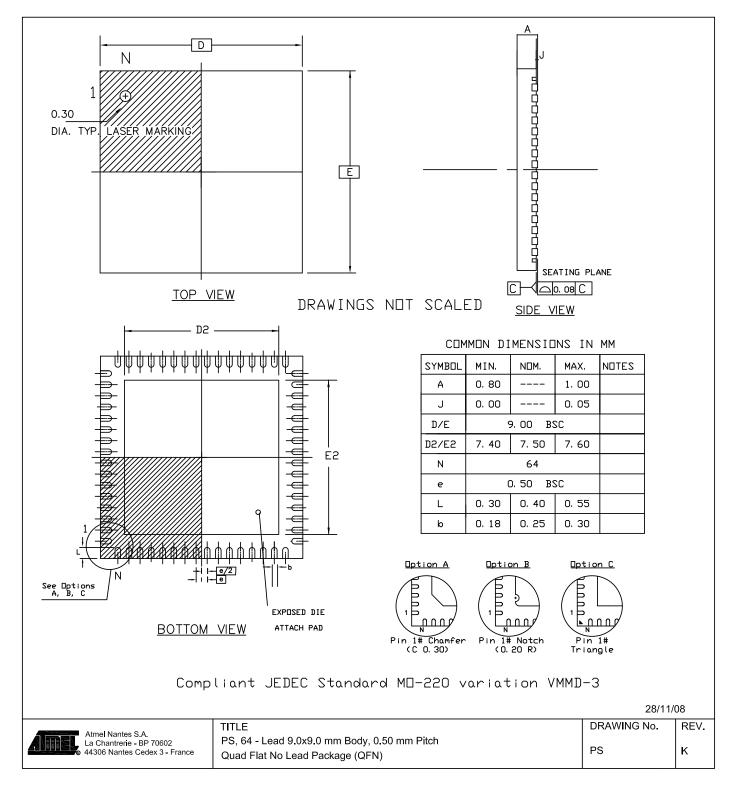
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1982.

2. "D1 AND E1" DIMENSIONS DO NOT INCLUDE MOLD PROTUSIONS MOLD PROTUSIONS SHALL NOT EXCEED 0.25 mm (0.010 INCH) . THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15 mm.

3. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXISTS PLASTIC BODY AT BOTTOM OF PARTING LINE.

4. DATUM "A" AND "D" TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSION "f" DOES NOT INCLUDE DAMBAR PROTUSION ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm/.003" TOTAL EXCESS OF THE "f" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.



NOTES: QFN STANDARD NOTES

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1994.

2. DIMENSION & APPLIES TO METALLIZED TERMINAL AND IS MEASURED

BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION & SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

3. MAX. PACKAGE WARPAGE IS 0.05mm.

4. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

5. PIN #1 ID ON TOP WILL BE LASER MARKED.

6. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220.

7. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.30 mm

8. THE TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER BE EITHER A MOLD OR MARKED FEATURE

not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

6. VBUS session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

5. UBS signal rate

The average USB signal rate may sometime be measured out of the USB specifications $(12MHz \pm 30kHz)$ with short frames. When measured on a long period, the average signal rate value complies with the specifications. This bit rate deviation does not generates communication or functional errors.

Problem fix/workaround

None.

4. VBUS residual level

In USB device and host mode, once a 5V level has been detected to the VBUS pad, a residual level (about 3V) can be measured on the VBUS pin.

Problem fix/workaround

None.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

9.1.3 Atmel AT90USB1287/6 second release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- VBUS Session valid threshold voltage
- Spike on TWI pins when TWI is enabled
- · High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

7. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

6. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

5. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

4. VBUS session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep again it may wake up multiple times.

Problem fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

9.1.5 Atmel AT90USB1287/6 Fourth Release

- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- · Async timer interrupt wake up from sleep generate multiple interrupts

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300μ A extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem fix/workaround

No known workaround, enable Atmel AT90USB64/128 TWI first, before the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem fix/workaround

Before entering sleep, interrupts not used to wake up the part from sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep mode and wakes-up from an asynchronous timer interrupt and then goes back into sleep mode, it may wake up multiple times.

Problem fix/workaround

A software workaround is to wait before performing the sleep instruction: until TCNT2>OCR2+1.

10. Datasheet revision history for Atmel AT90USB64/128

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

10.1 Changes from 7593A to 7593B

- 1. Changed default configuration for fuse bytes and security byte.
- 2. Suppression of timer 4,5 registers which does not exist.
- 3. Updated typical application schematics in USB section

10.2 Changes from 7593B to 7593C

1. Update to package drawings, MQFP64 and TQFP64.

10.3 Changes from 7593C to 7593D

 For further product compatibility, changed USB PLL possible prescaler configurations. Only 8MHz and 16MHz crystal frequencies allows USB operation (see Table 7-11 on page 50).

10.4 Changes from 7593D to 7593E

- 1. Updated PLL Prescaler table: configuration words are different between AT90USB64x and AT90USB128x to enable the PLL with a 16MHz source.
- 2. Cleaned up some bits from USB registers, and updated information about OTG timers, remote wake-up, reset and connection timings.
- 3. Updated clock distribution tree diagram (USB prescaler source and configuration register).
- 4. Cleaned up register summary.
- 5. Suppressed PCINT23:8 that do not exist from External Interrupts.
- 6. Updated Electrical Characteristics.
- 7. Added Typical Characteristics.
- 8. Update Errata section.

10.5 Changes from 7593E to 7593F

- 1. Removed 'Preliminary' from document status.
- 2. Clarification in Stand by mode regarding USB.

10.6 Changes from 7593F to 7593G

1. Updated Errata section.

10.7 Changes from 7593G to 7593H

- 1. Added Signature information for 64K devices.
- 2. Fixed figure for typical bus powered application
- 3. Added min/max values for BOD levels
- 4. Added ATmega32U6 product
- 5. Update Errata section
- 6. Modified descriptions for HWUPE and WAKEUPE interrupts enable (these interrupts should be enabled only to wake up the CPU core from power down mode).

10.8 Changes from 7593H to 7593I

1. Updated Table 9-2 in "Brown-out detection" on page 60. Unused BOD levels removed.

10.9 Changes from 7593I to 7593J

- 1. Updated Table 9-2 in "Brown-out detection" on page 60. BOD level 100 removed.
- 2. Updated "Ordering information" on page 18.
- 3. Removed ATmega32U6 errata section.

10.10 Changes from 7593J to 7593K

- 1. Corrected Figure 6-7 on page 34, Figure 6-8 on page 34 and Figure 6-9 on page 35.
- Corrected ordering information for Section 7.3 "Atmel AT90USB1286" on page 20, Section 7.4 "Atmel AT90USB1287" on page 21 and Section 7.2 "Atmel AT90USB647" on page 19.
- 3. Removed the ATmega32U6 device and updated the datasheet accordingly.
- 4. Updated Assembly Code Example in "Watchdog reset" on page 61.

10.11 Changes from 7593K to 7593L

- 1. Updated the "Ordering information" on page 18. Changed the speed from 20MHz to 16MHz.
- 2. Replaced ATmegaAT90USBxxxx by AT90USBxxxx through the datasheet.
- 3. Updated the first paragraph of "Overview" on page 307. Port A replaced by Port F.
- 4. Updated ADC equation in "ADC conversion result" on page 318. The equation has 1024 instead of 1023.
- 5. Created "Packaging Information" chapter.
- 6. Replaced the "QFN64" Packaging by an updated QFN64 Packaging drawing.
- 7. Updated "Errata" on page 26. AT90USB1286/7 has a fourth release, while AT90USB646/7 updated with a second release.
- 8. In Section "Overview" on page 307, "Port A" has been replaced by "Port F" in the first section.
- 9. In Section "Atmel AT90USB647" on page 19 the USB interface has been changed to USB OTG.
- 10. In Section "Atmel AT90USB1286" on page 20 the USB interface has been changed to Device.
- 11. In Section "Atmel AT90USB1287" on page 21 the USB interface has been changed to Host OTG.
- 12. General update according to new template.

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