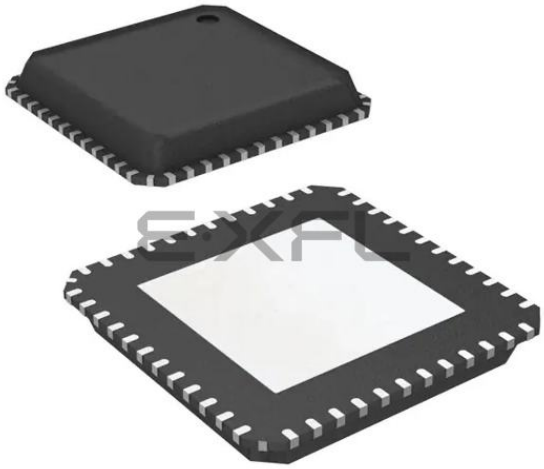
Infineon Technologies - XC2321D20F66VAAKXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2321d20f66vaakxuma1

Table of Contents

- On-Chip Peripheral Modules
  - Synchronizable 12-bit A/D Converter with up to 10 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 4 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 32 message objects (Full CAN/Basic CAN) on 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable window watchdog timer and oscillator watchdog
- Up to 33 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP), Single-Pin DAP (SPD) or JTAG interface
- 48-pin Green VQFN package, 0.5 mm (10.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range[1]:
  - SAF-…: -40°C to 85°C
  - SAH-…: -40°C to 110°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XC232[01]D please contact your sales representative or local distributor.

This document describes several derivatives of the XC232[01]D group:

Basic Device Types are readily available and
Special Device Types are only available on request.

1) Not all derivatives are offered in all temperature ranges.

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P5.4	I	In/B	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/B	**Analog Input Channel 4 for ADC0**
	CCU63_T12HRB	I	In/B	**External Run Control Input for T12 of CCU63**
	T3EUDA	I	In/B	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/B	**JTAG Test Mode Selection Input**
14	P5.8	I	In/B	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/B	**Analog Input Channel 8 for ADC0**
	CCU6x_T12HRC	I	In/B	**External Run Control Input for T12 of CCU60/3**
	CCU6x_T13HRC	I	In/B	**External Run Control Input for T13 of CCU60/3**
15	P5.9	I	In/B	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/B	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/B	**CAPCOM2 Timer T7 Count Input**
16	P2.0	O0 / I	DA/B	**Bit 0 of Port 2, General Purpose Input/Output**
	CCU63_CC60	O2	DA/B	**CCU63 Channel 0 Output**
	RxDC0C	I	DA/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	DA/B	**CCU63 Channel 0 Input**
	ADC0_CH19	I	DA/B	**Analog Input Channel 19 for ADC0**
	T5INB	I	DA/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
23	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
24	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	ESR1_10	I	St/B	**ESR1 Trigger Input 10**
25	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
38	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	CCU63_COUT61	O3	St/B	**CCU63 Channel 1 Output**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCPOS0A	I	St/B	**CCU60 Position Input 0**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
39	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U1C0_SCLKOUT	O3	St/B	**USIC1 Channel 0 Shift Clock Output**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	ESR2_11	I	St/B	**ESR2 Trigger Input 11**

3.5 Interrupt System

The architecture of the XC232[01]D supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC232[01]D has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC232[01]D can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 64 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC232[01]D provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service

1) Depending if the jump cache is used or not.

3.8 Capture/Compare Units CCU6x

The XC232[01]D types feature the CCU60 and CCU63 units.

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

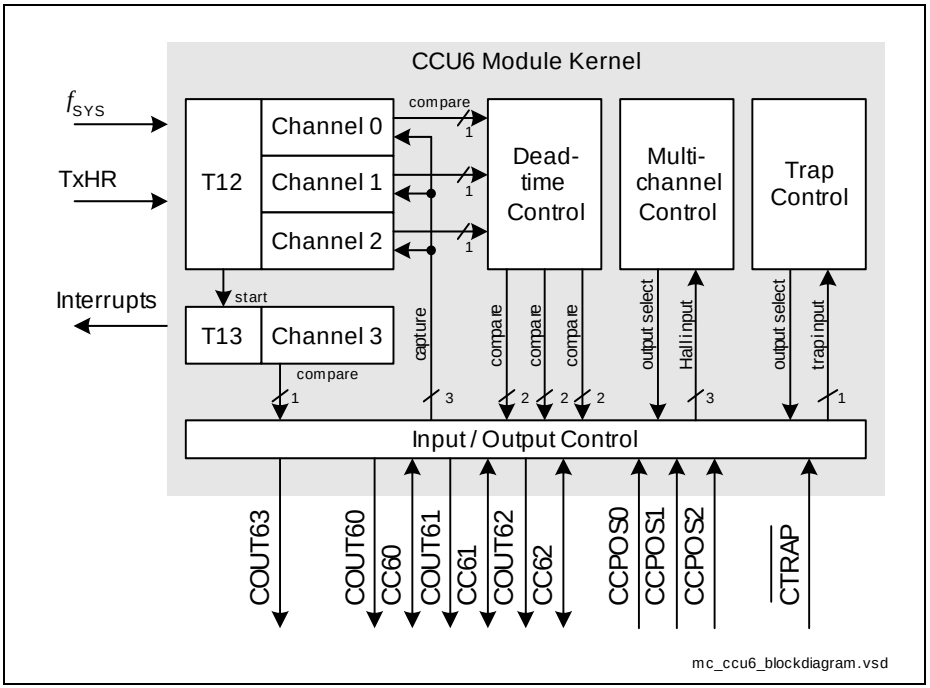


Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.12 Universal Serial Interface Channel Modules (USIC)

The XC232[01]D features the USIC modules USIC0 and USIC1. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

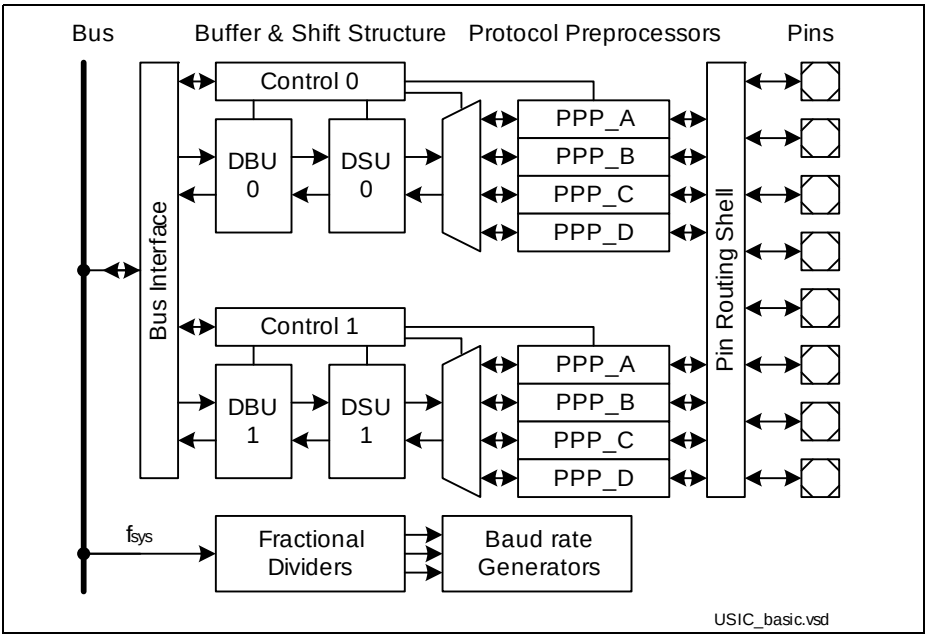


Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - module capability: maximum baud rate = f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - module capability: maximum baud rate = f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  - module capability: maximum baud rate = f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - module capability: maximum baud rate = f_{SYS} / 2

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

8) Value is controlled by on-chip regulator.

4.2 Voltage Range definitions

The XC232[01]D timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5.0	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC232[01]D and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC232[01]D provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC232[01]D.

Table 17 DC Characteristics for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	
Output High voltage[6]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$ [7]
Output Low Voltage[6]	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$ [8]
		–	–	1.0	V	$I_{OL} \leq I_{OLmax}$

1) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

2) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

3) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): I_{OZ} = $I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

4) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.

5) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.

6) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

7) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.

8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

4.3.3 Power Consumption

The power consumed by the XC232[01]D depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in most parts of domain DMP_M stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Note: Operating Conditions apply.

Table 23 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.825\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.625\ \mu s$

Conversion 8-bit:

$t_{C8} = 10 \times t_{ADCI} + 2 \times t_{SYS} = 10 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.525\ \mu s$

Converter Timing Example B:

Assumptions: f_{SYS} = 66 MHz (i.e. t_{SYS} = 15.2 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 16.5 MHz, i.e. t_{ADCI} = 60.6 ns
Sample time t_S = $t_{ADCI} \times 2$ = 121.2 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 1.0\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 0.758\ \mu s$

4.6 Flash Memory Parameters

The XC232[01]D is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC232[01]D's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	2[1)]		$N_{FL\_RD} \leq 1$
		–	–	1[2)]		$N_{FL\_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq$ 20 years
Flash wait states[3)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq$ 8 MHz
		2	–	–		$f_{SYS} \leq$ 13 MHz
		3	–	–		$f_{SYS} \leq$ 17 MHz
		4	–	–		$f_{SYS} >$ 17 MHz
Erase time per sector/page	t_{ER} CC	–	7[4)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[4)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{ER} \leq$ 1,000 cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

Table 31 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	0.8	mA	Driver_Strength = Medium
		–	–	1.0	mA	Driver_Strength = Strong
		–	–	0.15	mA	Driver_Strength = Weak
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	73 + 0.85 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	6 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	33 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	385 + 3.25 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 25 mA.

Table 33 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= lower

Table 33 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 10[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 9[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-7	–	11	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 34 is valid under the following conditions: C_L= 20 pF; *SSC*= slave ; voltage_range= upper

Table 34 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	

4.7.6 Debug Interface Timing

The debugger can communicate with the XC232[01]D via 1-pin SPD interface, via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 36 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 36 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	100[1)]	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	92	95	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

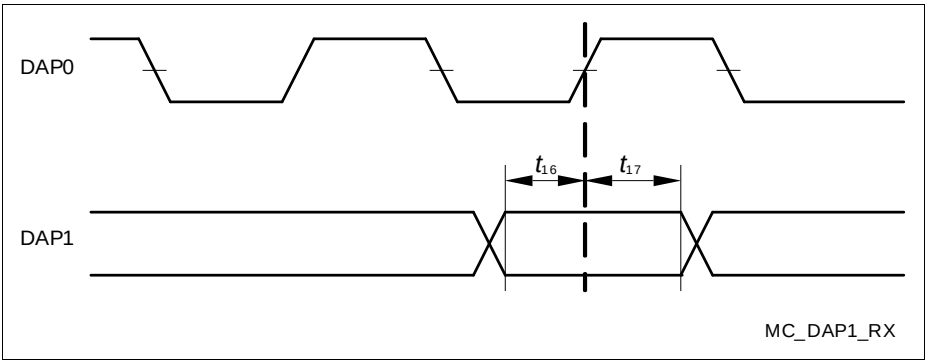


Figure 23 DAP Timing Host to Device

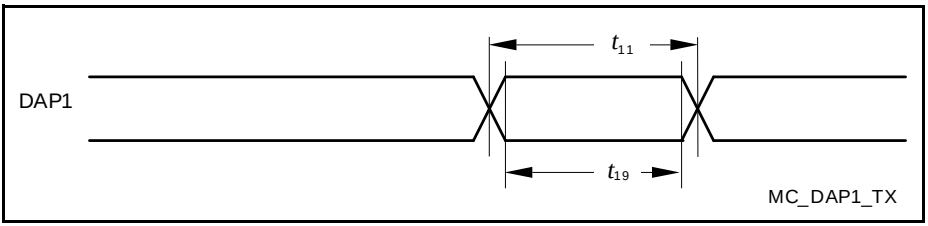


Figure 24 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.

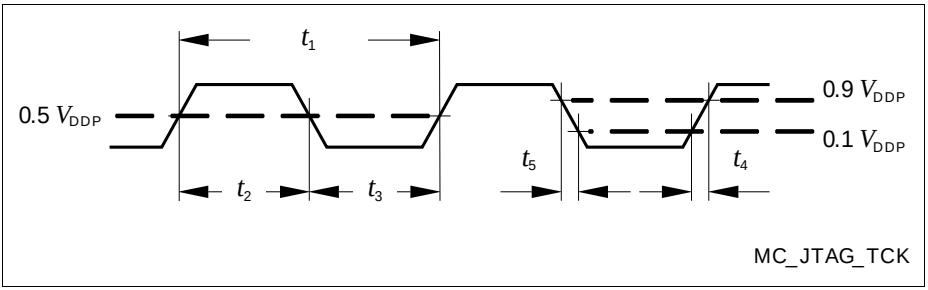


Figure 25 Test Clock Timing (TCK)

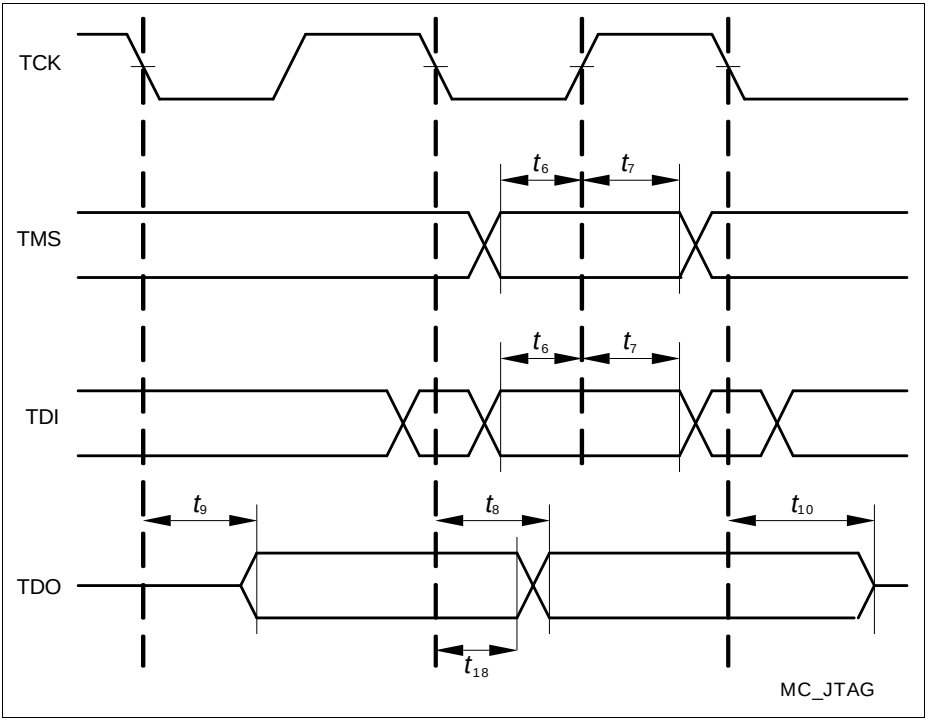


Figure 26 JTAG Timing