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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe002hz010ec00tr

PIN DESCRIPTION

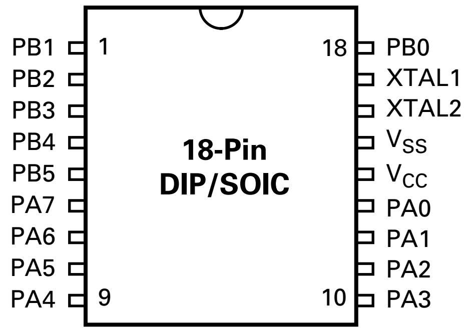


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

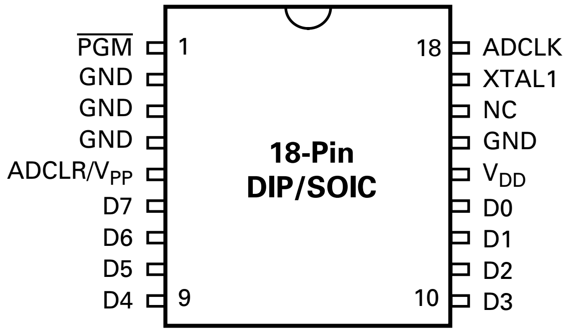


Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1-MHz Clock	Input
18	ADCLK	Address Clock	Input

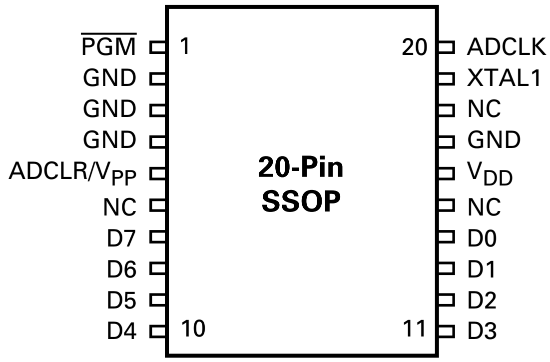


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Table 4. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1-MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on PB5 Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		40	mA	3
Maximum Allowable Current into V_{DD}		40	mA	3
Maximum Allowable Current into an Input Pin	–600	+600	µA	4
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	5
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	3
Maximum Allowable Output Current Sourced by Port A		40	mA	3
Maximum Allowable Output Current Sunk by Port B		40	mA	3
Maximum Allowable Output Current Sourced by Port B		40	mA	3

Notes:
1. Applies to all pins except the PB5 pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Peak Current. Do not exceed 25mA average current in either direction.
4. Excludes XTAL pins.
5. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

DC ELECTRICAL CHARACTERISTICS

Table 5. DC Electrical Characteristics

			T_A = 0ºC to +70ºC Standard Temperatures					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical[2] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	$0.7V_{CC}$	$V_{CC}+0.3$	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	$V_{SS}–0.3$	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	$V_{SS}–0.3$	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	$0.7V_{CC}$	$V_{CC}+0.3$	1.3	V		
		5.5V	$0.7V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.0V	$V_{SS}–0.3$	$0.2V_{CC}$	0.7	V		
		5.5V	$V_{SS}–0.3$	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.0V	$V_{CC}–0.4$		3.1	V	I_{OH} = –2.0 mA	
		5.5V	$V_{CC}–0.4$		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	3.0V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	3.0V	$V_{SS}–0.3$	$V_{CC}–1.0$		V		3
		5.5V	$V_{SS}–0.3$	$V_{CC}–1.0$		V		3
R_{PB5}	PB5 Pull-up Resistor	3.0V	100		200	kOhm		4
		5.5V	100		200			
V_{LV}	V_{CC} Low-Voltage Protection		2.45	2.85	2.60	V		

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 5. DC Electrical Characteristics (Continued)

			T_A = 0ºC to +70ºC Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	5,6
		5.5V		6.0	3.5	mA	@ 10 MHz	5,6
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current			500	150	nA	STOP mode V_{IN} = 0V, V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 6. DC Electrical Characteristics (Continued)

			T_A = –40ºC to +105ºC Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7
		5.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

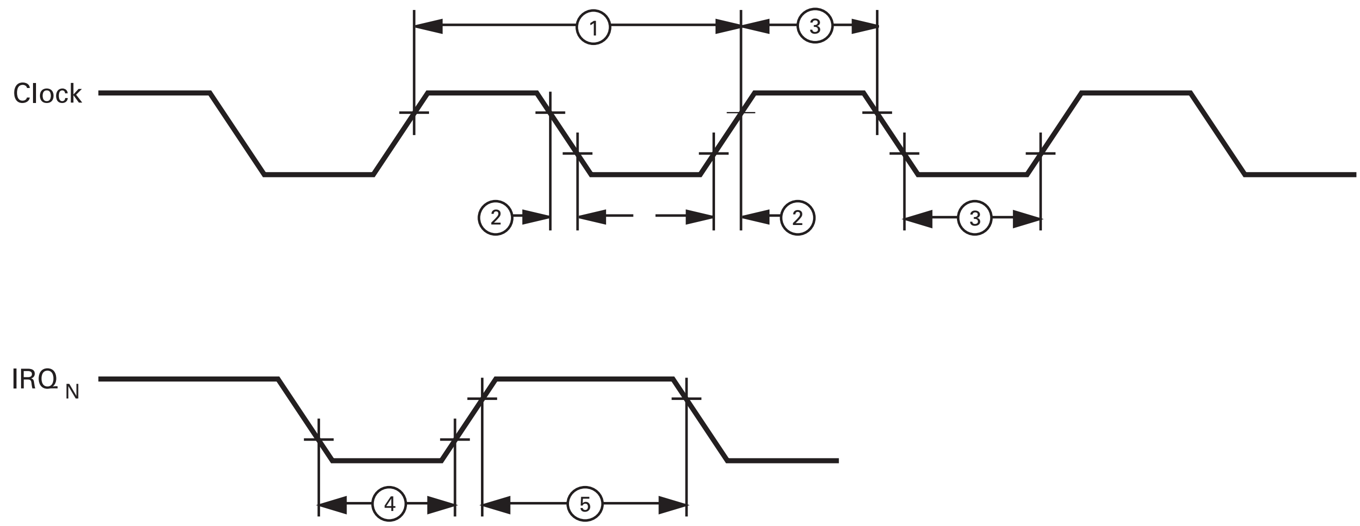


Figure 8. AC Electrical Timing Diagram

Table 7. Additional Timing

No	Symbol	Parameter	V_{CC}[1]	Min	Max	Units	Notes
				T_A = 0ºC to +70ºC T_A = –40ºC to +105ºC @ 10 MHz			
1	T_PC	Input Clock Period	3.0V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.0V		15	ns	2
			5.5V		15	ns	2
3	T_WC	Input Clock Width	3.0V	50		ns	2
			5.5V	50		ns	2
4	T_WIL	Int. Request Input Low Time	3.0V	70		ns	2
			5.5V	70		ns	2
5	T_WIH	Int. Request Input High Time	3.0V	5TpC			2
			5.5V	5TpC			2
6	T_{WSM}	STOP mode Recovery Width Spec.	3.0V	25		ns	
			5.5V	25		ns	
7	T_{OST}	Oscillator Start-Up Time	3.0V		5TpC		
			5.5V		5TpC		
8	T_{POR}	Power-On Reset Time	3.0V	128 T_PC + T_{OST}			
			5.5V				

Notes:
1. The V_{DD} voltage specification of 3.0V guarantees 3.0V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logical 1 and 0.2 V_{CC} for a logical 0.

IREQ SOFTWARE INTERRUPT GENERATION

IREQ can be used to generate software interrupts by specifying IREQ as the destination of any instruction referencing the Z8Plus Standard Register File. These software interrupts (SWI) are controlled in the same manner as hardware generated requests. In other words, the IMASK controls the enabling of each SWI.

To generate a SWI, the request bit in IREQ is set by the following statement:

```
OR IREQ,#NUMBER
```

The immediate data variable, NUMBER, has a `1` in the bit position corresponding to the required level of SWI. For example, an SWI must be issued when an IREQ5 occurs. Bit `5` of NUMBER must have a value of `1`.

```
OR IREQ, #00100000B
```

If the interrupt system is globally enabled, IREQ5 is enabled, and there are no higher priority requests pending, control is transferred to the service routine pointed to by the IREQ5 vector.

Note: Software may modify the IREQ register at any time. Care should be taken when using any instruction that modifies the IREQ register while interrupt sources are active. The software writeback always takes precedence over the hardware. If a software writeback takes place on the same cycle as an interrupt source tries to set an IREQ bit, the new interrupt is lost.

Nesting of Vectored Interrupts

Nesting vectored interrupts allows higher priority requests to interrupt a lower priority request. To initiate vectored interrupt nesting, perform the following steps during the interrupt service routine:

- PUSH the old IMASK on the stack
- Load IMASK with a new mask to disable lower priority interrupts
- Execute an EI instruction
- Proceed with interrupt processing
- Execute a DI instruction after processing is complete
- Restore the IMASK to its original value by POPing the previous mask from the stack
- Execute IRET

Depending on the application, some simplification of the above procedure may be possible.

RESET Conditions

The IMASK and IREQ registers initialize to `00h` on RESET.

PROGRAMMABLE OPTIONS

EPROM Protect. When selecting the DISABLE EPROM PROTECT/ENABLE TESTMODE option, the user can read the software code in the program memory. ZiLOG's internal factory test mode, or any of the standard test mode methods, are useful for reading or verifying the code in the microcontroller when using an EPROM programmer. If the user should select the ENABLE EPROM PROTECT/DISABLE TESTMODE option, it is not possible to read the code using a tester, programmer, or any other standard method. As a result, ZiLOG is unable to test the EPROM memory at any time after customer delivery.

This option bit only affects the user's ability to read the code and has no effect on the operation of the part in an application. ZiLOG tests the EPROM memory before customer delivery whether or not the ENABLE EPROM PROTECT/DISABLE TESTMODE option is selected; ZiLOG provides a standard warranty for the part.

System Clock Source. When selecting the RC OSCILLATOR ENABLE option, the oscillator circuit on the microcontroller is configured to work with an external RC circuit. When selecting the Crystal/Other Clock Source option, the oscillator circuit is configured to work with an external crystal, ceramic resonator, or LC oscillator.

WATCH-DOG TIMER

The Watch-Dog Timer (WDT) is a retriggerable one-shot 16-bit timer that resets the device if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer time-out periods required in applications, the watch-dog timer is only updated every 64th clock cycle. When operating in the RUN or HALT modes, a WDT time-out reset is functionally equivalent to an interrupt vectoring the PC to 0020H, and setting the WDT flag to 1. Coming out of RESET, the WDT is fully enabled with its time-out value set at minimum, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2h and C3h) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after RESET and when the device enters STOP mode.

The WDT instruction should be executed often enough to provide some margin of time to allow the WDT registers to approach 0. Because the WDT time-out periods are relatively long, a WDT RESET occurs in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

RESET clears both the WDT and SMR flags. A WDT time-out sets the WDT flag, and the STOP instruction sets the SMR flag. This function enables software to determine whether a WDT time-out or a return from STOP mode occurred. Reading the WDT and SMR flags does not reset the flag to 0; therefore, the user must clear the flag via software.

Note: Failure to clear the SMR flag can result in unexpected behavior.

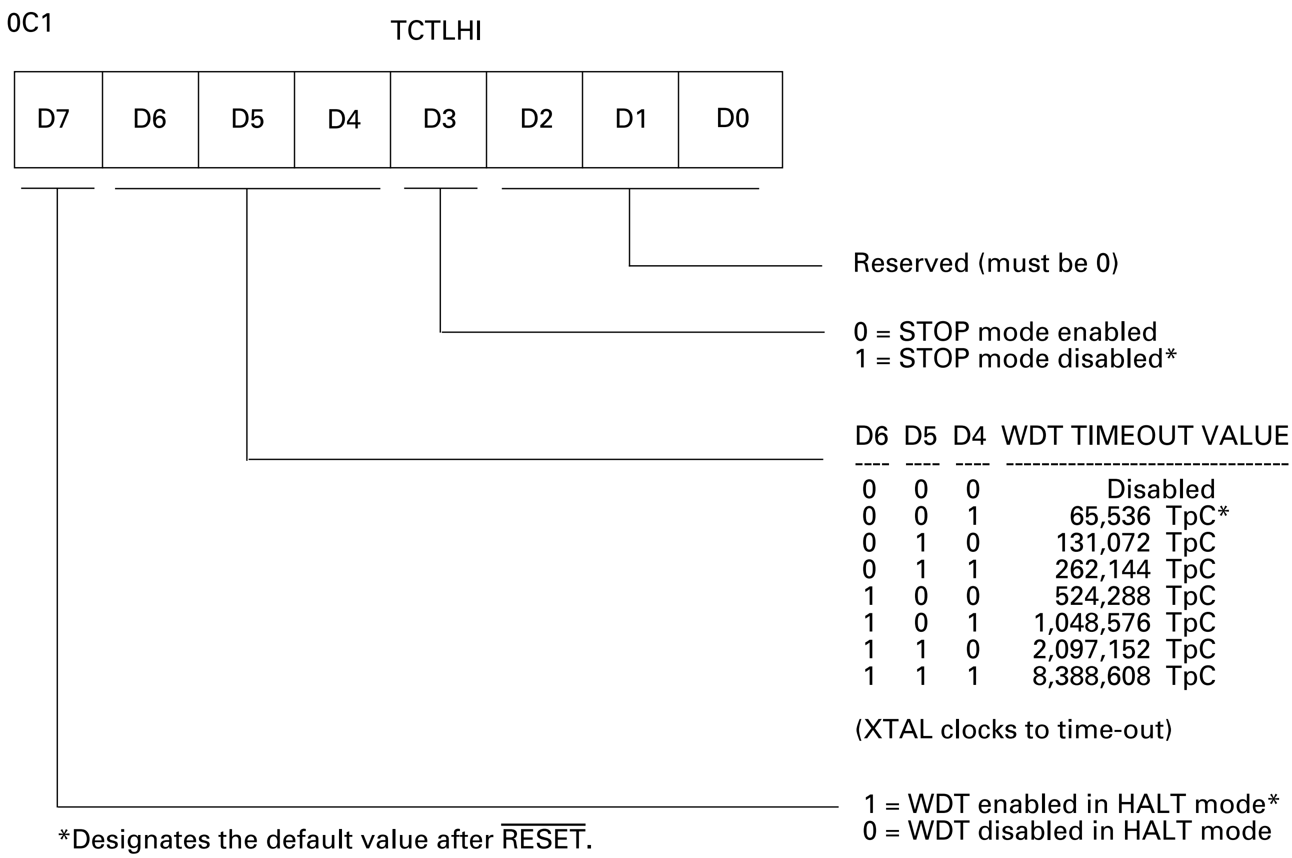


Figure 11. TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of the RESET performs this function. Logic within the device detects that it is in the process of executing the first instruction after the processor leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 13 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are 001, which sets the WDT to its minimum time-out period when coming out of RESET.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT mode. A 0 prevents the WDT from resetting the part while halted. Coming out of RESET, the WDT is enabled during HALT mode.

STOP MODE (D3). Coming out of RESET, the device STOP mode is disabled. If an application requires use of STOP mode, bit D3 must be cleared immediately at leaving RESET. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters STOP mode.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 13. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10-MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	8,388,608 TpC	838.86 ms

Note: *TpC is an XTAL clock cycle. The default at reset is 001.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8Plus MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter HALT mode, the device only requires a HALT instruction. It is *not* necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT       ; enter HALT mode
```

HALT mode can be exited by servicing an external or internal interrupt. The first instruction executed is the interrupt service routine. At completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT mode can also be exited via a RESET activation or a Watch-Dog Timer (WDT) time-out. In these cases, program execution restarts at 0020H, the reset restart address.

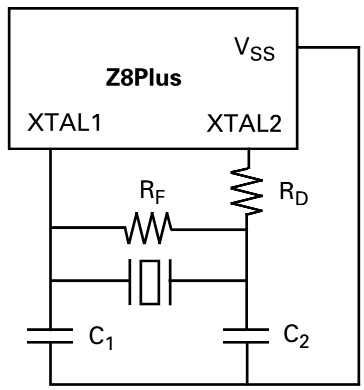


Figure 16. Crystal/Ceramic Resonator Oscillator

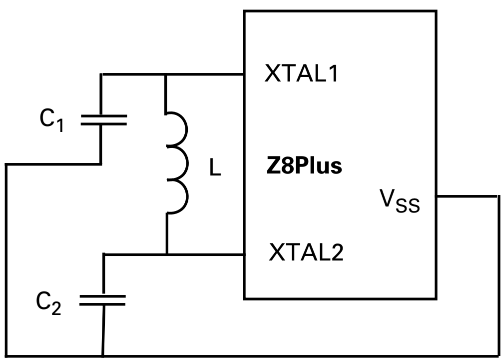


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

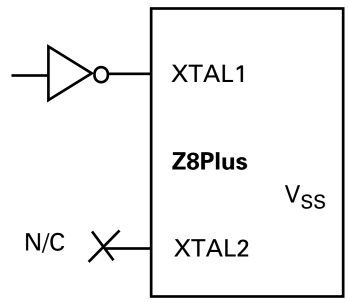


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8Plus oscillator can use an inductor capacitor oscillator (LC) network to generate an XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$1/C_T = 1/C_1 + 1/C_2$$
$$\text{If } C_1 = C_2$$
$$1/C_T = 2/C_1$$
$$C_1 = 2C_T$$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 µH is displayed as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi [27\ (10^{-6})\ C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pF}$$

Thus, C_1 = 55.2 pF and C_2 = 55.2 pF.

TIMERS

Two 8-bit timers, timer 0 (T0) and timer 1 (T1) are available to function as a pair of independent 8-bit standard timers. They may also be cascaded to function as a 16-bit Pulse-Width Modulator (PWM) timer. Two additional 8-bit timers (T2 and T3) are provided, but they can only operate as one 16-bit standard timer.

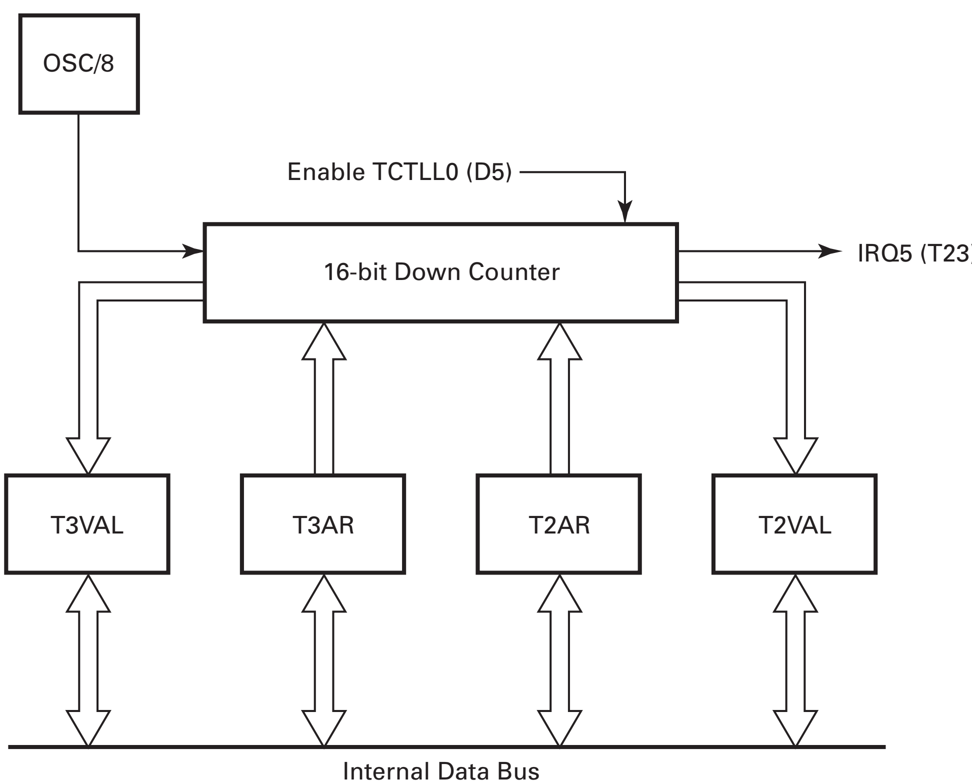


Figure 19. 16-Bit Standard Timer

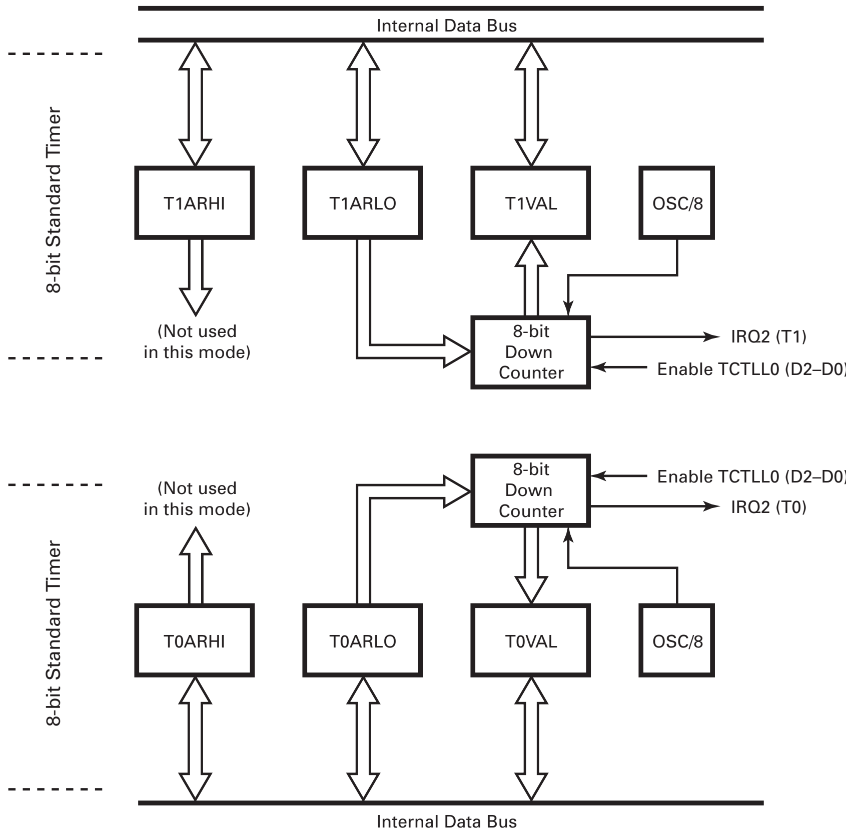


Figure 20. 8-Bit Standard Timers

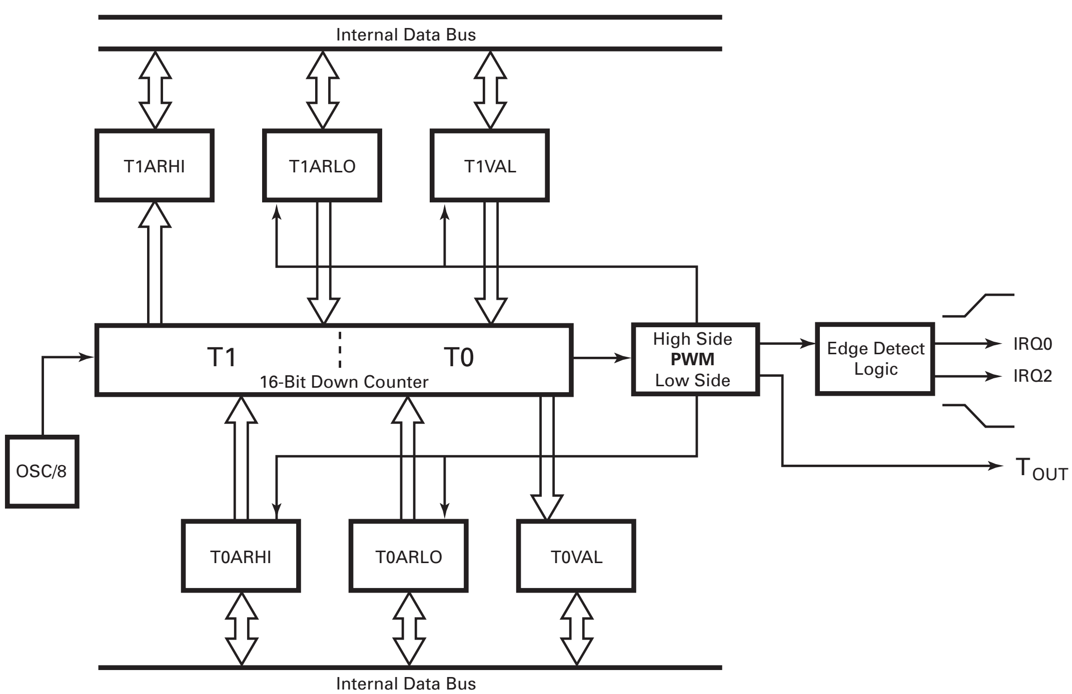


Figure 21. 16-Bit Standard PWM Timer

TIMERS (Continued)

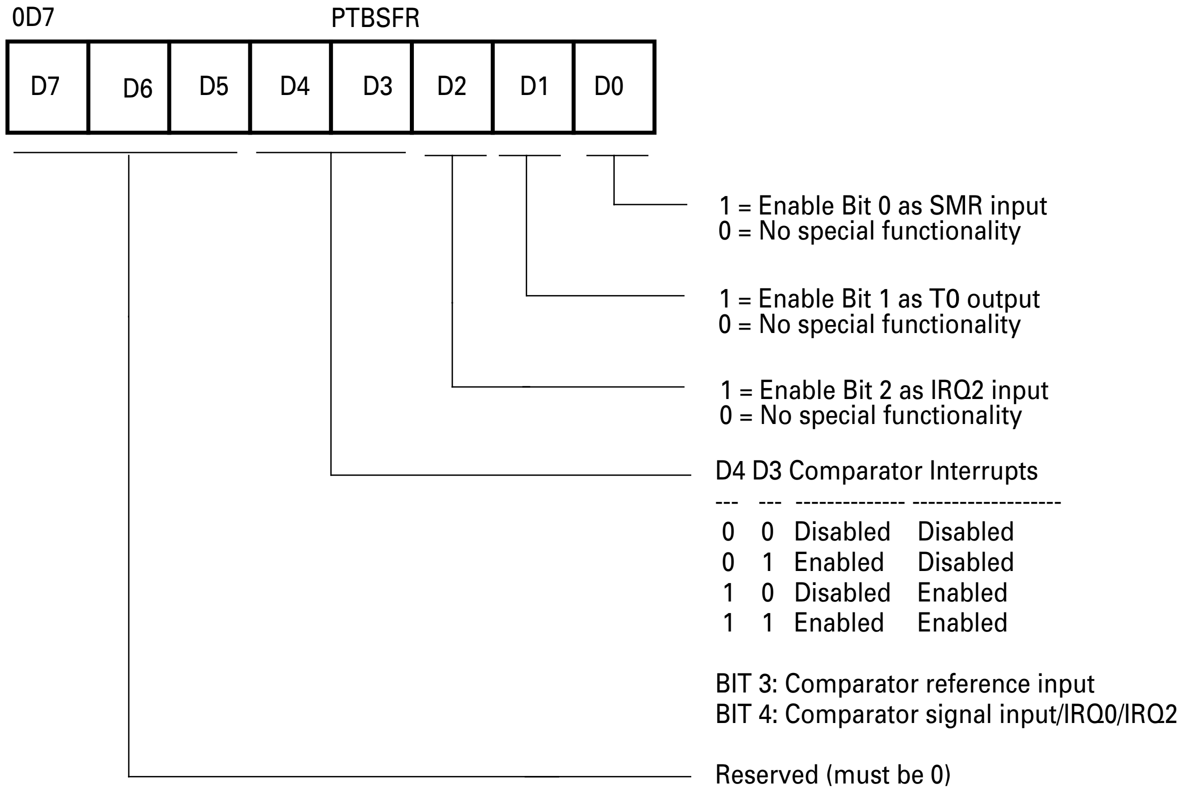


Figure 23. PortB Special Function Register

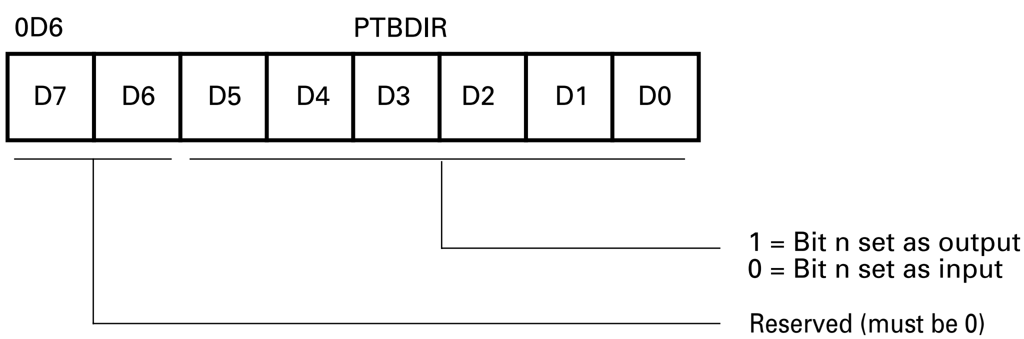


Figure 24. Port B Directional Control Register

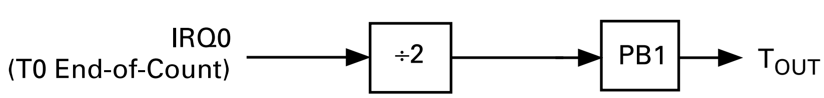


Figure 25. Timer T0 Output Through T_{OUT}

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

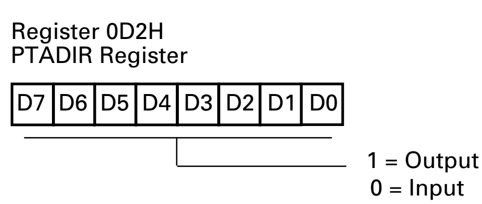


Figure 27. Port A Directional Control Register

PORT B—PIN 0 CONFIGURATION

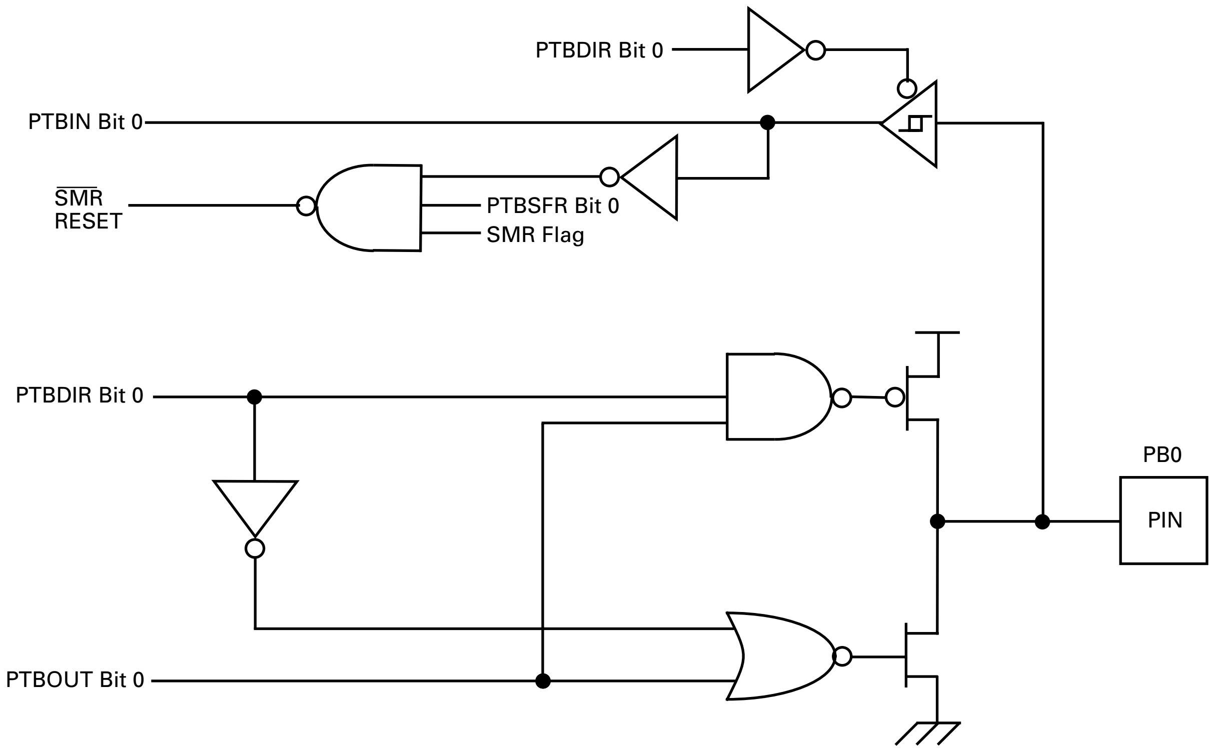
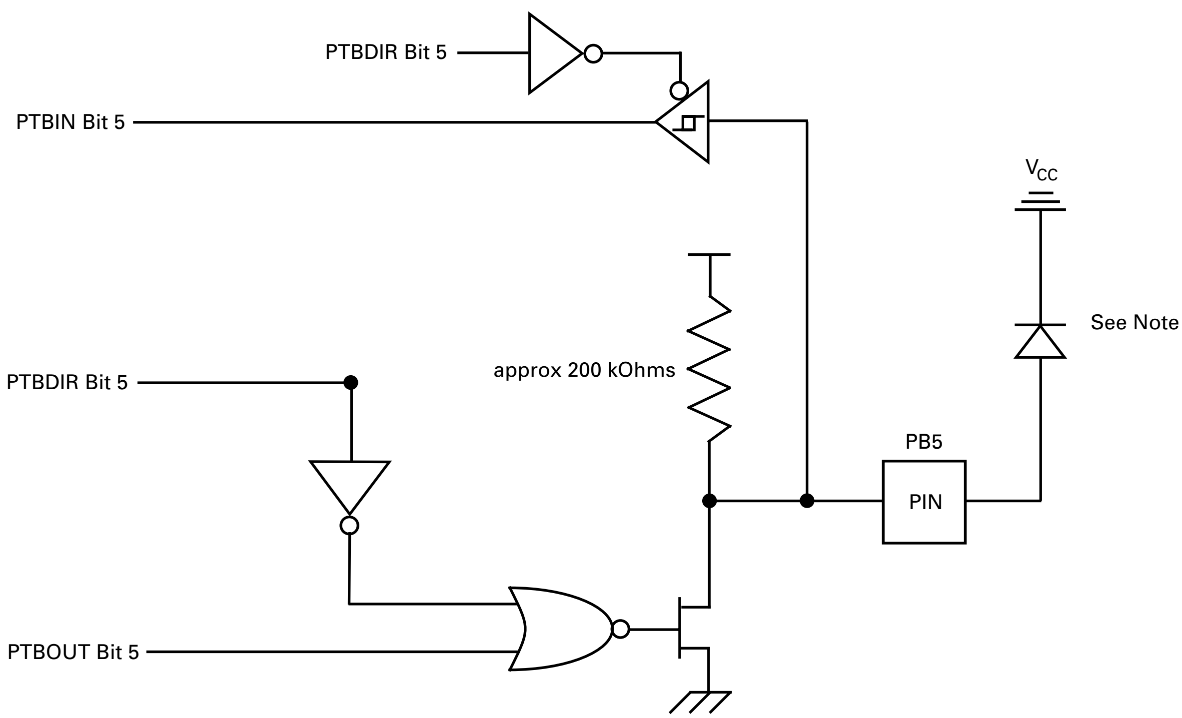


Figure 33. Port B Pin 0 Diagram



Note: There is no high-side protection device. The user should always place an external protection diode as shown.

Figure 34. Port B Pin 5 Diagram

PORT B CONTROL REGISTERS (Continued)

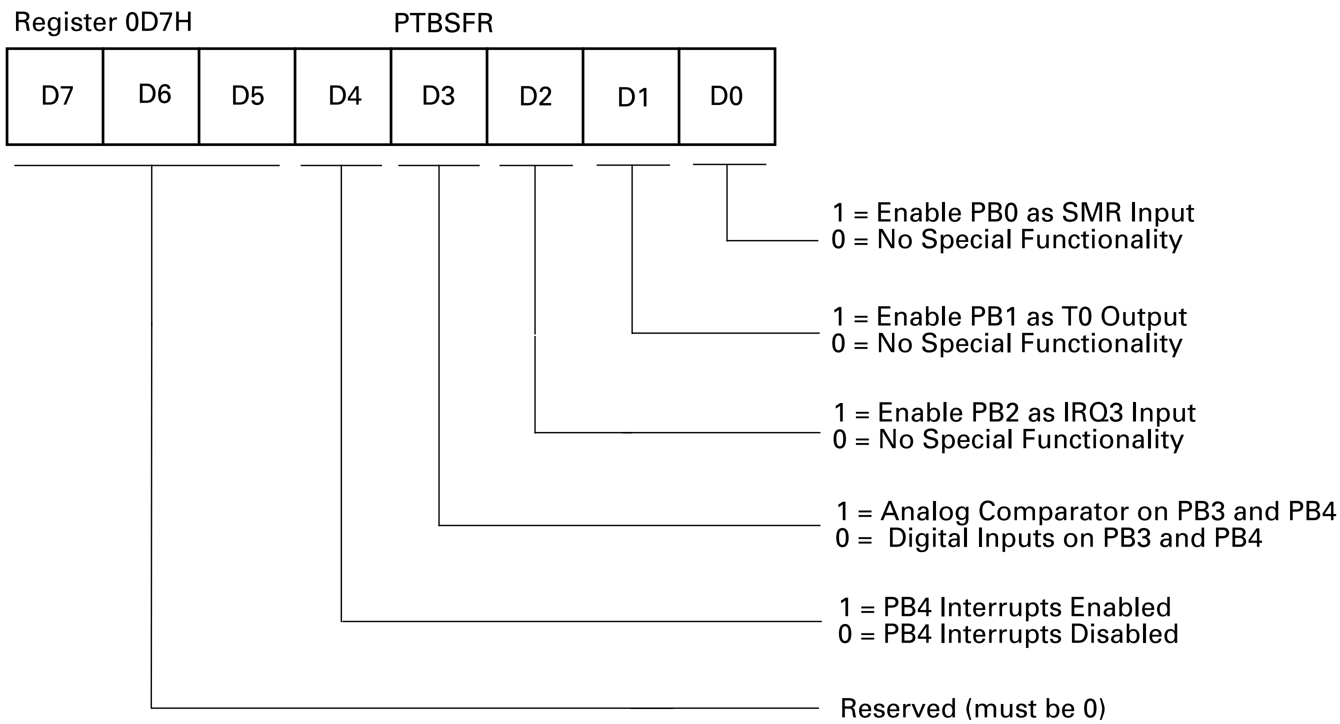


Figure 41. Port B Special Function Register

COMPARATOR OPERATION (Continued)

age Protection trip point (V_{LV}) is reached. The actual Low-Voltage Protection trip point is a function of process parameters.

Low-Voltage Protection is active in RUN and HALT modes only, but is disabled in STOP mode (Figure 42).

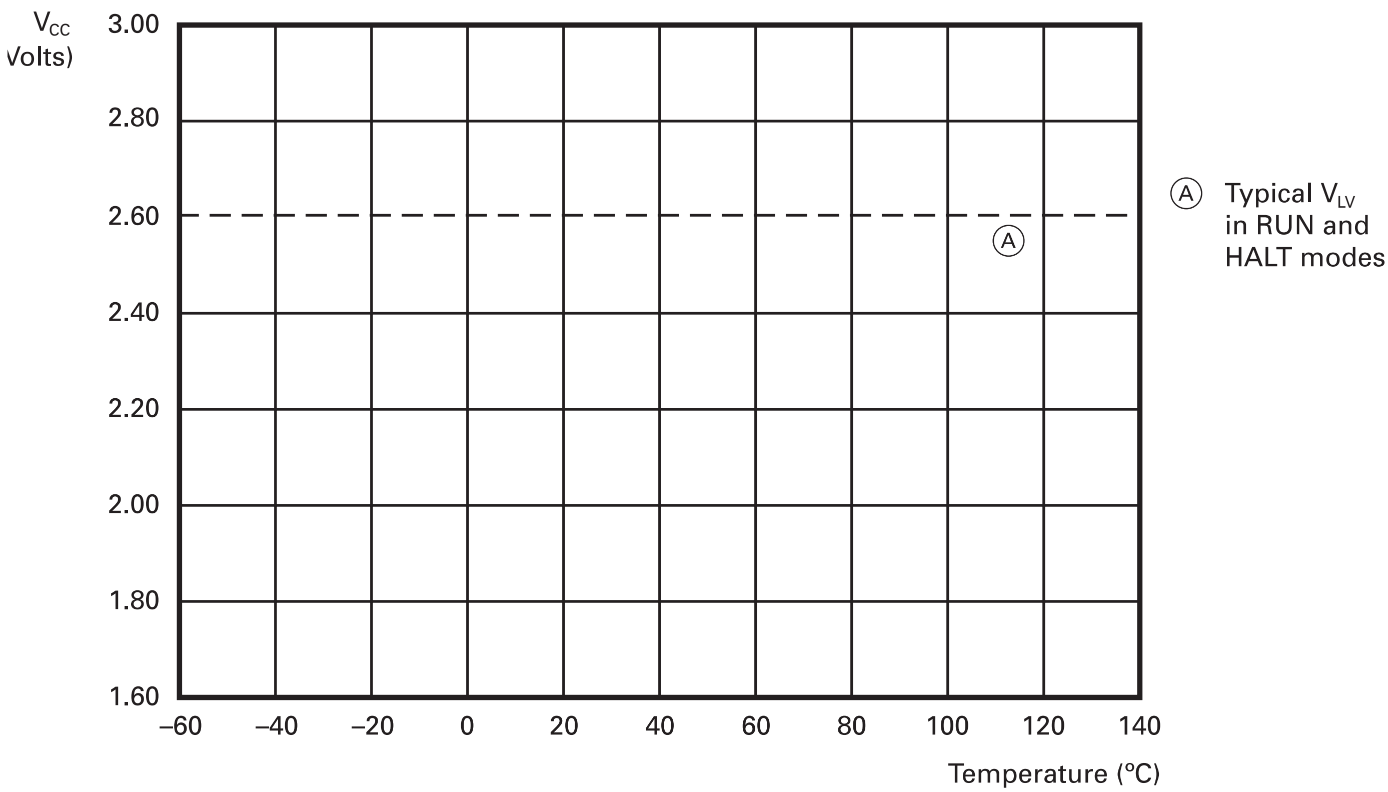
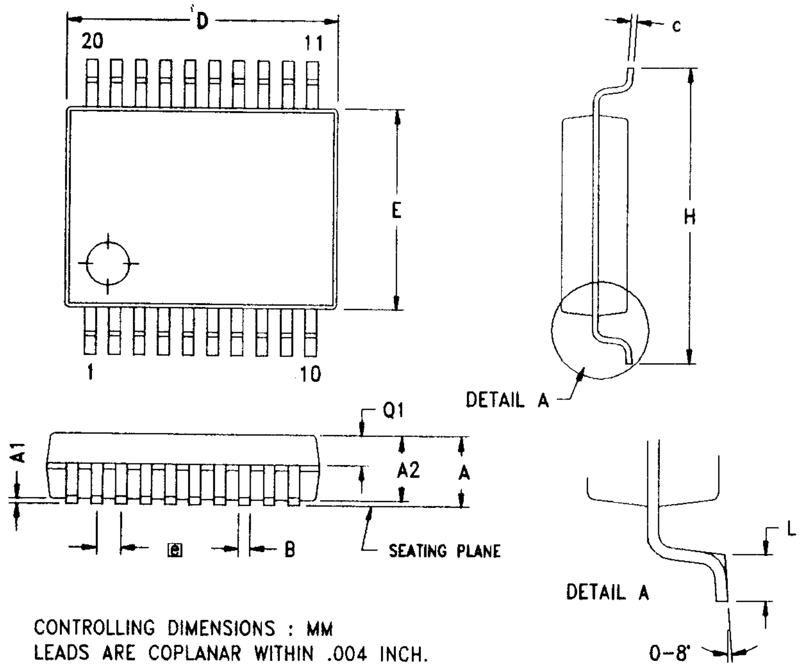


Figure 42. Voltage vs. Temperature



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram