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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe002hz010sc

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low; and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

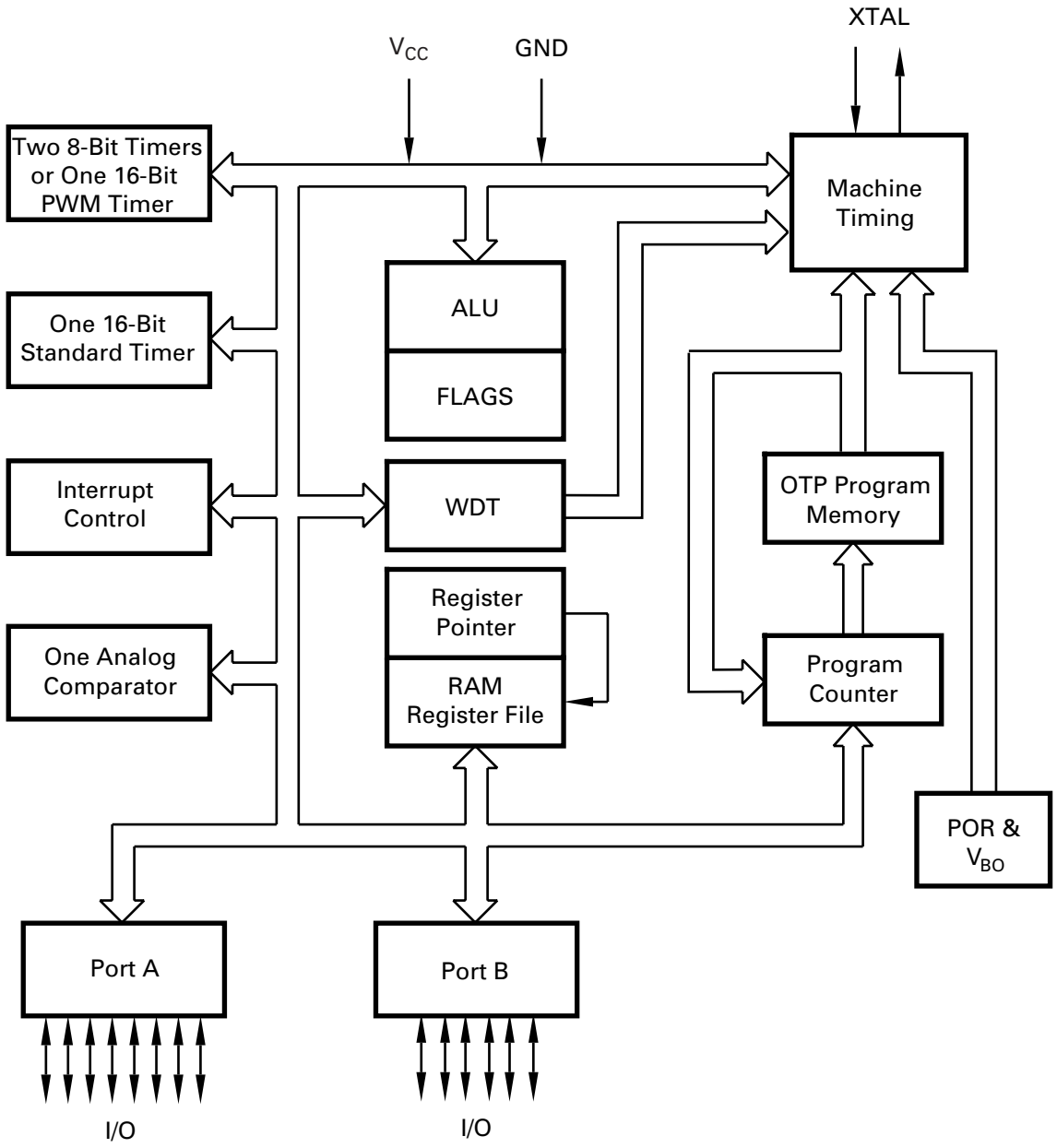


Figure 1. Functional Block Diagram

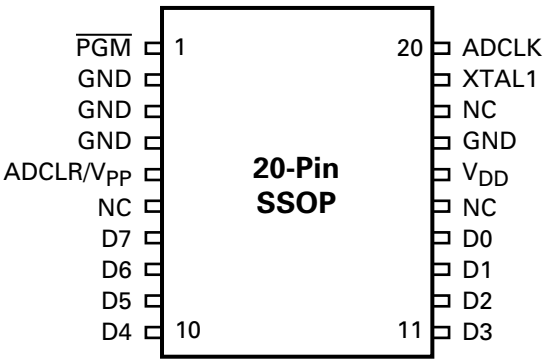


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Table 4. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1-MHz Clock	Input
20	ADCLK	Address Clock	Input

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

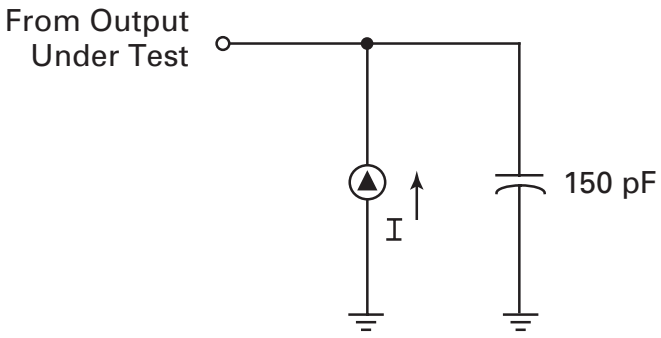


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 5. DC Electrical Characteristics (Continued)

			T_A = 0ºC to +70ºC Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	5,6
		5.5V		6.0	3.5	mA	@ 10 MHz	5,6
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current			500	150	nA	STOP mode V_{IN} = 0V, V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 6. DC Electrical Characteristics (Continued)

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7
		5.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Z8PLUS CORE

The device is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 32 KB of program memory and 4 KB of RAM. Register RAM is accessed as either 8- or 16-bit registers using a combination of 4-, 8-, and 12-bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using 6 addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8Plus reset conditions, reset timing, and register initialization procedures. Reset is generated by the Voltage Brown-Out/Power-On Reset (VBO/POR), Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8Plus device into a known state. To initialize the chip's internal logic, the POR device counts 64 internal clock cycles after the oscillator stabilizes. The control registers and ports are not reset to their default conditions after wakeup from a STOP mode or WDT time-out.

During $\overline{\text{RESET}}$, the value of the program counter is 0020H. The I/O ports and control registers are configured to their default reset state. Resetting the device does not affect the contents of the general-purpose registers.

The $\overline{\text{RESET}}$ circuit initializes the control and peripheral registers, as shown in Table 8. Specific reset values are indicated by a 1 or a 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

Program execution starts 10 External Crystal (XTAL) clock cycles after the POR delay. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration This activity is followed by initialization of the remaining control registers.

Table 8. Control and Peripheral Registers*

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by $\overline{\text{RESET}}$.
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by $\overline{\text{RESET}}$.
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by $\overline{\text{RESET}}$.
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$.
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by $\overline{\text{RESET}}$.
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual copy of the current working register set.
DF–D8	Reserved									
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$.
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after $\overline{\text{RESET}}$.
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$.

Note: *The SMR and WDT flags are set to indicate the source of the $\overline{\text{RESET}}$.

RESET (Continued)

Table 8. Control and Peripheral Registers* (Continued)

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$.
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$.
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$.
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$.
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT enabled in HALT mode, WDT time-out at maximum value, STOP mode disabled.
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled.

Note: *The SMR and WDT flags are set to indicate the source of the $\overline{\text{RESET}}$.

Table 9. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	V_{BO}/POR
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

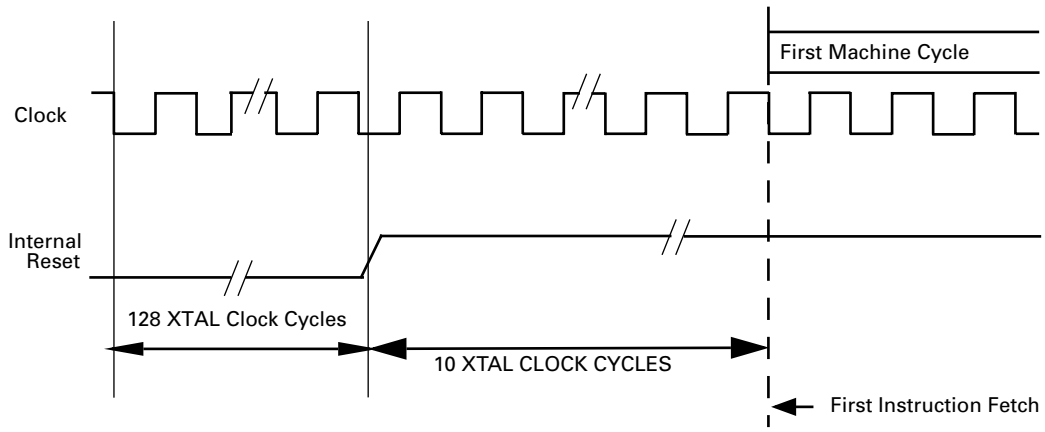


Figure 9. Reset Timing

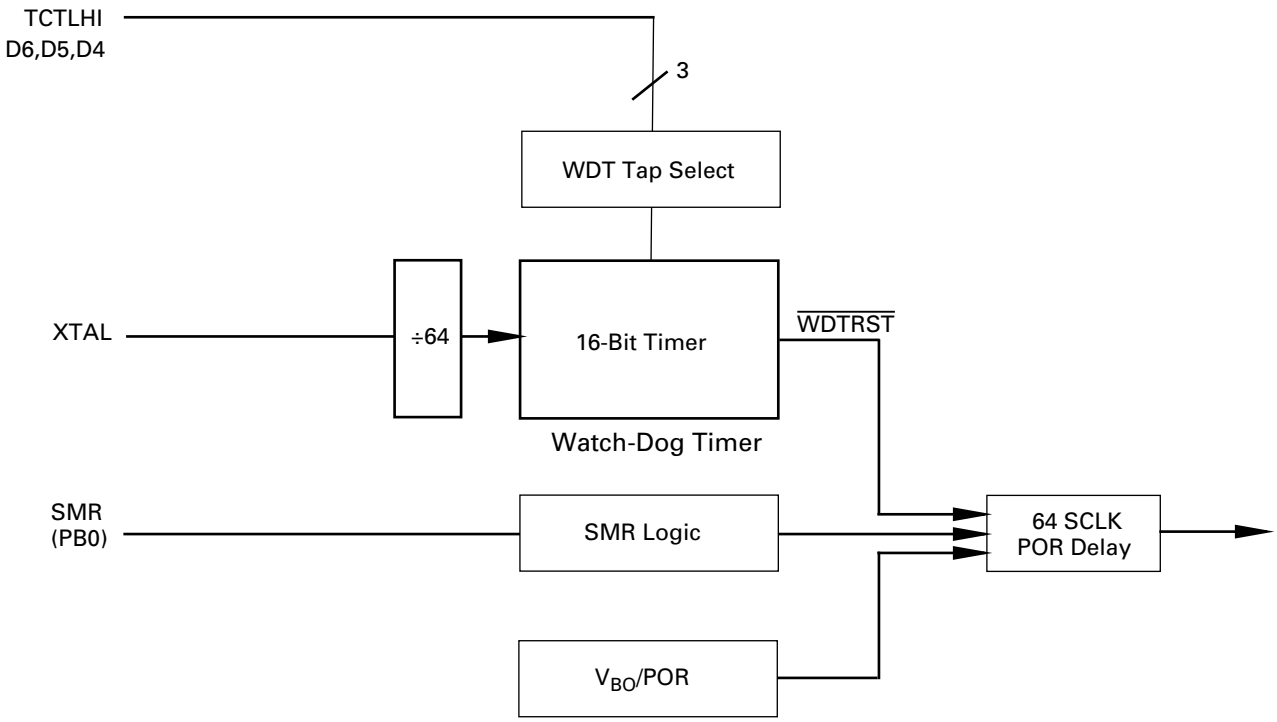


Figure 10. Reset Circuitry with POR, WDT, V_{BO}, and SMR

WATCH-DOG TIMER

The Watch-Dog Timer (WDT) is a retriggerable one-shot 16-bit timer that resets the device if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer time-out periods required in applications, the watch-dog timer is only updated every 64th clock cycle. When operating in the RUN or HALT modes, a WDT time-out reset is functionally equivalent to an interrupt vectoring the PC to 0020H, and setting the WDT flag to 1. Coming out of $\overline{\text{RESET}}$, the WDT is fully enabled with its time-out value set at minimum, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2h and C3h) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$ and when the device enters STOP mode.

The WDT instruction should be executed often enough to provide some margin of time to allow the WDT registers to approach 0. Because the WDT time-out periods are relatively long, a WDT $\overline{\text{RESET}}$ occurs in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

$\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT time-out sets the WDT flag, and the STOP instruction sets the SMR flag. This function enables software to determine whether a WDT time-out or a return from STOP mode occurred. Reading the WDT and SMR flags does not reset the flag to 0; therefore, the user must clear the flag via software.

Note: Failure to clear the SMR flag can result in unexpected behavior.

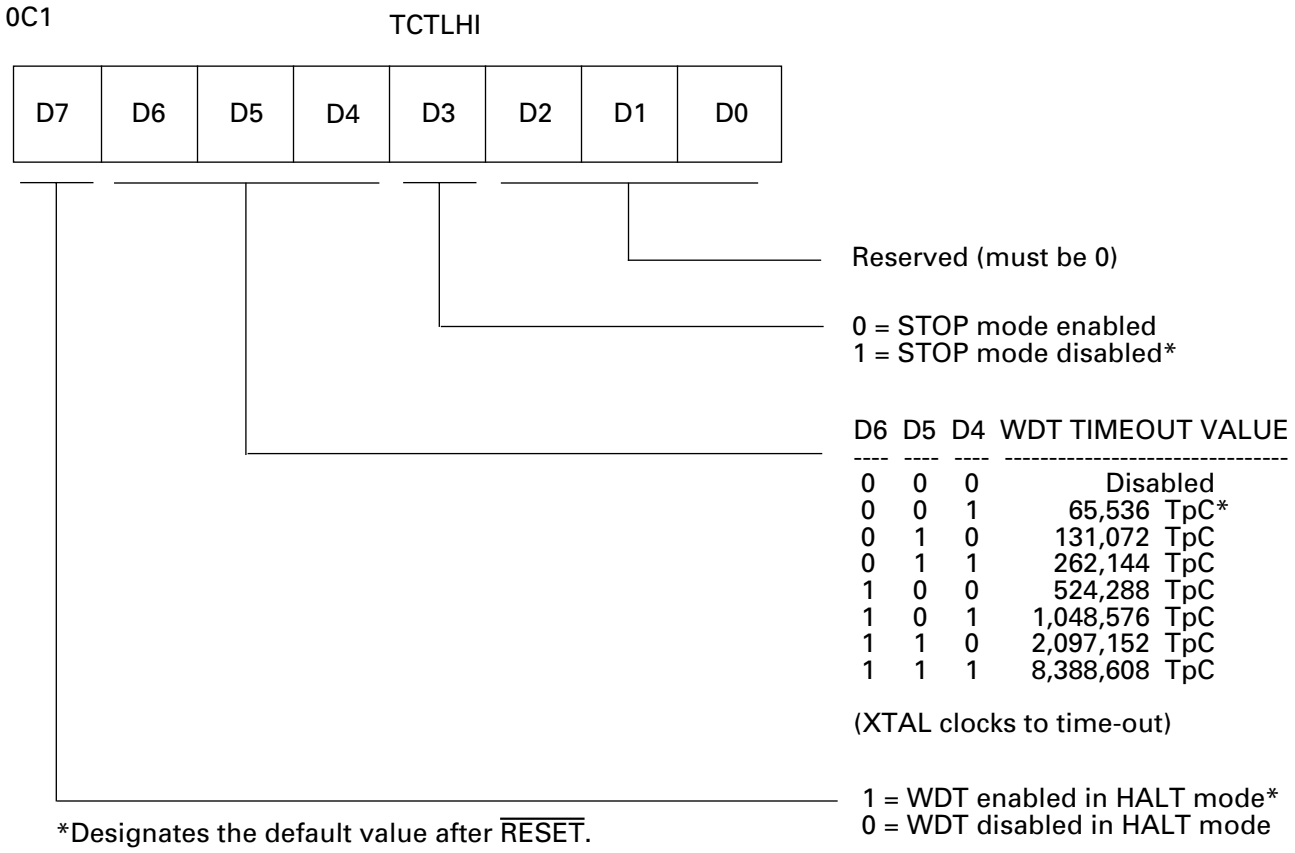


Figure 11. TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of the $\overline{\text{RESET}}$ performs this function. Logic within the device detects that it is in the process of executing the first instruction after the processor leaves $\overline{\text{RESET}}$. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 13 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are 001, which sets the WDT to its minimum time-out period when coming out of $\overline{\text{RESET}}$.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT mode. A 0 prevents the WDT from resetting the part while halted. Coming out of $\overline{\text{RESET}}$, the WDT is enabled during HALT mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the device STOP mode is disabled. If an application requires use of STOP mode, bit D3 must be cleared immediately at leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters STOP mode.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 13. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10-MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	8,388,608 TpC	838.86 ms

Note: *TpC is an XTAL clock cycle. The default at reset is 001.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8Plus MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter HALT mode, the device only requires a HALT instruction. It is *not* necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT        ; enter HALT mode
```

HALT mode can be exited by servicing an external or internal interrupt. The first instruction executed is the interrupt service routine. At completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) time-out. In these cases, program execution restarts at 0020H, the reset restart address.

CLOCK

The Z8Plus MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, and a divide-by-two shaping circuit. Figure 12 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

By selecting the RC OSCILLATOR option in the graphical user interface (GUI), the circuit may instead be driven by an external Resistor and Capacitor (RC) oscillator. Figure 13 illustrates this configuration. This design is limited to no more than 4 MHz to restrict EMI noise.

Note: The reduced drive strength of this configuration also allows the clock circuit to use a micropower-type crystal (also known as a tuning fork) without reduction resistors.

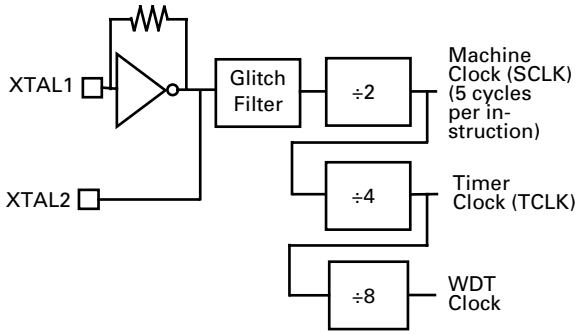


Figure 12. Clock Circuit

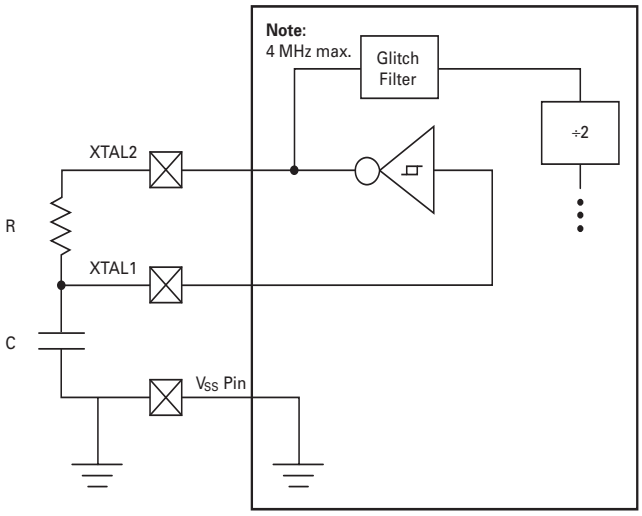


Figure 13. Z8Plus in RC Oscillator Mode

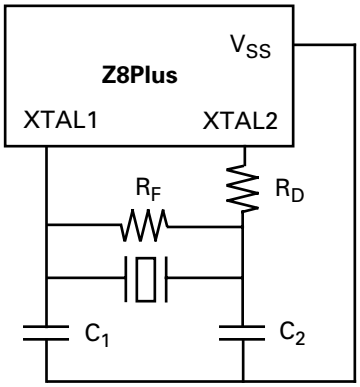


Figure 16. Crystal/Ceramic Resonator Oscillator

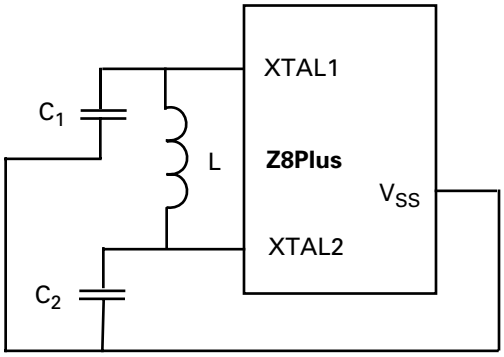


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

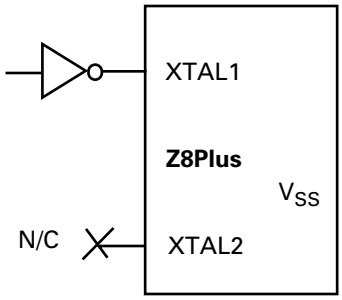


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

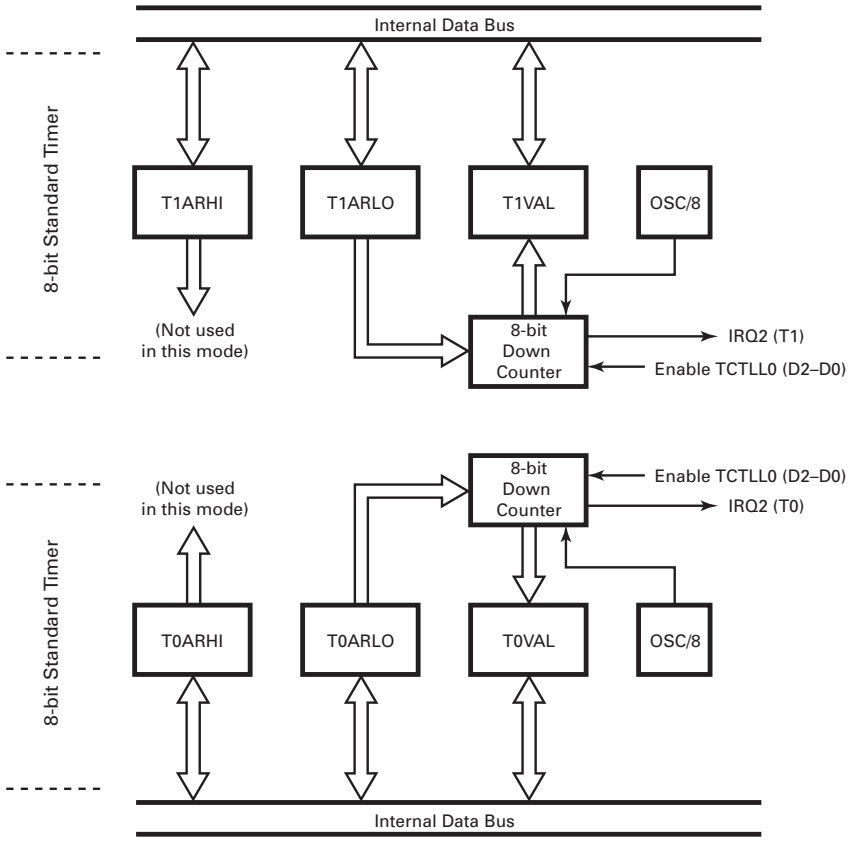


Figure 20. 8-Bit Standard Timers

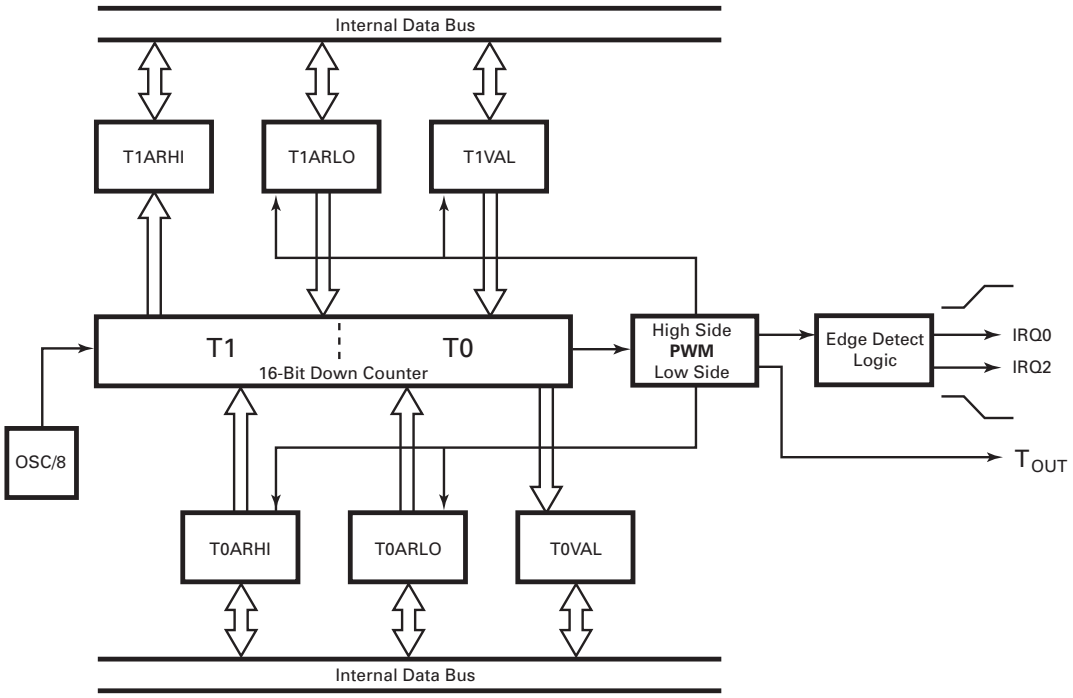


Figure 21. 16-Bit Standard PWM Timer

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

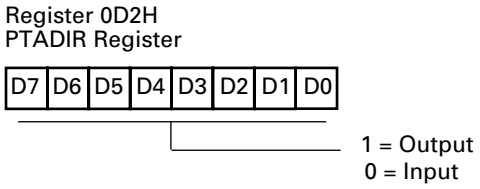


Figure 27. Port A Directional Control Register

PORT A REGISTER DIAGRAMS

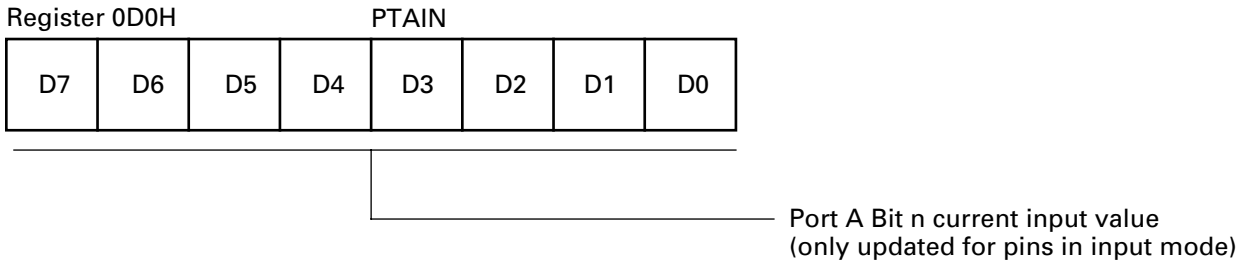


Figure 28. Port A Input Value Register

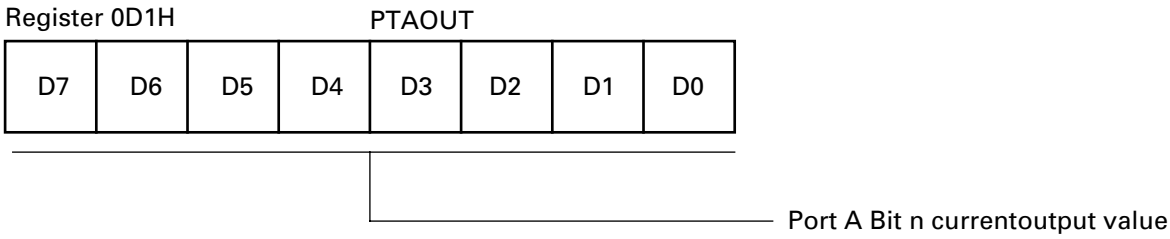


Figure 29. Port A Output Value Register

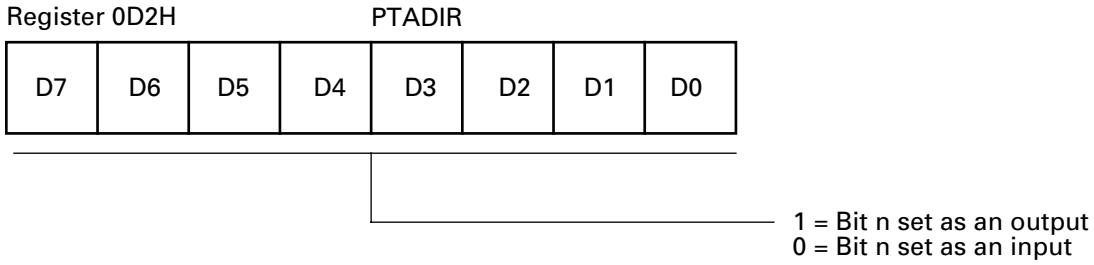


Figure 30. Port A Directional Control Register

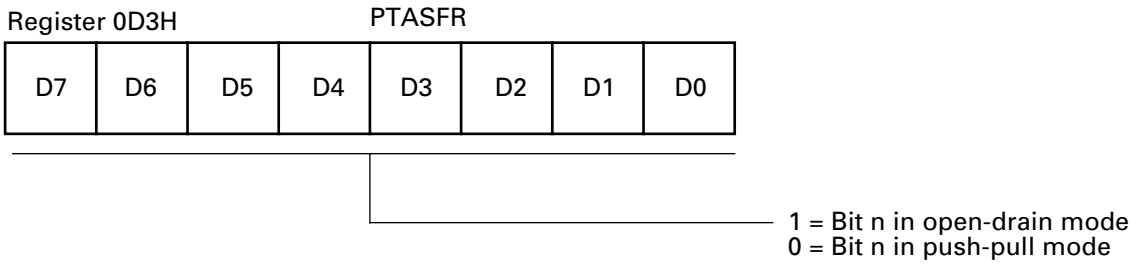


Figure 31. Port A Special Function Register

PORT B—PIN 0 CONFIGURATION

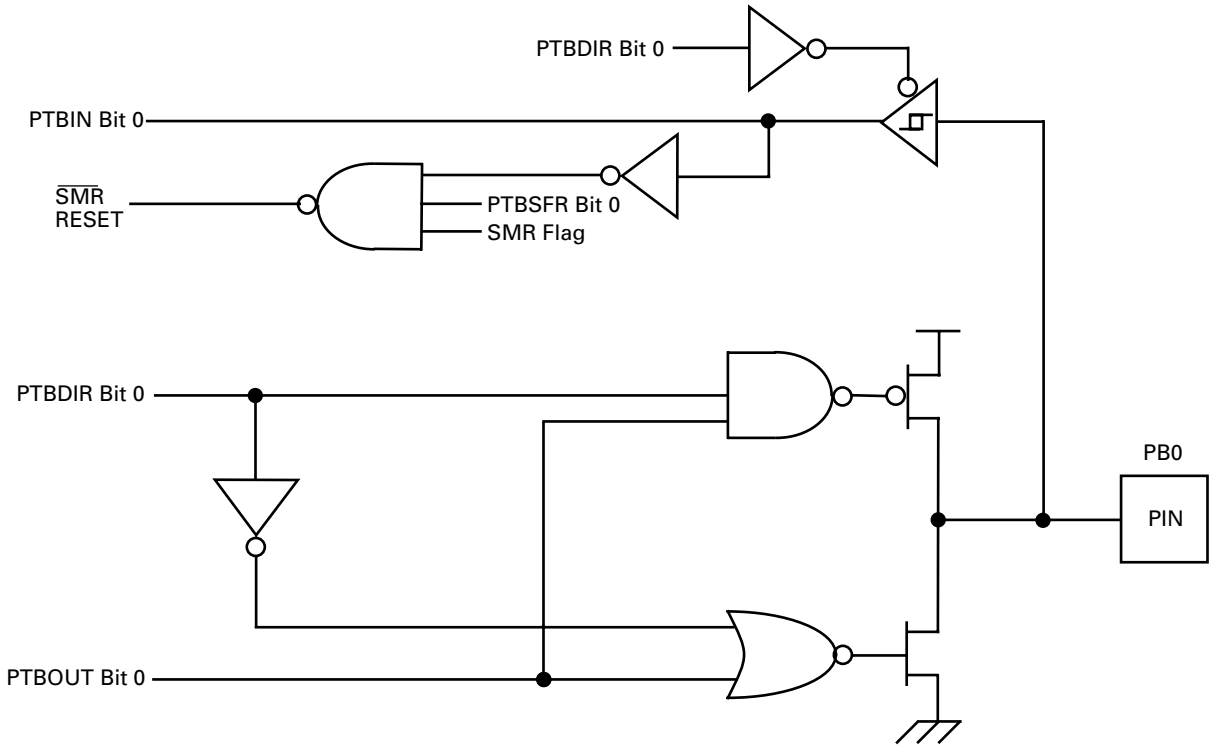
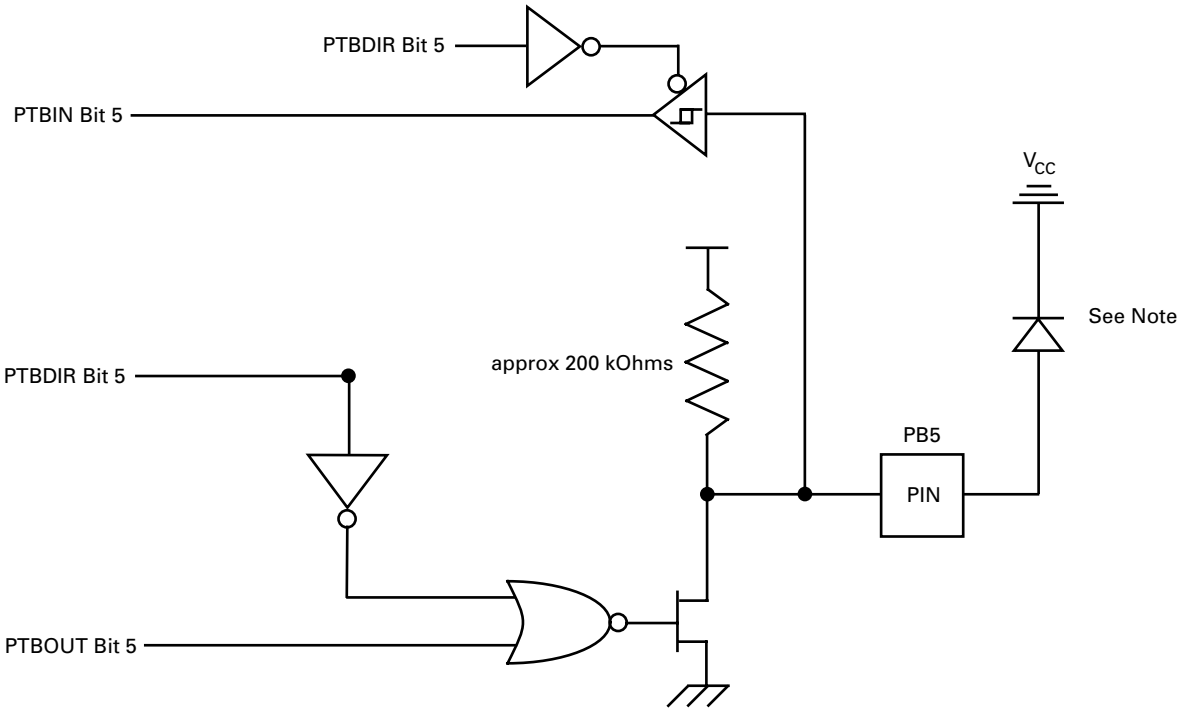


Figure 33. Port B Pin 0 Diagram



Note: There is no high-side protection device. The user should always place an external protection diode as shown.

Figure 34. Port B Pin 5 Diagram

PORT B—PIN 1 CONFIGURATION

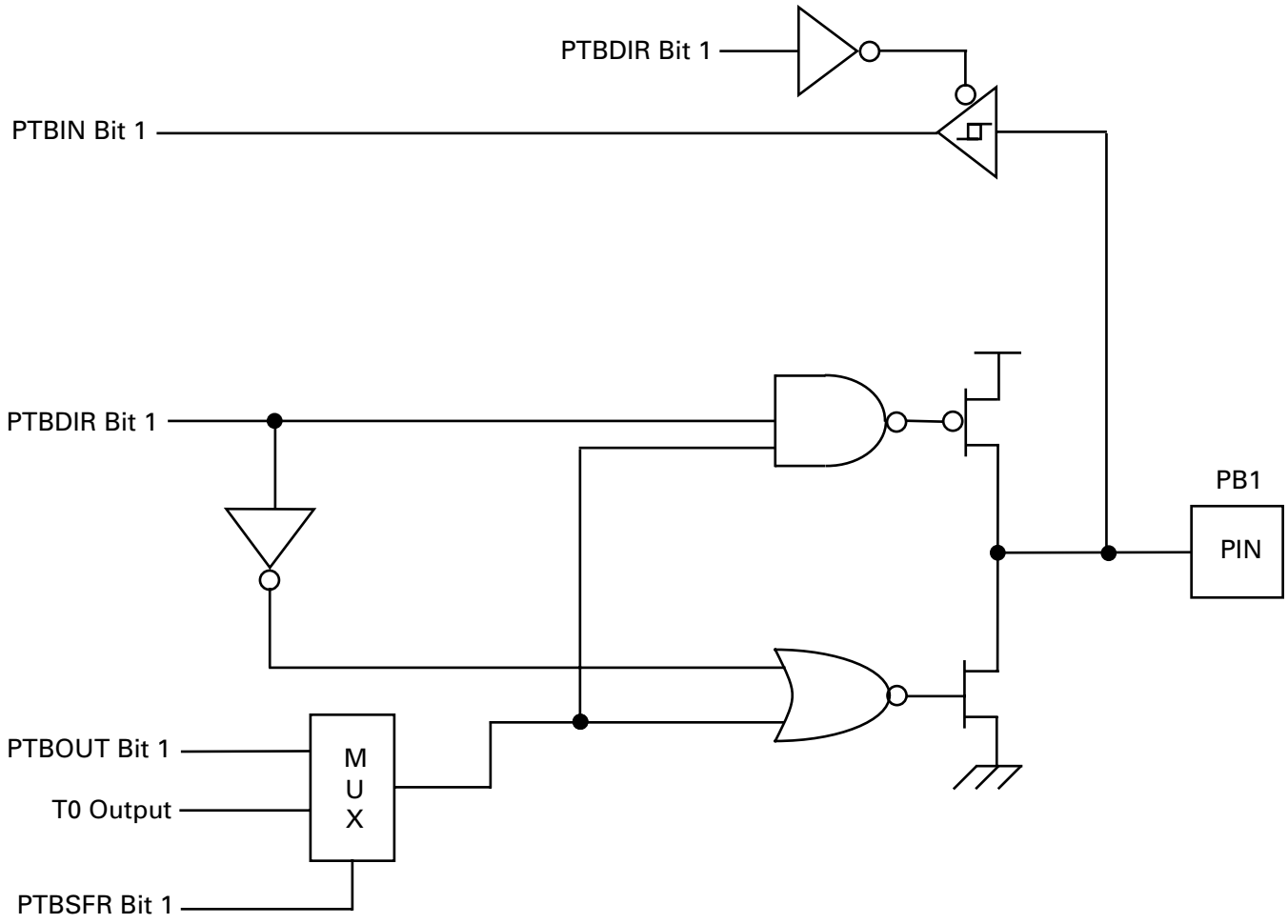


Figure 35. Port B Pin 1 Diagram

PORT B—PIN 2 CONFIGURATION

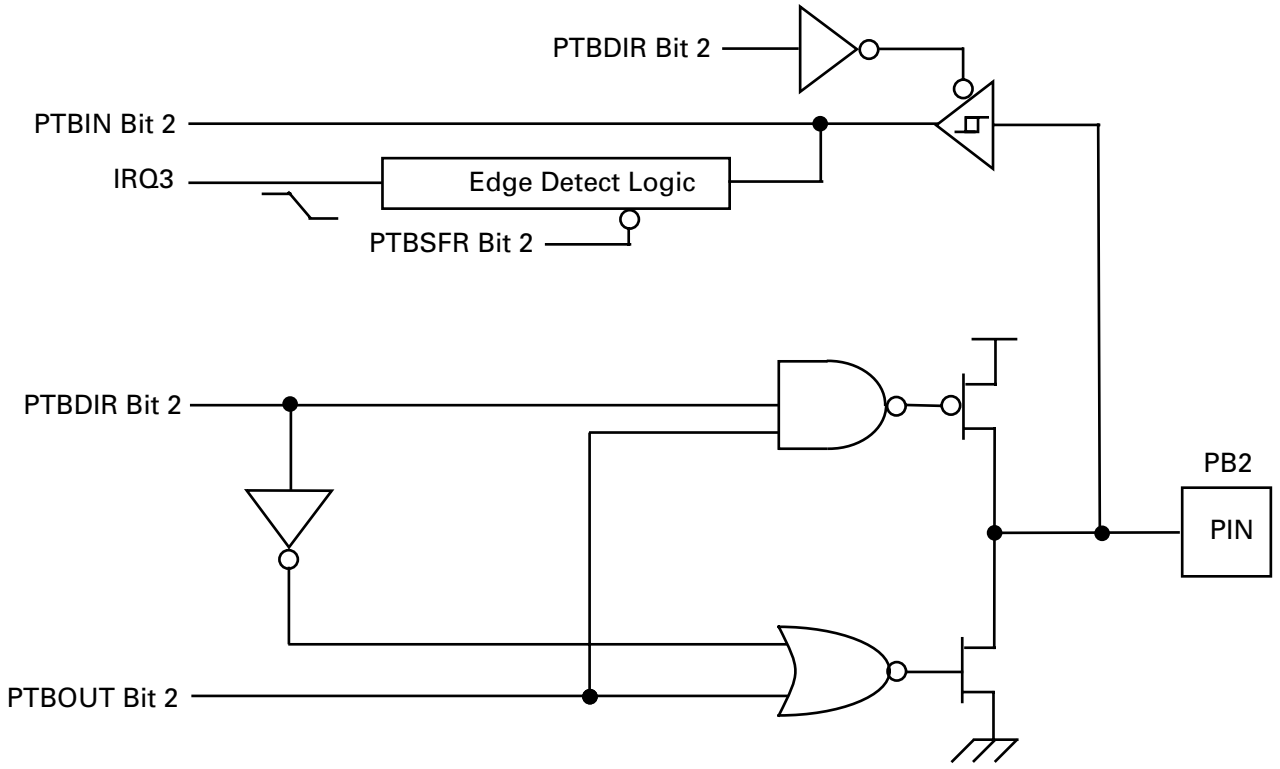


Figure 36. Port B Pin 2 Diagram

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

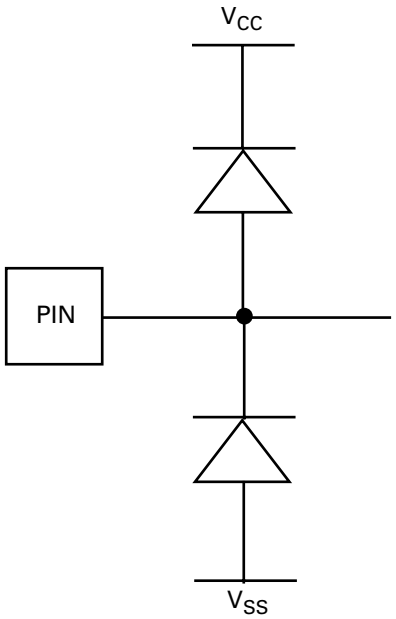


Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

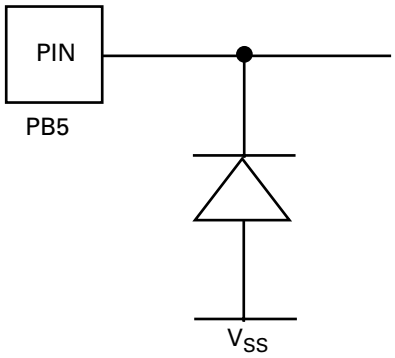
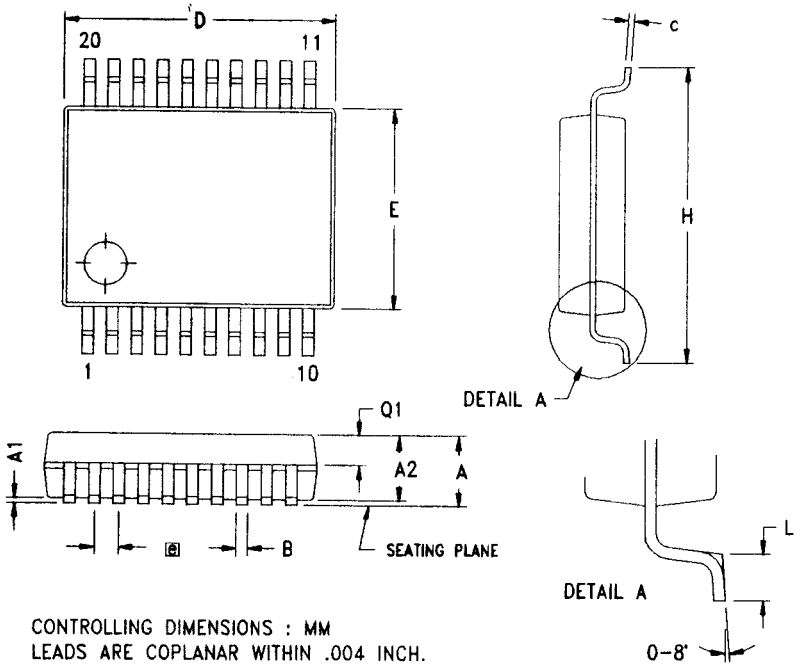


Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram