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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe002pz010sc

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, $\overline{B/W}$, in which WORD is active Low; and $\overline{B/W}$, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

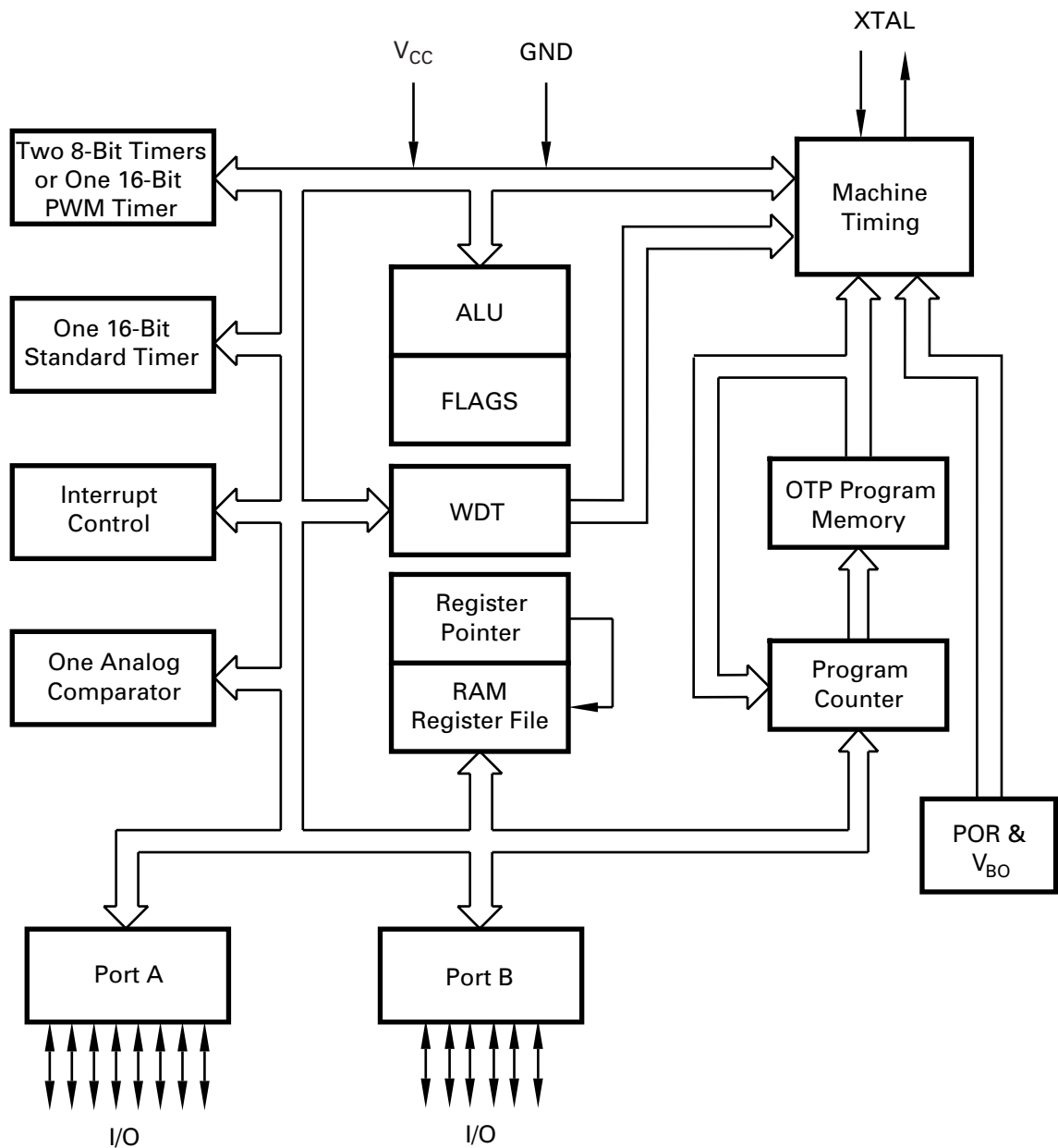


Figure 1. Functional Block Diagram

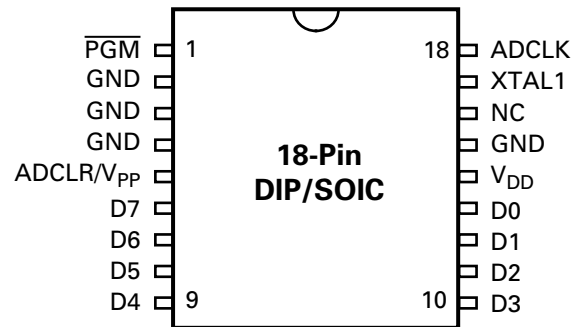


Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{\text{PGM}}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V _{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V _{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1-MHz Clock	Input
18	ADCLK	Address Clock	Input

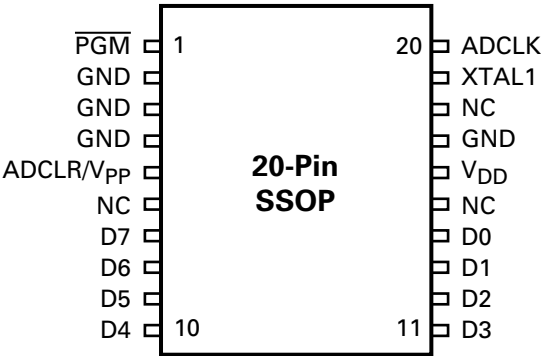


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Table 4. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{\text{PGM}}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V _{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V _{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1-MHz Clock	Input
20	ADCLK	Address Clock	Input

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 6. DC Electrical Characteristics

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ Extended Temperatures								
Sym	Parameter	V_{CC}^1	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0 \text{ mA}$	
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0 \text{ mA}$	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	$I_{OL} = +4.0 \text{ mA}$	
		5.5V		0.4	0.1	V	$I_{OL} = +4.0 \text{ mA}$	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	$I_{OL} = +12 \text{ mA}$	
		5.5V		1.2	0.5	V	$I_{OL} = +12 \text{ mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	4.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
I_{OL}	Output Leakage	4.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
V_{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	$V_{CC} - 1.5\text{V}$		V		3
		5.5V	0	$V_{CC} - 1.5\text{V}$		V		3
R_{PB5}	PB5 Pull-up Resistor	4.5V	100		200	kOhm		4
		5.5V	100		200			
V_{LV}	V_{CC} Low-Voltage Protection		2.45	2.85	2.60	V		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	5,6
		5.5V		7.0	4.0	mA	@ 10 MHz	5,6

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees $5.0\text{V} \pm 0.5\text{V}$.
2. Typical values are measured at $V_{CC} = 5.0\text{V}$; $V_{SS} = 0\text{V} = \text{GND}$.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC} . External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. $CL1 = CL2 = 22 \text{ pF}$.
7. Same as note 5, except inputs are at V_{CC} .

Table 6. DC Electrical Characteristics (Continued)

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ Extended Temperatures								
Sym	Parameter	V_{CC}^1	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode $V_{IN} = 0V$, $V_{CC} @ 10 \text{ MHz}$	5,6
		5.5V		2.0	1.0	mA	HALT mode $V_{IN} = 0V$, $V_{CC} @ 10 \text{ MHz}$	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} $= 0V, V_{CC}$	7
		5.5V		700	250	nA	STOP mode V_{IN} $= 0V, V_{CC}$	7

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees $5.0V \pm 0.5V$.
2. Typical values are measured at $V_{CC} = 5.0V$; $V_{SS} = 0V = \text{GND}$.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC} . External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. $CL1 = CL2 = 22 \text{ pF}$.
7. Same as note 5, except inputs are at V_{CC} .

INTERRUPT SOURCES

Table 10 presents the interrupt types, sources, and vectors available in the Z8Plus. Other processors from the Z8Plus family may define the interrupts differently.

Table 10. Interrupt Types, Sources, and Vectors

Name	Sources	Vector Location	Comments	Fixed Priority
IREQ ₀	Timer0 Time-out	2,3	Internal	1 (Highest)
IREQ ₁	PB4 High-to-Low Transition	4,5	External (PB4), Edge Triggered	2
IREQ ₂	Timer1 Time-out	6,7	Internal	3
IREQ ₃	PB2 High-to-Low Transition	8,9	External (PB2), Edge Triggered	4
IREQ ₄	PB4 Low-to-High Transition	A,B	External (PB4), Edge Triggered	5
IREQ ₅	Timer2 Time-out	C,D	Internal	6 (Lowest)
IREQ ₆ –IREQ ₁₅	Reserved		Reserved for future expansion	

External Interrupt Sources

External sources can be generated by a transition on the corresponding port pin. The interrupt may detect a rising edge, a falling edge, or both.

Notes: The interrupt sources and trigger conditions are device dependent. See the device product specification to determine available sources (internal and external), triggering edge options, and exact programming details.

Although interrupts are edge triggered, minimum interrupt request Low and High times must be observed for proper operation. See the device product specification for exact timing requirements on external interrupt requests ($T_{W/L}$, $T_{W/H}$).

Internal Interrupt Sources

Internal interrupt sources and trigger conditions are device dependent. On-chip peripherals may set interrupt under various conditions. Some peripherals always set their corresponding IREQ bit while others must be specifically configured to do so.

See the device product specification to determine available sources, triggering edge options, and exact programming

details. For more details on the interrupt sources, refer to the chapters describing the timers, comparators, I/O ports, and other peripherals.

Interrupt Mask Register (IMASK) Initialization

The IMASK register individually or globally enables or disables the interrupts (Table 11). When bits 0 through 5 are set to 1, the corresponding interrupt requests are enabled. Bit 7 is the master enable bit and must be set before any of the individual interrupt requests can be recognized. Resetting bit 7 disables all the interrupt requests. Bit 7 is set and reset by the EI and DI instructions. It is automatically set to 0 during an interrupt service routine and set to 1 following the execution of an Interrupt Return (IRET) instruction. The IMASK registers are reset to 00h, disabling all interrupts.

Notes: It is not good programming practice to directly assign a value to the master enable bit. A value change should always be accomplished by issuing the EI and DI instructions.

Care should be taken not to set or clear IMASK bits while the master enable is set.

IREQ SOFTWARE INTERRUPT GENERATION

IREQ can be used to generate software interrupts by specifying IREQ as the destination of any instruction referencing the Z8Plus Standard Register File. These software interrupts (SWI) are controlled in the same manner as hardware generated requests. In other words, the IMASK controls the enabling of each SWI.

To generate a SWI, the request bit in IREQ is set by the following statement:

```
OR IREQ, #NUMBER
```

The immediate data variable, **NUMBER**, has a 1 in the bit position corresponding to the required level of SWI. For example, an SWI must be issued when an IREQ5 occurs. Bit 5 of **NUMBER** must have a value of 1.

```
OR IREQ, #00100000B
```

If the interrupt system is globally enabled, IREQ5 is enabled, and there are no higher priority requests pending, control is transferred to the service routine pointed to by the IREQ5 vector.

Note: Software may modify the IREQ register at any time. Care should be taken when using any instruction that modifies the IREQ register while interrupt sources are active. The software writeback always takes precedence over the hardware. If a software writeback takes place on the

same cycle as an interrupt source tries to set an IREQ bit, the new interrupt is lost.

Nesting of Vectored Interrupts

Nesting vectored interrupts allows higher priority requests to interrupt a lower priority request. To initiate vectored interrupt nesting, perform the following steps during the interrupt service routine:

- PUSH the old IMASK on the stack
- Load IMASK with a new mask to disable lower priority interrupts
- Execute an EI instruction
- Proceed with interrupt processing
- Execute a DI instruction after processing is complete
- Restore the IMASK to its original value by POPing the previous mask from the stack
- Execute IRET

Depending on the application, some simplification of the above procedure may be possible.

RESET Conditions

The IMASK and IREQ registers initialize to 00h on RESET.

PROGRAMMABLE OPTIONS

EPROM Protect. When selecting the DISABLE EPROM PROTECT/ENABLE TESTMODE option, the user can read the software code in the program memory. ZiLOG's internal factory test mode, or any of the standard test mode methods, are useful for reading or verifying the code in the microcontroller when using an EPROM programmer. If the user should select the ENABLE EPROM PROTECT/DISABLE TESTMODE option, it is not possible to read the code using a tester, programmer, or any other standard method. As a result, ZiLOG is unable to test the EPROM memory at any time after customer delivery.

This option bit only affects the user's ability to read the code and has no effect on the operation of the part in an application. ZiLOG tests the EPROM memory before customer delivery whether or not the ENABLE EPROM PROTECT/DISABLE TESTMODE option is selected; ZiLOG provides a standard warranty for the part.

System Clock Source. When selecting the RC OSCILLATOR ENABLE option, the oscillator circuit on the microcontroller is configured to work with an external RC circuit. When selecting the Crystal/Other Clock Source option, the oscillator circuit is configured to work with an external crystal, ceramic resonator, or LC oscillator.

STOP MODE OPERATION

The STOP mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP mode, the Z8Plus only requires a STOP instruction. It is *not* necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F  STOP  ;enter STOP mode
```

The STOP mode is exited by any one of the following resets: POR or a Stop-Mode Recovery source. At reset generation, the processor always restarts the application program at address 0020H, and the STOP mode flag is set. Reading the STOP mode flag does not clear it. The user must clear the STOP mode flag with software.

Note: Failure to clear the STOP mode flag can result in undefined behavior.

The Z8Plus provides a dedicated Stop-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin PB0 (I/O Port B, bit 0) triggers an SMR. To use this mode, pin PB0 must be configured as an input and the special function selected before the STOP mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM} . Program execution starts at address 20h, after the POR delay.

Notes: 1. The PB0 input, when used for Stop-Mode Recovery, does not initialize the control registers.

The STOP mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the device's operating range
- Output current sourcing is minimized
- All inputs (digital and analog) are at the Low or High rail voltages

2. For detailed information about flag settings, see the [Z8Plus User's Manual](#).

OSCILLATOR OPERATION (Continued)

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8Plus as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry

and the internal system clock output should be separated as much as possible.

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 meg-Ohms.

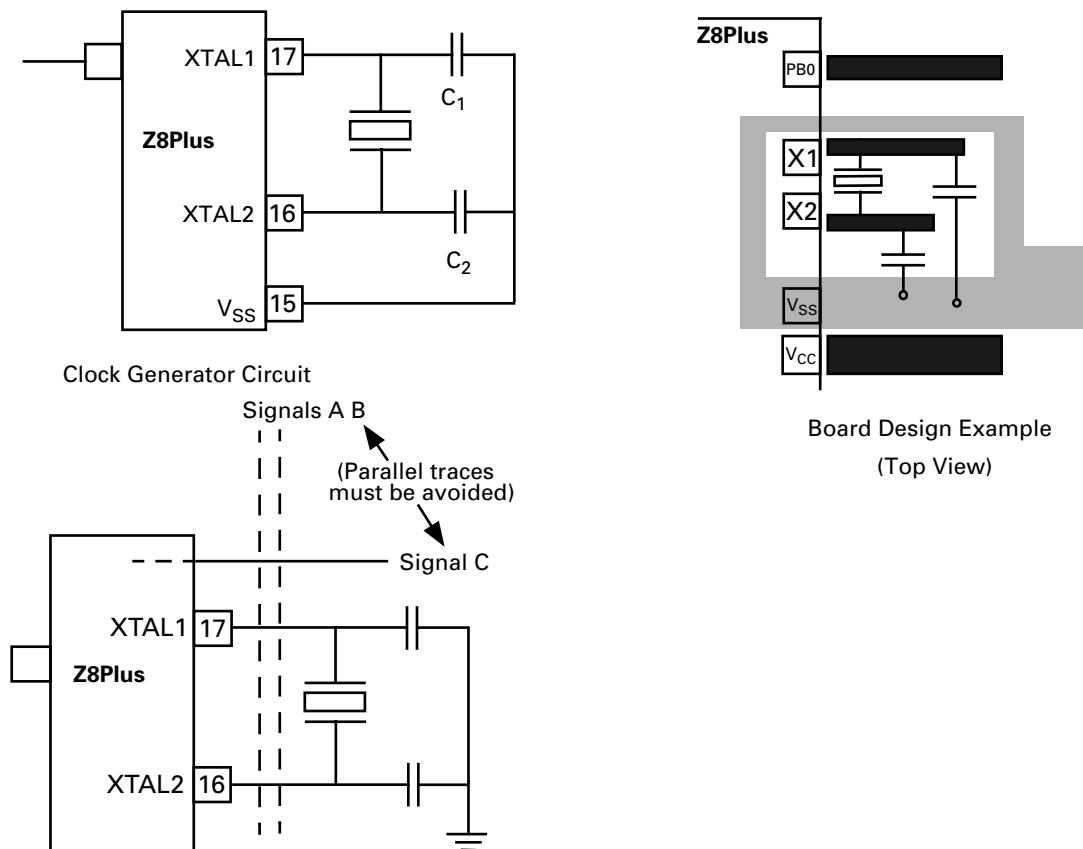


Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should exhibit the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, fundamental mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 Ohms maximum

Depending on the operation frequency, the oscillator may require additional capacitors, C_1 and C_2 , as illustrated in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturer's crystal specifications.

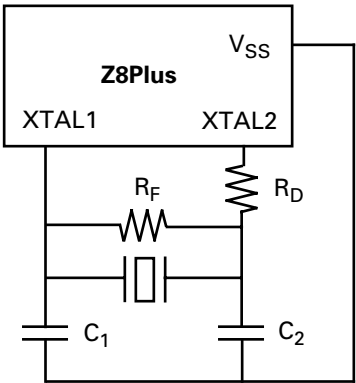


Figure 16. Crystal/Ceramic Resonator Oscillator

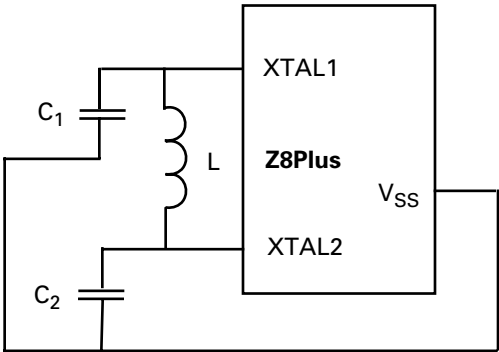


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crys-

tal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

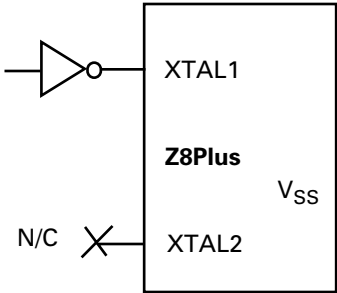


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2 , including all parasitics (PCB and holder).

TIMERS (Continued)

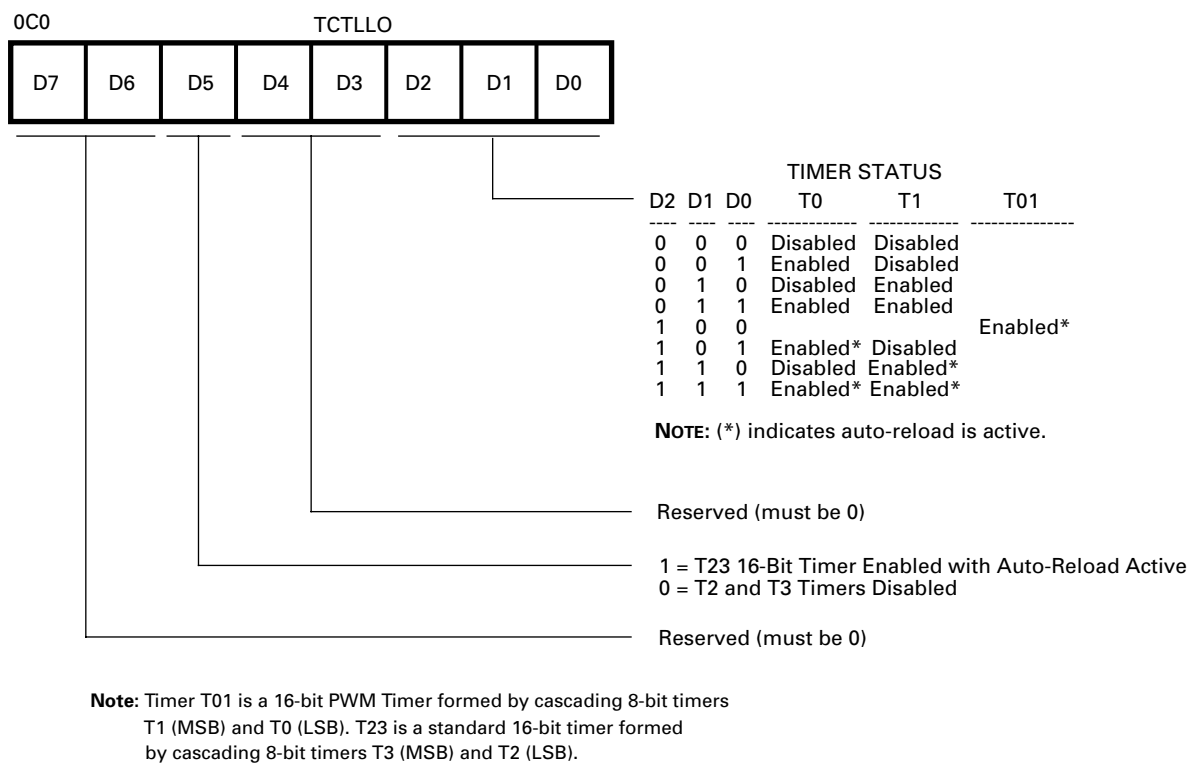


Figure 22. TCTLLO Register

A pair of READ/WRITE registers is utilized for each 8-bit timer. One register is defined to contain the auto-initialization value for the timer. The second register contains the current value for the timer. When a timer is enabled, the timer decrements the value in its count register and continues decrementing until it reaches 0. An interrupt is generated, and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer stops counting when the value reaches 0. Control logic clears the appropriate control register bit to disable the timer. This operation is referred to as a *single-shot*. If auto-initialization is enabled, the timer counts from the initialization value. Software must not attempt to use timer registers for any other function.

User software is allowed to write to any WRITE register at any time; however, care should be taken if timer registers are updated while the timer is enabled. If software changes the count value while the timer is in operation, the timer continues counting from the updated value.

Note: Unpredictable behavior can occur if the value updates at the same time that the timer reaches 0.

Similarly, if user software changes the initialization value register while the timer is active, the next time that the timer reaches 0, the timer initializes to the changed value.

Note: Unpredictable behavior can occur if the initialization value register is changed while the timer is in the process of being initialized.

The initialization value is determined by the exact timing of the WRITE operation. In all cases, the Z8Plus assigns a higher priority to the software WRITE than to a decremter write-back. However, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software WRITE. A READ of either register can be conducted at any time, with no effect on the functionality of the timer.

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16-bit timer. The interrupt for the combined timer is defined to be generated by timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function is performed automatically.

All 16-bit timers continue counting while their interrupt requests are active and operate independently of each other.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt is responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the WRITE begin counting from the value in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source input only. Each enabled timer is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initial-

ization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it alternately initializes its count value using the Low auto-init pair, followed by the High auto-init pair. This functionality corresponds to a PWM. That is, the T1 interrupt defines the end of the High section of the waveform, and the T0 interrupt marks the end of the Low portion of the PWM waveform.

The PWM begins counting with whatever data is held in the count registers. After this value expires, the first reload depends on the state of the PB1 pin if T_{OUT} mode is selected. Otherwise, the Low value is applied first.

After the auto-initialization is completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt IRQ2 is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H; Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6; Figure 24) to configure PB1 for T_{OUT} operation for T0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 is capable of being a clock output for T0, toggling the PB1 output pin on each T0 time-out.

At end-of-count, the interrupt request line (IRQ0), clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when T0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, T0 is in Continuous Counting Mode, T_{OUT} exhibits a 50-percent duty cycle output. If the timer pair is selected (T01) as a PWM, the duty cycle depends on the High and Low reload values. At the end of each High time, PB1 toggles Low. At the end of each Low time, PB1 toggles HI.

RESET CONDITIONS

After a $\overline{\text{RESET}}$, the timers are disabled. See Table 8 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8Plus dedicates 14 lines to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide either standard input/output, or the following special functions: T0 output, comparator input, SMR input, and external interrupt inputs.

All pins except PB5 include push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation. The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question. Each port is defined by a set of four control registers (Figure 26).

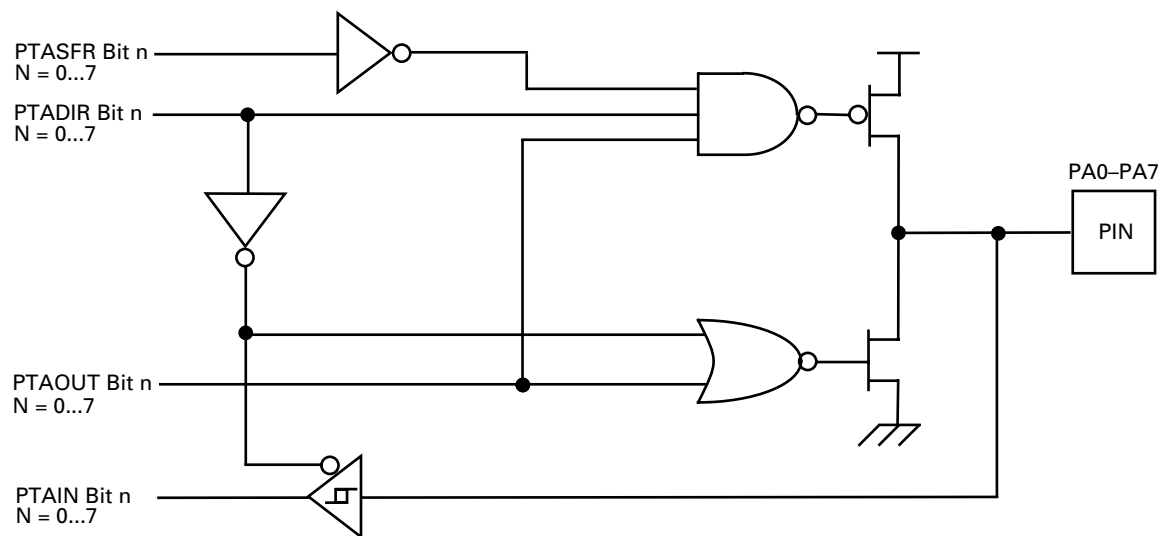


Figure 26. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

Directional Control and Special Function Registers

Each port on the Z8Plus features a dedicated directional control register that determines (on a bit-wise basis) if a given port bit operates as input or output. Each port on the Z8Plus features a special function register (SFR) that, in conjunction with the directional control register, implements (on a bit-by-bit basis) any special functionality that can be defined for each particular port bit.

Table 14. I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port features an Output Value Register and an input value register. For port bits configured as an input by means of the directional control register, the input value register

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto

the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port’s directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-

pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

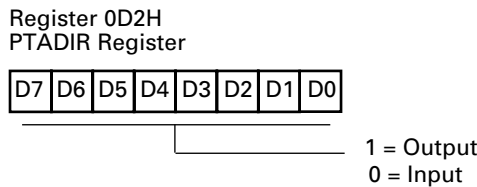


Figure 27. Port A Directional Control Register

PORT A REGISTER DIAGRAMS

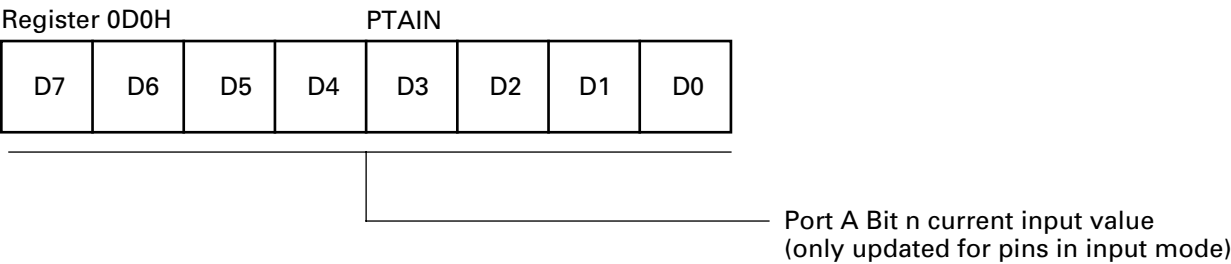


Figure 28. Port A Input Value Register

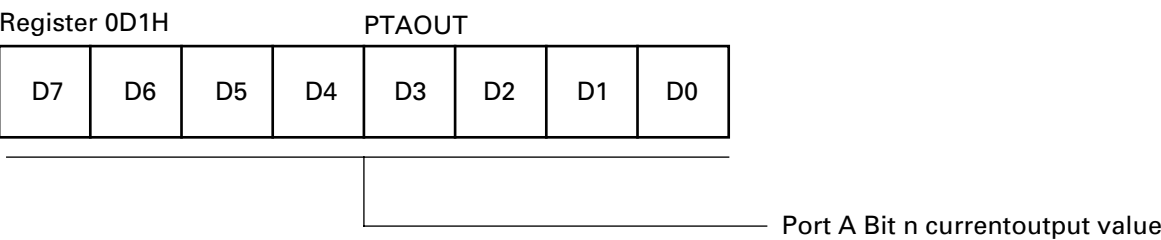


Figure 29. Port A Output Value Register

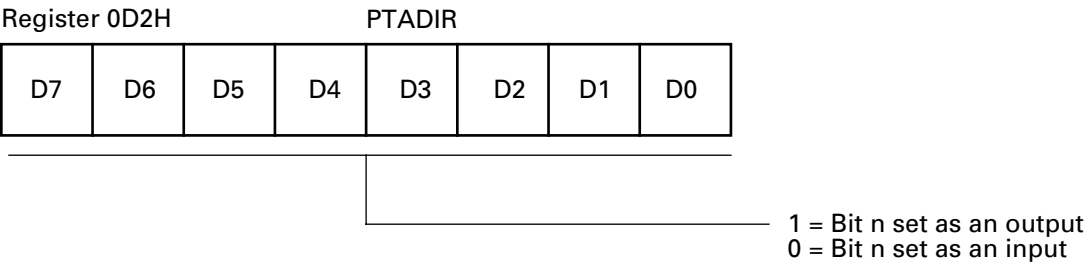


Figure 30. Port A Directional Control Register

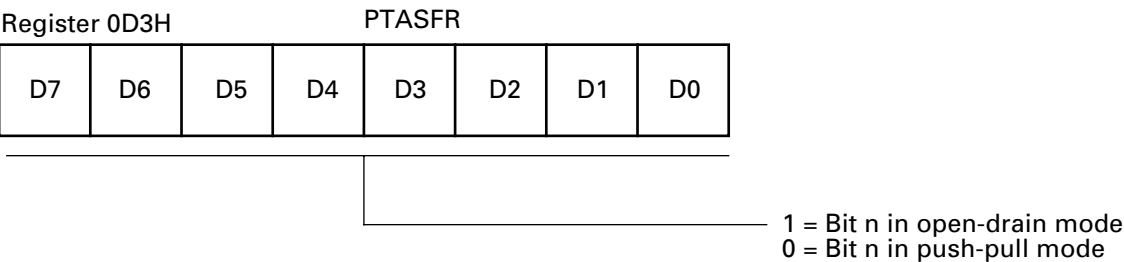


Figure 31. Port A Special Function Register

PORT B CONTROL REGISTERS (Continued)

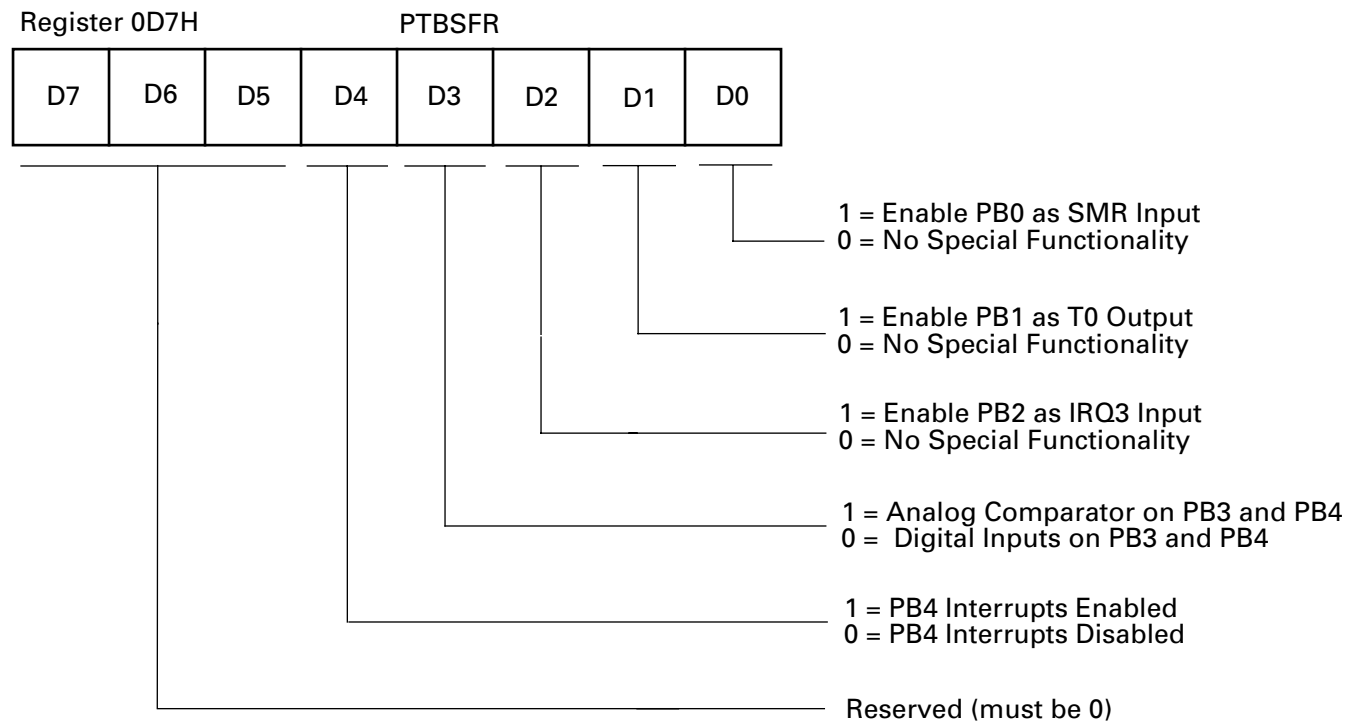


Figure 41. Port B Special Function Register

COMPARATOR OPERATION (Continued)

age Protection trip point (V_{LV}) is reached. The actual Low-Voltage Protection trip point is a function of process parameters.

Low-Voltage Protection is active in RUN and HALT modes only, but is disabled in STOP mode (Figure 42).

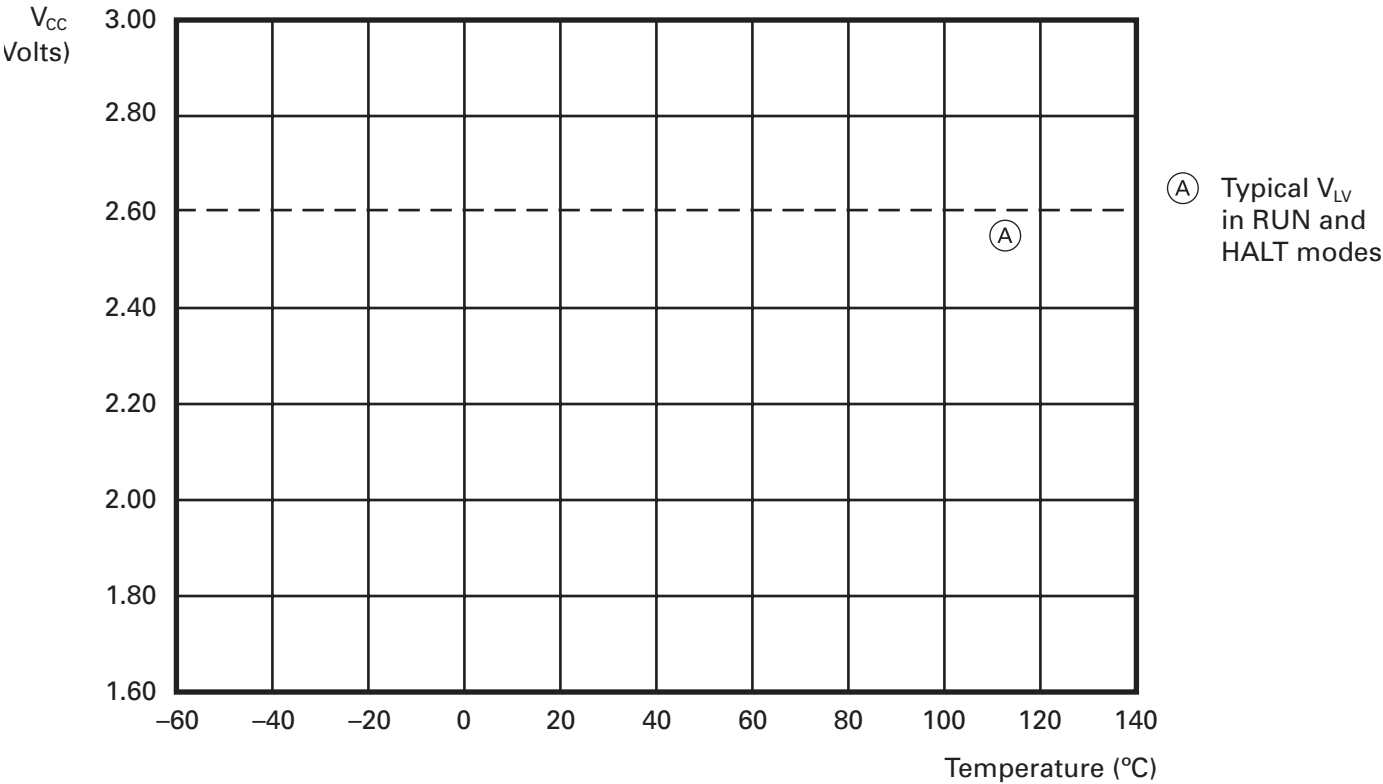


Figure 42. Voltage vs. Temperature

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

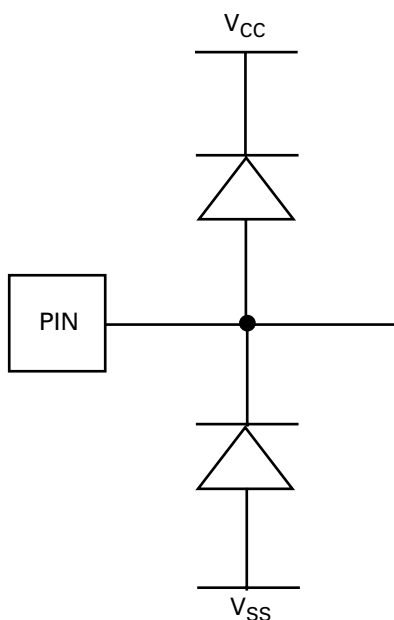


Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

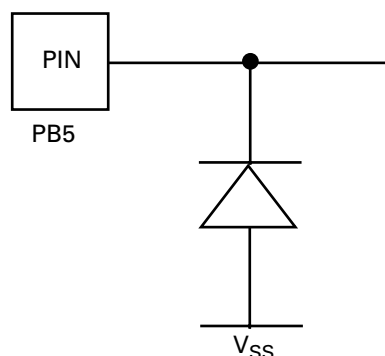
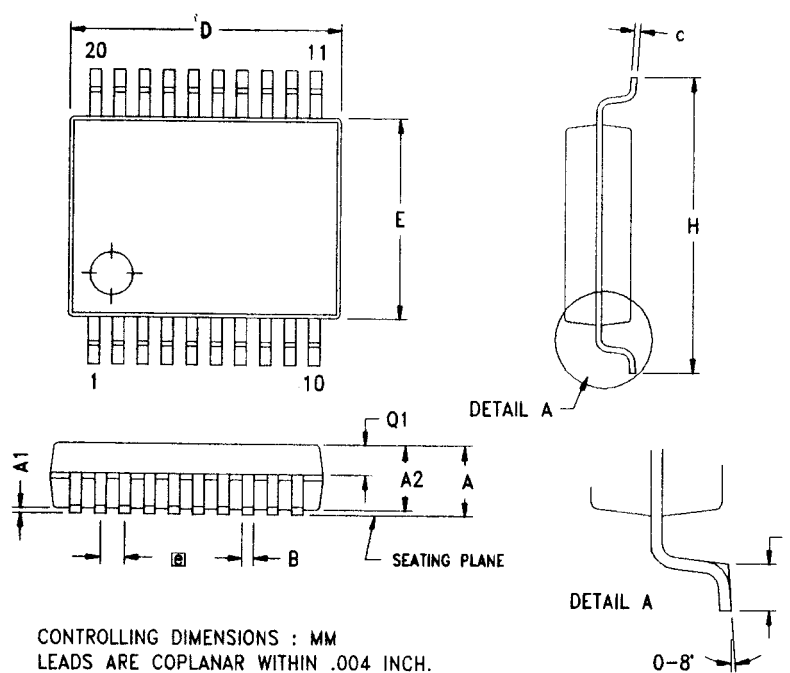


Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
⓪	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram

ORDERING INFORMATION

Standard Temperature

18-Pin DIP	Z8PE002PZ010SC
18-Pin SOIC	Z8PE002SZ010SC
20-Pin SSOP	Z8PE002HZ010SC

Extended Temperature

18-Pin DIP	Z8PE002PZ010EC
18-Pin SOIC	Z8PE002SZ010EC
20-Pin SSOP	Z8PE002CZ010EC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes

Preferred Package	PZ = Plastic DIP
Longer Lead Time	SZ = SOIC
	HZ = SSOP
Speed	010 = 10 MHz
Standard Temperature	S = 0°C to +70°C
Extended Temperature	E = -40°C to +105°C
Environmental Flow	C = Plastic Standard

Example:

The Z8PE002PZ010SC is a 10-MHz DIP, 0°C to 70°C, with Plastic Standard Flow.

Z	ZiLOG Prefix
8PE	Z8Plus Product
002	Product Number
PZ	Package Designation Code
010	Speed
SC	Temperature and Environmental Flow

Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance

with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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