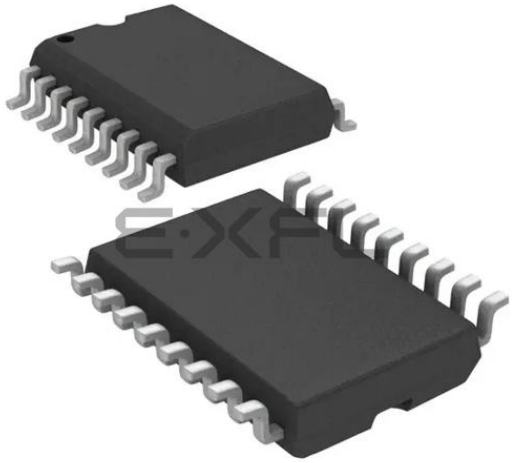

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe002sz010sc

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low; and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

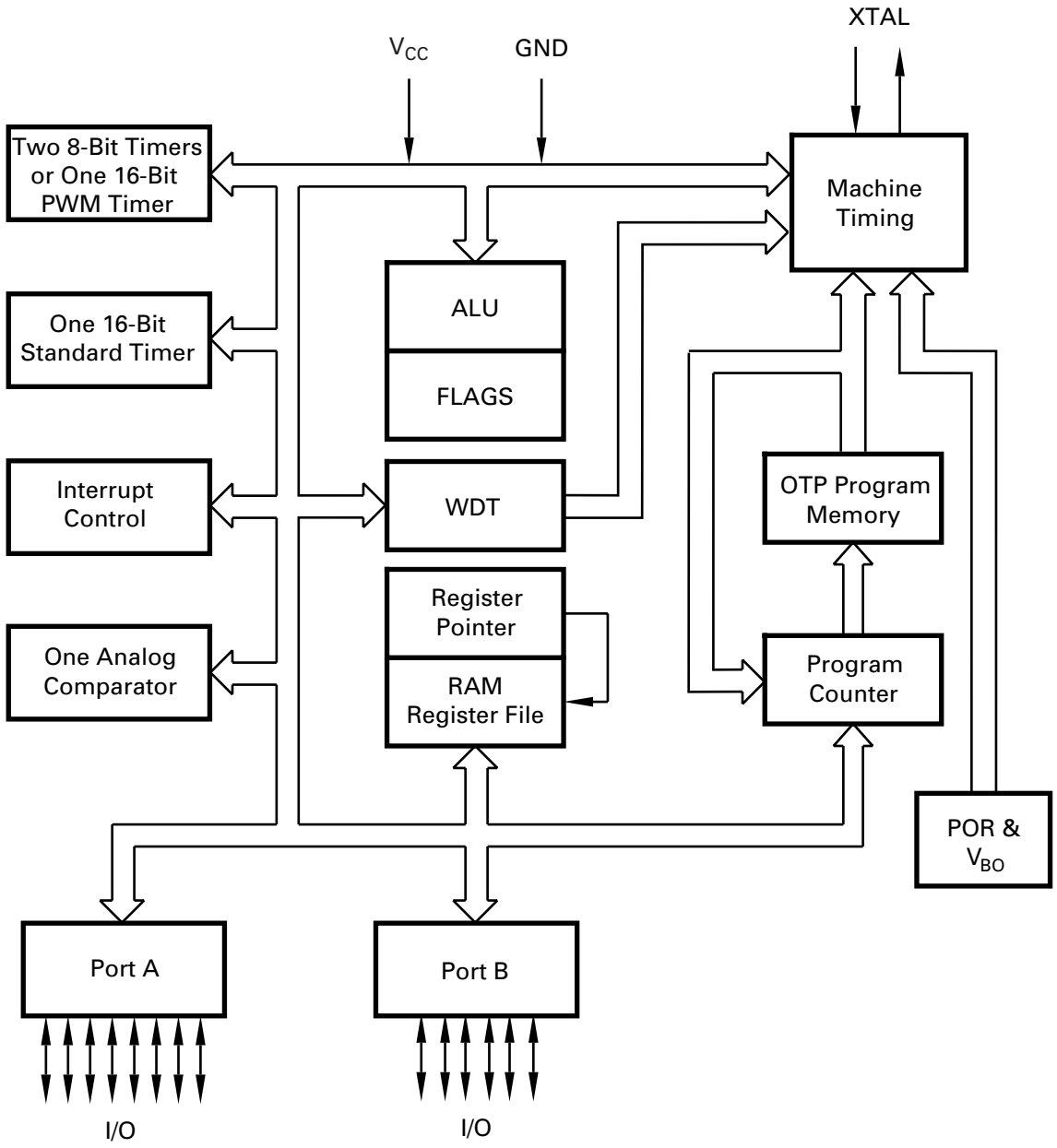

Figure 1. Functional Block Diagram

PIN DESCRIPTION

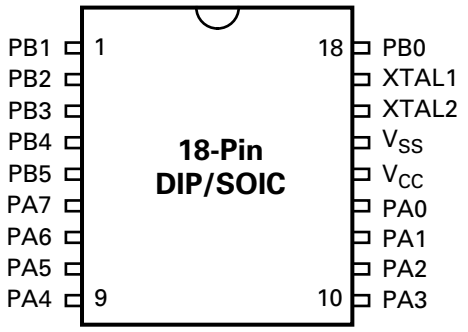

Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

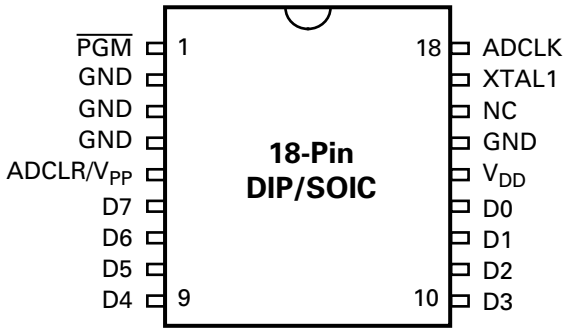

Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1-MHz Clock	Input
18	ADCLK	Address Clock	Input

PIN DESCRIPTION (Continued)

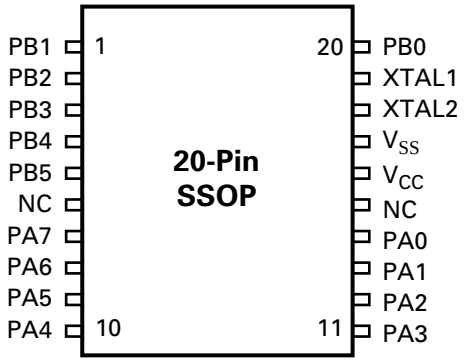

Figure 5. 20-Pin SSOP Pin Identification

Table 3. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	Input/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

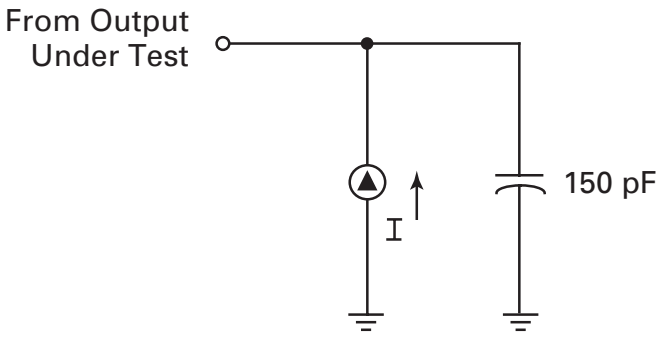

Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 5. DC Electrical Characteristics (Continued)

			T_A = 0ºC to +70ºC Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	5,6
		5.5V		6.0	3.5	mA	@ 10 MHz	5,6
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current			500	150	nA	STOP mode V_{IN} = 0V, V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 6. DC Electrical Characteristics (Continued)

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7
		5.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

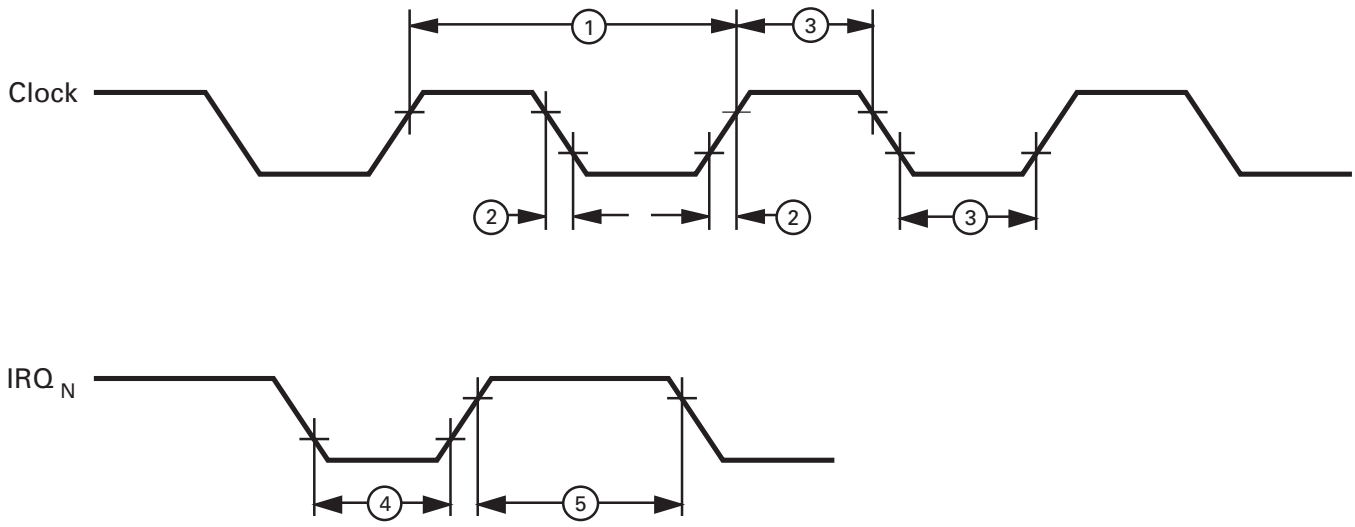

Figure 8. AC Electrical Timing Diagram

Table 7. Additional Timing

				T_A = 0°C to +70°C T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	3.0V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.0V		15	ns	2
			5.5V		15	ns	2
3	T_WC	Input Clock Width	3.0V	50		ns	2
			5.5V	50		ns	2
4	T_WIL	Int. Request Input Low Time	3.0V	70		ns	2
			5.5V	70		ns	2
5	T_WIH	Int. Request Input High Time	3.0V	5TpC			2
			5.5V	5TpC			2
6	T_{WSM}	STOP mode Recovery Width Spec.	3.0V	25		ns	
			5.5V	25		ns	
7	T_{OST}	Oscillator Start-Up Time	3.0V		5TpC		
			5.5V		5TpC		
8	T_{POR}	Power-On Reset Time	3.0V	128 T_PC + T_{OST}			
			5.5V				

Notes:
1. The V_{DD} voltage specification of 3.0V guarantees 3.0V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logical 1 and 0.2 V_{CC} for a logical 0.

RESET (Continued)

Table 8. Control and Peripheral Registers* (Continued)

		Bits								
Register (HEX)	**Register Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Comments**
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$.
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$.
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$.
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$.
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT enabled in HALT mode, WDT time-out at maximum value, STOP mode disabled.
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled.

Note: *The SMR and WDT flags are set to indicate the source of the $\overline{\text{RESET}}$.

Table 9. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	V_{BO}/POR
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

IREQ SOFTWARE INTERRUPT GENERATION

IREQ can be used to generate software interrupts by specifying IREQ as the destination of any instruction referencing the Z8Plus Standard Register File. These software interrupts (SWI) are controlled in the same manner as hardware generated requests. In other words, the IMASK controls the enabling of each SWI.

To generate a SWI, the request bit in IREQ is set by the following statement:

```
OR IREQ,#NUMBER
```

The immediate data variable, NUMBER, has a 1 in the bit position corresponding to the required level of SWI. For example, an SWI must be issued when an IREQ5 occurs. Bit 5 of NUMBER must have a value of 1.

```
OR IREQ, #00100000B
```

If the interrupt system is globally enabled, IREQ5 is enabled, and there are no higher priority requests pending, control is transferred to the service routine pointed to by the IREQ5 vector.

Note: Software may modify the IREQ register at any time. Care should be taken when using any instruction that modifies the IREQ register while interrupt sources are active. The software writeback always takes precedence over the hardware. If a software writeback takes place on the same cycle as an interrupt source tries to set an IREQ bit, the new interrupt is lost.

Nesting of Vectored Interrupts

Nesting vectored interrupts allows higher priority requests to interrupt a lower priority request. To initiate vectored interrupt nesting, perform the following steps during the interrupt service routine:

- PUSH the old IMASK on the stack
- Load IMASK with a new mask to disable lower priority interrupts
- Execute an EI instruction
- Proceed with interrupt processing
- Execute a DI instruction after processing is complete
- Restore the IMASK to its original value by POPing the previous mask from the stack
- Execute IRET

Depending on the application, some simplification of the above procedure may be possible.

RESET Conditions

The IMASK and IREQ registers initialize to 00h on RESET.

PROGRAMMABLE OPTIONS

EPROM Protect. When selecting the DISABLE EPROM PROTECT/ENABLE TESTMODE option, the user can read the software code in the program memory. ZiLOG's internal factory test mode, or any of the standard test mode methods, are useful for reading or verifying the code in the microcontroller when using an EPROM programmer. If the user should select the ENABLE EPROM PROTECT/DISABLE TESTMODE option, it is not possible to read the code using a tester, programmer, or any other standard method. As a result, ZiLOG is unable to test the EPROM memory at any time after customer delivery.

This option bit only affects the user's ability to read the code and has no effect on the operation of the part in an application. ZiLOG tests the EPROM memory before customer delivery whether or not the ENABLE EPROM PROTECT/DISABLE TESTMODE option is selected; ZiLOG provides a standard warranty for the part.

System Clock Source. When selecting the RC OSCILLATOR ENABLE option, the oscillator circuit on the microcontroller is configured to work with an external RC circuit. When selecting the Crystal/Other Clock Source option, the oscillator circuit is configured to work with an external crystal, ceramic resonator, or LC oscillator.

WATCH-DOG TIMER

The Watch-Dog Timer (WDT) is a retriggerable one-shot 16-bit timer that resets the device if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer time-out periods required in applications, the watch-dog timer is only updated every 64th clock cycle. When operating in the RUN or HALT modes, a WDT time-out reset is functionally equivalent to an interrupt vectoring the PC to 0020H, and setting the WDT flag to 1. Coming out of $\overline{\text{RESET}}$, the WDT is fully enabled with its time-out value set at minimum, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2h and C3h) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$ and when the device enters STOP mode.

The WDT instruction should be executed often enough to provide some margin of time to allow the WDT registers to approach 0. Because the WDT time-out periods are relatively long, a WDT $\overline{\text{RESET}}$ occurs in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

$\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT time-out sets the WDT flag, and the STOP instruction sets the SMR flag. This function enables software to determine whether a WDT time-out or a return from STOP mode occurred. Reading the WDT and SMR flags does not reset the flag to 0; therefore, the user must clear the flag via software.

Note: Failure to clear the SMR flag can result in unexpected behavior.

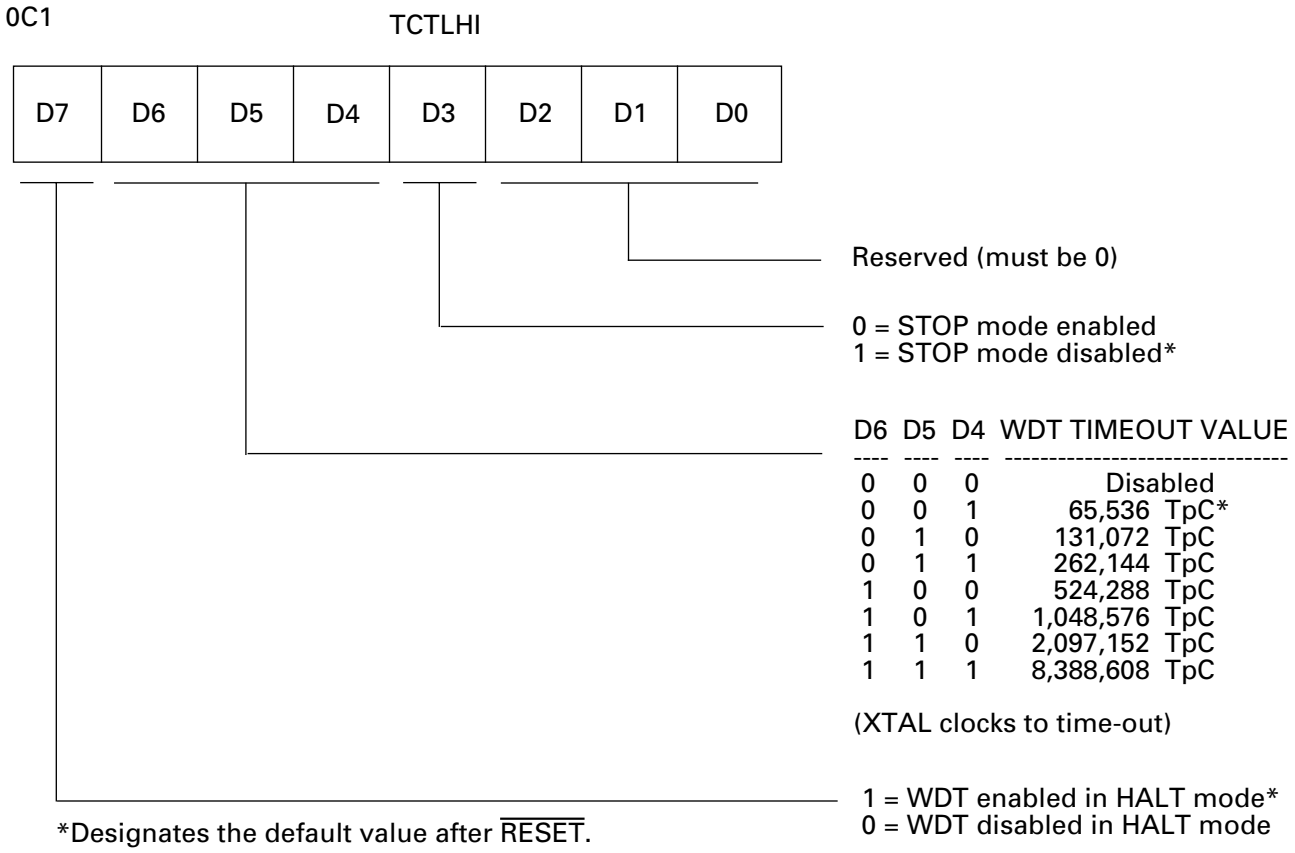

Figure 11. TCTLHI Register for Control of WDT

OSCILLATOR OPERATION

The Z8Plus MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

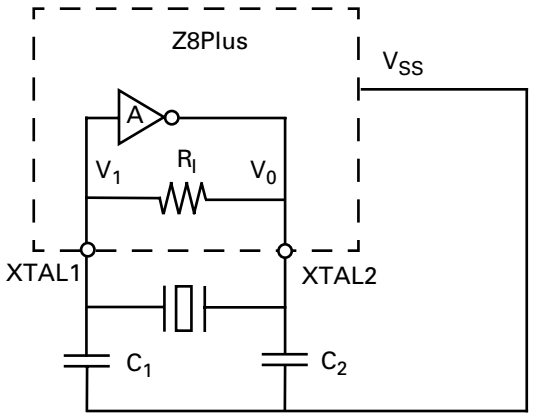

Figure 14. Pierce Oscillator with Internal Feedback Circuit

One drawback to the Pierce oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements. A x B = 1; where A = VO/VI is the gain of the amplifier, and B = VI/VO is the gain of the feedback element. The total phase shift around the loop is forced to 0 (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

Start-up time may be affected if C_1 and C_2 are increased dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it ceases to operate.

For fast and reliable oscillator start-up over the manufacturing process range, the load capacitors should be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8Plus oscillator pins should be as short and wide as possible to reduce parasitic inductance and resistance. The components (caps, the crystal, and resistors) should be placed as close as possible to the oscillator pins of the Z8Plus.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, and system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8Plus device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8Plus device V_{SS} (GND) pin. It should not be shared with any other system-ground trace or components except at the Z8Plus device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-Up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the C_1 and C_2 capacitors require reduction. The amplifier gain is either not adequate at frequency, or the crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

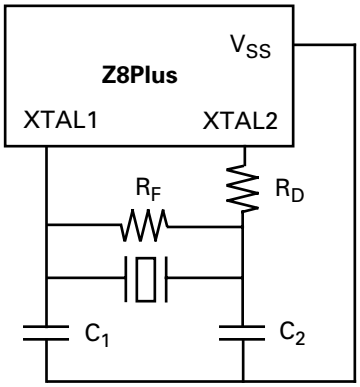

Figure 16. Crystal/Ceramic Resonator Oscillator

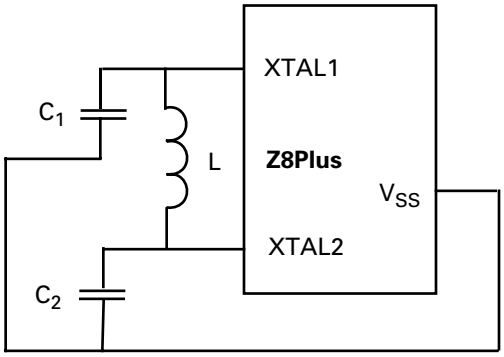

Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

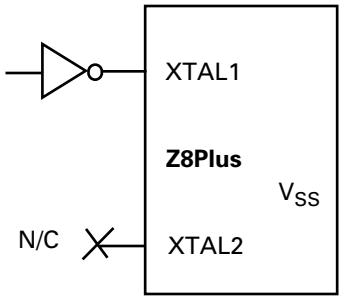

Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

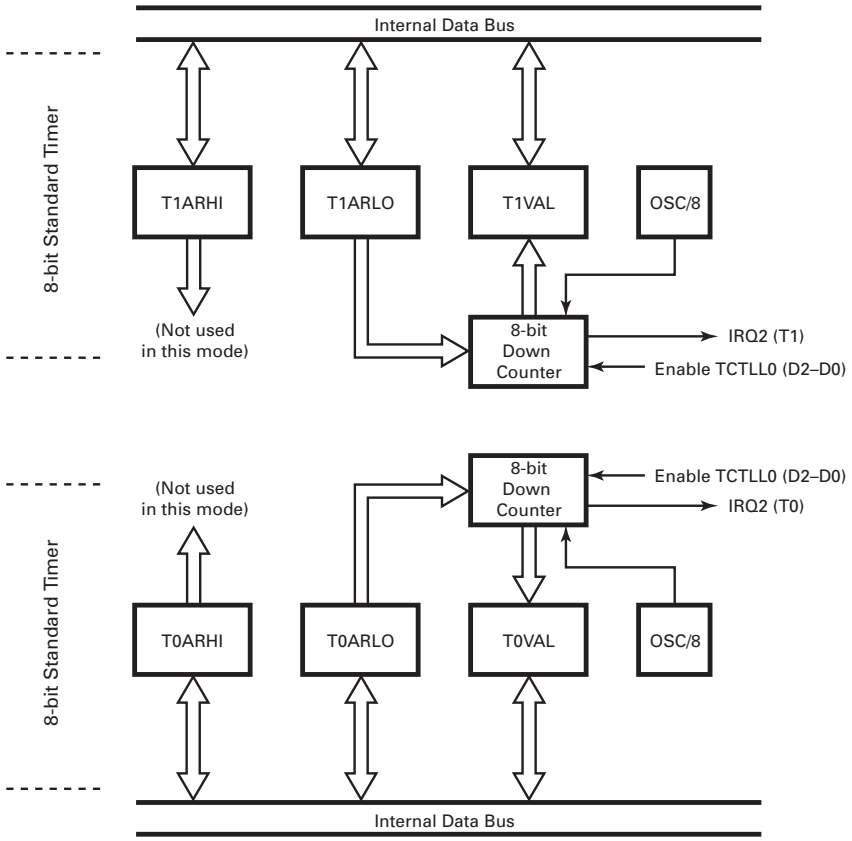

Figure 20. 8-Bit Standard Timers

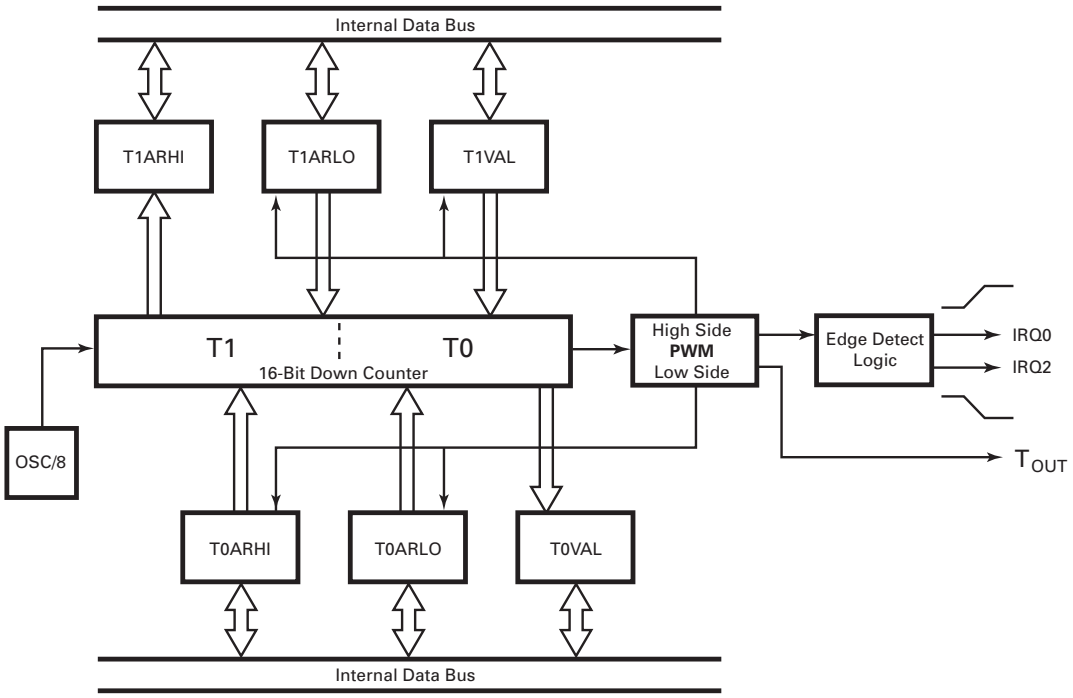

Figure 21. 16-Bit Standard PWM Timer

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

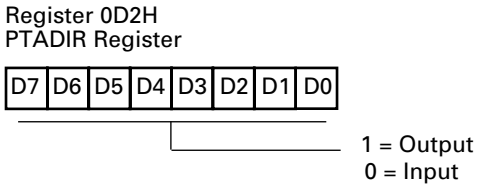

Figure 27. Port A Directional Control Register

PORT B

Port B Description

Port B is a 6-bit (bidirectional), CMOS-compatible I/O port. These six I/O lines can be configured under software control to be an input or output. Each bit is configured independently from the other bits. That is, one bit may be set to INPUT while another bit is set to OUTPUT.

In addition to standard input/output capability, five pins of Port B provide special functionality as indicated in Table 15.

Table 15. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	T0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

Special functionality is invoked via the Port B special function register. Port B, bit 5, is an open-drain-only pin when in output mode. There is no high-side driver on the output stage, nor is there any high-side protection device, because PB5 acts as the V_{PP} pin for EPROM programming mode. The user should always place an external protection diode on this pin. See Figure 32.

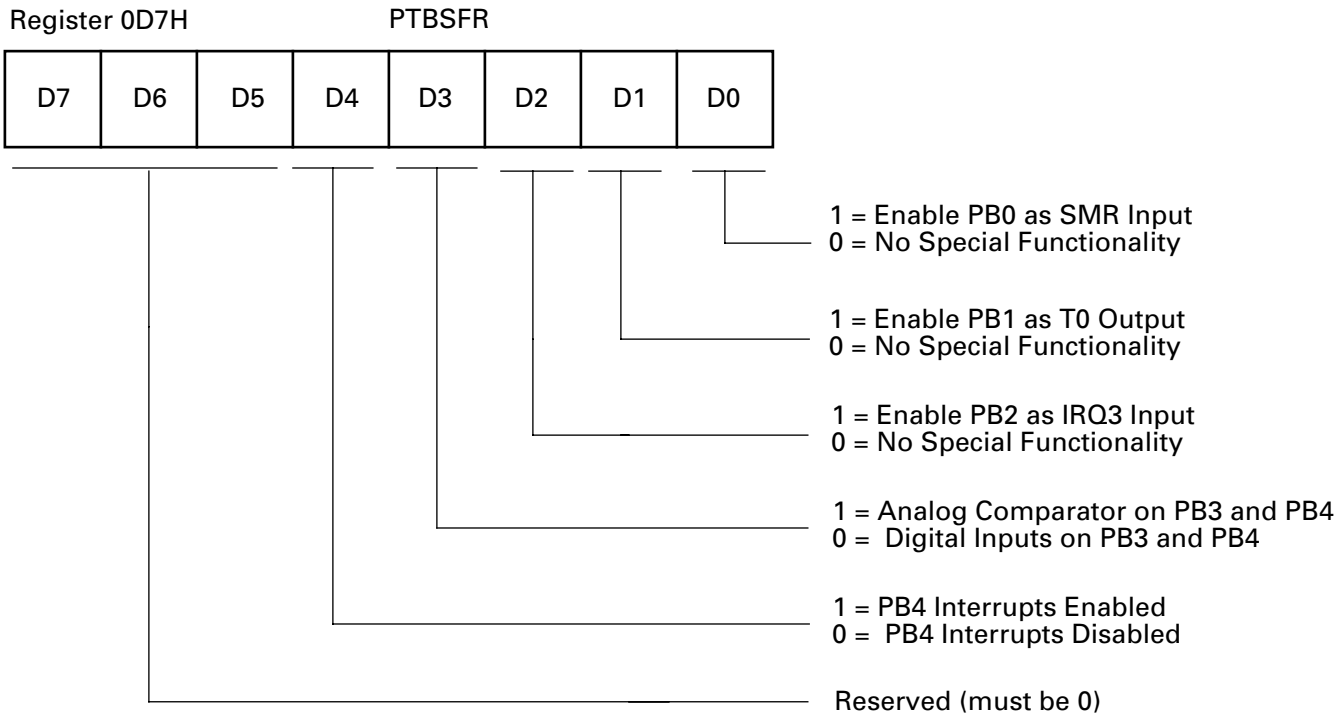

Figure 32. Port B Special Function Register

PORT B—PIN 2 CONFIGURATION

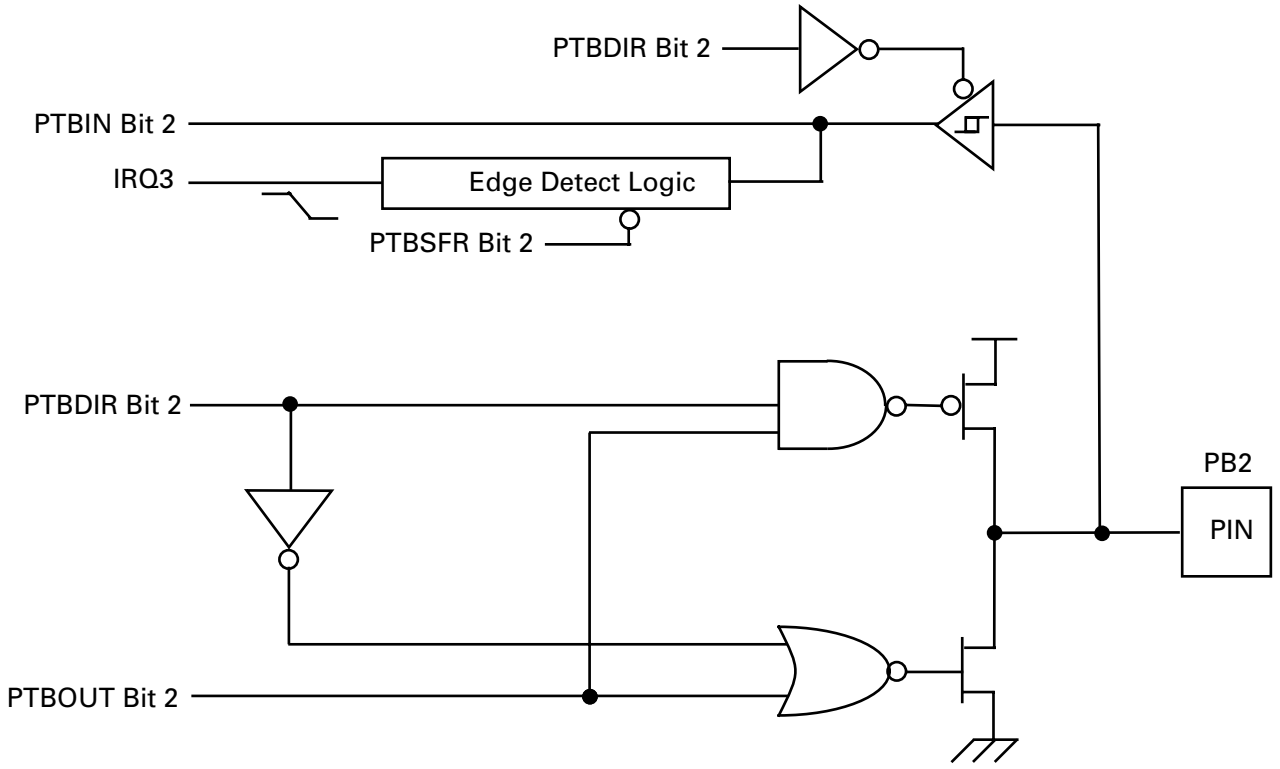

Figure 36. Port B Pin 2 Diagram

PORT B CONTROL REGISTERS

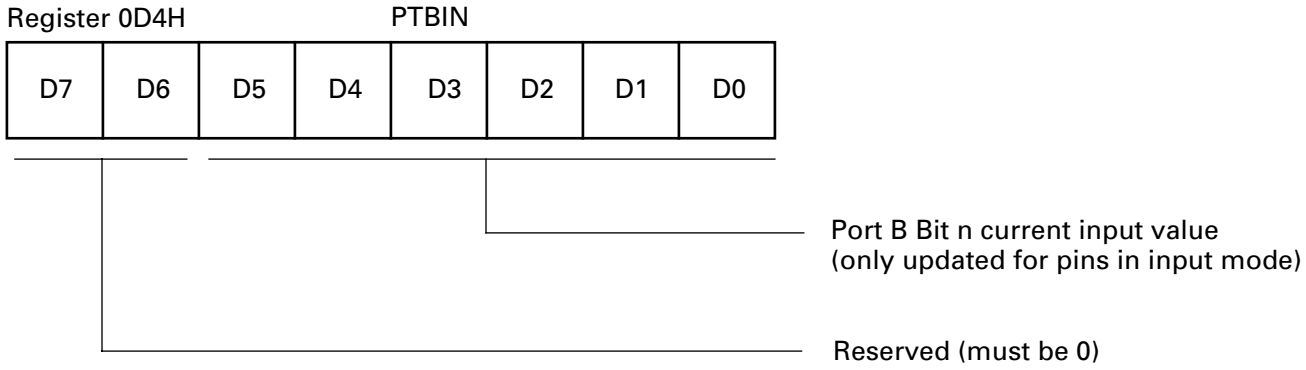

Figure 38. Port B Input Value Register

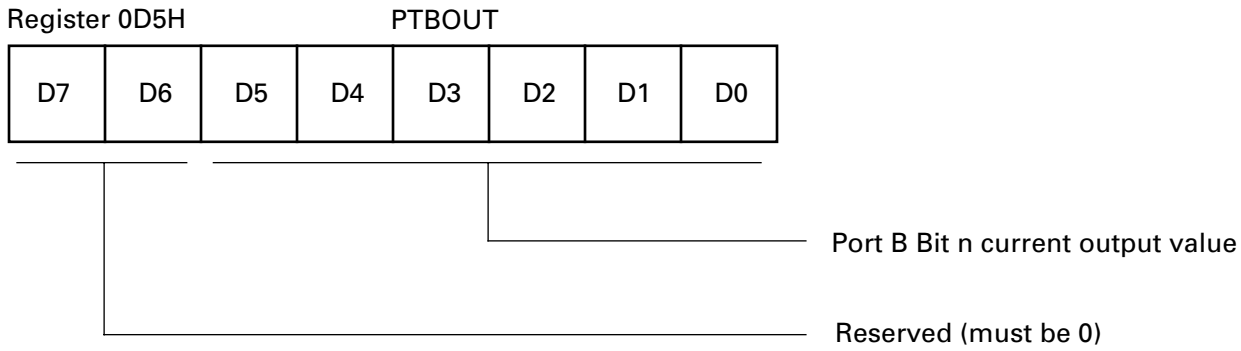

Figure 39. Port B Output Value Register

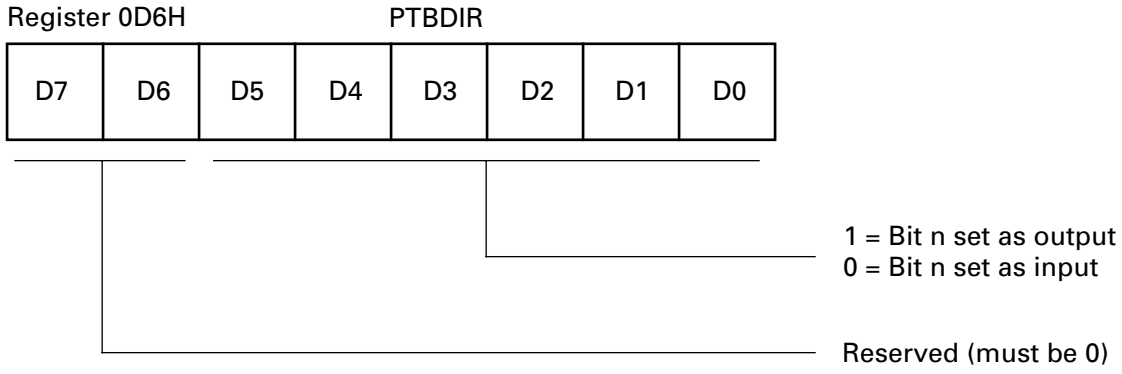

Figure 40. Port B Directional Control Register

PORT B CONTROL REGISTERS (Continued)

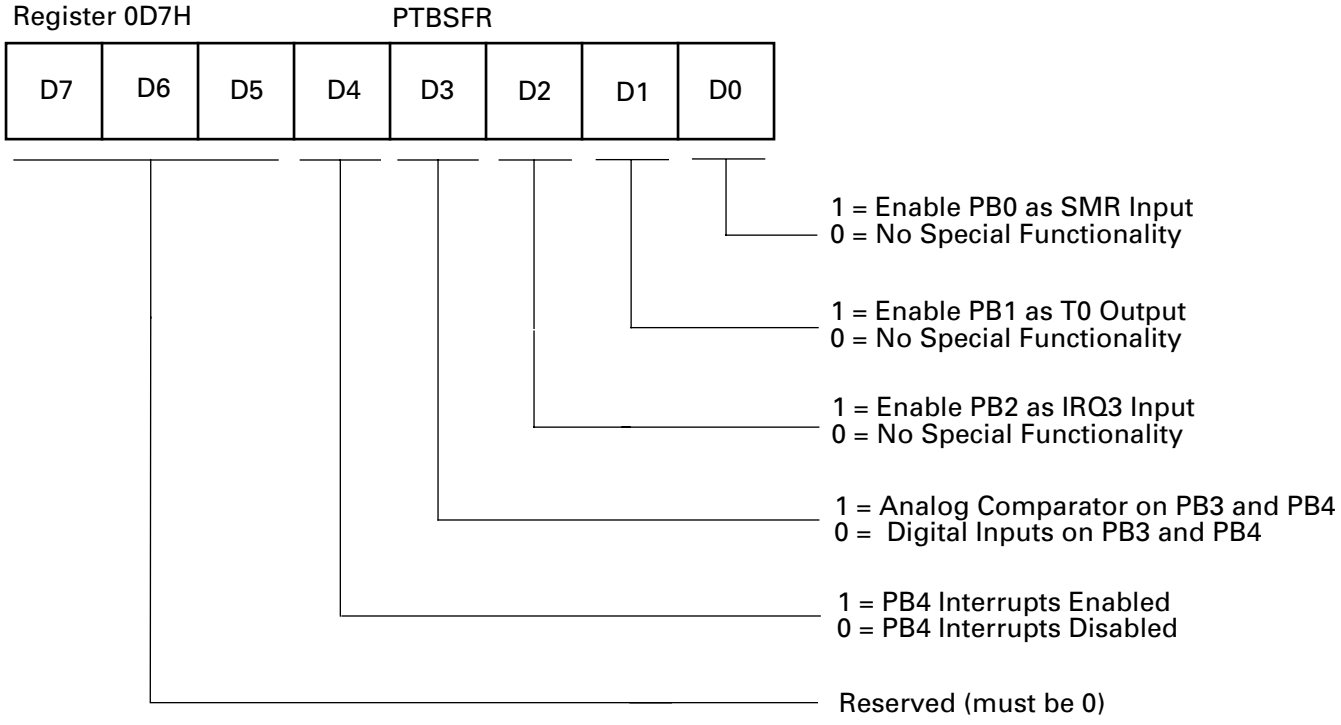

Figure 41. Port B Special Function Register

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

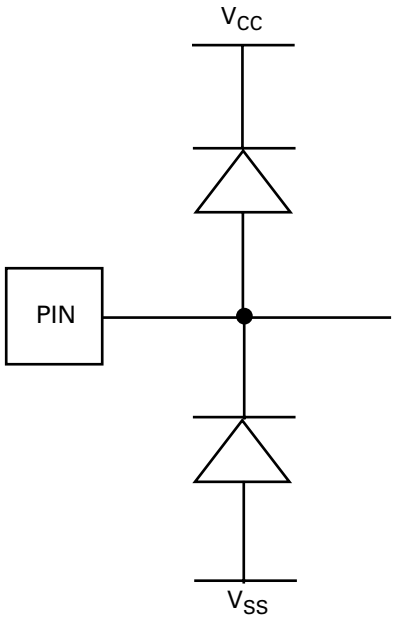

Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

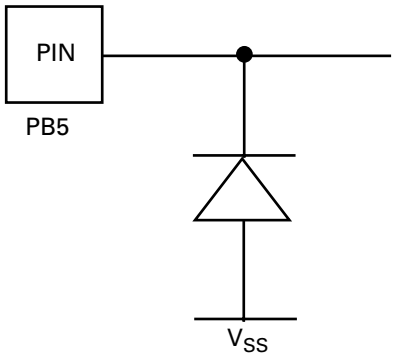

Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.