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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe002sz010sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

PB1 C PB2 C PB3 C PB4 C PB5 C PA7 C PA6 C PA5 C
PA4 🗆
PB3 C PB4 C PB5 C PA7 C PA6 C PA5 C PA4 C

Figure 3.	18-Pin	DIP/	SOIC	Pin	Identification
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Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7-PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3-PA0	Port A, Pins 3,2,1,0	Input/Output
14	V _{CC}	Power Supply	
15	V _{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

Table 1. Standard Programming Mode

PIN DESCRIPTION (Continued)

rigure 5. 20-Pin 550P Pin identification	Figure 5.	20-Pin	SSOP	Pin	Identification
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Table 3. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6	NC	No Connection	
7–10	PA7-PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3-PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V _{CC}	Power Supply	
17	V _{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	Input/Output





Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Pin #	Symbol	Function	Direction		
1	PGM	Program Mode	Input		
2–4	GND	Ground			
5	ADCLR/V _{PP}	Clear Clock/Program Voltage	Input		
6	NC	No Connection			
7–10	D7–D4	Data 7,6,5,4	Input/Output		
11–14	D3–D0	Data 3,2,1,0	Input/Output		
15	NC	No Connection			
16	V _{DD}	Power Supply			
17	GND	Ground			
18	NC	No Connection			
19	XTAL1	1-MHz Clock Input			
20	ADCLK	Address Clock Input			

Table 4. EPROM Programming Mode

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	-40	+105	С	
Storage Temperature	-65	+150	С	
Voltage on any Pin with Respect to V _{SS}	-0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V	
Voltage on PB5 Pin with Respect to V _{SS}	-0.6	V _{DD} +1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V _{SS}		40	mA	3
Maximum Allowable Current into V _{DD}		40	mA	3
Maximum Allowable Current into an Input Pin	-600	+600	μA	4
Maximum Allowable Current into an Open-Drain Pin	-600	+600	μA	5
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	3
Maximum Allowable Output Current Sourced by Port A		40	mA	3
Maximum Allowable Output Current Sunk by Port B		40	mA	3
Maximum Allowable Output Current Sourced by Port B		40	mA	3

Notes:

1. Applies to all pins except the PB5 pin and where otherwise noted.

2. There is no input protection diode from pin to $\ensuremath{V_{\text{DD}}}$.

3. Peak Current. Do not exceed 25mA average current in either direction.

4. Excludes XTAL pins.

5. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

 $\begin{array}{l} \mbox{Total Power Dissipation} &= V_{DD} \; x \; [I_{DD} - (sum \; of \; I_{OH})] \\ &+ sum \; of \; [(V_{DD} - V_{OH}) \; x \; I_{OH}] \\ &+ sum \; of \; (V_{OL} \; x \; I_{OL}) \end{array}$

T _A = −40°C to +105°C Extended Temperatures Typical ²											
Sym	Parameter	V _{CC} ¹	Min	Max	@ 25°C	Units	Conditions	Notes			
I _{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V _{IN} = 0V, V _{CC} @ 10 MHz	5,6			
		5.5V		2.0	1.0	mA	HALT mode V _{IN} = 0V, V _{CC} @ 10 MHz	5,6			
I _{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V _{IN} = 0V,V _{CC}	7			
		5.5V		700	250	nA	STOP mode V _{IN} = 0V,V _{CC}	7			

Table 6 DC Electrical Characteristics (Continued)

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V \pm 0.5V. 2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND. 3. For analog comparator input when analog comparator is enabled.

4. No protection diode is provided from the pin to V_{CC} . External protection is recommended.

5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.

6. CL1 = CL2 = 22 pF.

7. Same as note 5, except inputs are at V_{CC} .

The device is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 32 KB of program memory and 4 KB of RAM. Register RAM is accessed as either 8- or 16-bit registers using a combination of 4-, 8-, and 12-bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using 6 addressing modes. See the <u>Z8Plus User's Manual</u> for more information.

RESET

This section describes the Z8Plus reset conditions, reset timing, and register initialization procedures. Reset is generated by the Voltage Brown-Out/Power-On Reset (VBO/POR), Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8Plus device into a known state. To initialize the chip's internal logic, the POR device counts 64 internal clock cycles after the oscillator stabilizes. The control registers and ports are not reset to their default conditions after wakeup from a STOP mode or WDT time-out.

During **RESET**, the value of the program counter is 0020H. The I/O ports and control registers are configured to their default reset state. Resetting the device does not affect the contents of the general-purpose registers.

The **RESET** circuit initializes the control and peripheral registers, as shown in Table 8. Specific reset values are indicated by a 1 or a 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

Program execution starts 10 External Crystal (XTAL) clock cycles after the POR delay. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration This activity is followed by initialization of the remaining control registers.

	Bits										
Deviator (HEV)	Dogiotor Norro	7	c	F	4		2	1	•	Commente	
Register (REA)	Register Name	/	O	5	4	3	2		U		
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET.	
FE	Reserved										
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET.	
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET.	
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by RESET.	
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET.	
F9–F0	Reserved										
EF–E0	Virtual Copy									Virtual copy of the current working register set.	
DF–D8	Reserved										
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET.	
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET.	
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by RESET.	
Note: *The SMR	and WDT flags are se	t to in	ndica	te the	sou	rce of	the I	RESE	Ŧ.		

Table 8. Control and Peripheral Registers*



Figure 10. Reset Circuitry with POR, WDT, V_{BO} , and SMR

INTERRUPT SOURCES

Table 10 presents the interrupt types, sources, and vectors available in the Z8Plus. Other processors from the Z8Plus family may define the interrupts differently.

Name	Sources	Vector Location	Comments	Fixed Priority
IREQ ₀	Timer0 Time-out	2,3	Internal	1 (Highest)
IREQ ₁	PB4 High-to-Low Transition	4,5	External (PB4), Edge Triggered	2
IREQ ₂	Timer1 Time-out	6,7	Internal	3
IREQ ₃	PB2 High-to-Low Transition	8,9	External (PB2), Edge Triggered	4
IREQ ₄	PB4 Low-to-High Transition	A,B	External (PB4), Edge Triggered	5
IREQ ₅	Timer2 Time-out	C,D	Internal	6 (Lowest)
IREQ ₆ –IREQ ₁₅	Reserved		Reserved for future expansion	

Table 10. Interrupt Types, Sources, and Vectors

External Interrupt Sources

External sources can be generated by a transition on the corresponding port pin. The interrupt may detect a rising edge, a falling edge, or both.

Notes: The interrupt sources and trigger conditions are device dependent. See the device product specification to determine available sources (internal and external), triggering edge options, and exact programming details.

Although interrupts are edge triggered, minimum interrupt request Low and High times must be observed for proper operation. See the device product specification for exact timing requirements on external interrupt requests (T_WIL , T_WIH).

Internal Interrupt Sources

Internal interrupt sources and trigger conditions are device dependent. On-chip peripherals may set interrupt under various conditions. Some peripherals always set their corresponding IREQ bit while others must be specifically configured to do so.

See the device product specification to determine available sources, triggering edge options, and exact programming

details. For more details on the interrupt sources, refer to the chapters describing the timers, comparators, I/O ports, and other peripherals.

Interrupt Mask Register (IMASK) Initialization

The IMASK register individually or globally enables or disables the interrupts (Table 11). When bits 0 through 5 are set to 1, the corresponding interrupt requests are enabled. Bit 7 is the master enable bit and must be set before any of the individual interrupt requests can be recognized. Resetting bit 7 disables all the interrupt requests. Bit 7 is set and reset by the EI and DI instructions. It is automatically set to 0 during an interrupt service routine and set to 1 following the execution of an Interrupt Return (IRET) instruction. The IMASK registers are reset to 00h, disabling all interrupts.

Notes: It is not good programming practice to directly assign a value to the master enable bit. A value change should always be accomplished by issuing the EI and DI instructions.

Care should be taken not to set or clear IMASK bits while the master enable is set.

Table 11. Interrupt Mask Register—IMASK (FBh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate U = Undefined/ Undetermined								

Bit Position	R/W	Value	Description
7		0	Disables Interrupts
		1	Enables Interrupts
6		0	Reserved, must be 0
5		0	Disables IRQ5
		1	Enables IRQ5
4		0	Disables IRQ4
		1	Enables IRQ4
3		0	Disables IRQ3
		1	Enables IRQ3
2		0	Disables IRQ2
		1	Enables IRQ2
1		0	Disables IRQ1
		1	Enables IRQ1
0		0	Disables IRQ0
		1	Enables IRQ0

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Interrupt Request (IREQ) Register Initialization

IREQ (Table 12) is a register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt is issued, the corresponding bit position in the register is set to 1. Bits 0 to 5 are assigned to interrupt requests IREQ0 to IREQ5, respectively.

Whenever **RESET** is executed, the **IREO** resistor is set to 00h.

Table 12. Interrupt Request Register-IREQ (FAh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R = Read W = Write X = Indeterminate U = Undefined/ Undetermined

Bit	D /\\/	Value	Description
Position	n/ vv	value	Description
7	R/W	0	Reserved, must be 0
6	R/W	0	Reserved, must be 0
5	R/W	0	IRQ5 reset
		1	IRQ5 set
4	R/W	0	IRQ4 reset
		1	IRQ4 set
3	R/W	0	IRQ3 reset
		1	IRQ3 set
2	R/W	0	IRQ2 reset
		1	IRQ2 set
1	R/W	0	IRQ1 reset
		1	IRQ1 set
0	R/W	0	IRQ0 reset
		1	IRQ0 set

WATCH-DOG TIMER

The Watch-Dog Timer (WDT) is a retriggerable one-shot 16-bit timer that resets the device if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer time-out periods required in applications, the watch-dog timer is only updated every 64th clock cycle. When operating in the RUN or HALT modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H, and setting the WDT flag to 1. Coming out of **RESET**, the WDT is fully enabled with its time-out value set at minimum, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2h and C3h) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after **RESET** and when the device enters STOP mode.

The WDT instruction should be executed often enough to provide some margin of time to allow the WDT registers to approach 0. Because the WDT time-out periods are relatively long, a WDT $\overrightarrow{\text{RESET}}$ occurs in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag, and the STOP instruction sets the SMR flag. This function enables software to determine whether a WDT time-out or a return from STOP mode occurred. Reading the WDT and SMR flags does not reset the flag to 0; therefore, the user must clear the flag via software.

Note: Failure to clear the SMR flag can result in unexpected behavior.



Figure 11. TCTLHI Register for Control of WDT

The STOP mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP mode, the Z8Plus only requires a STOP instruction. It is *not* necessary to execute a NOP instruction immediately before the STOP instruction.

6F STOP ;enter STOP mode

The STOP mode is exited by any one of the following resets: POR or a Stop-Mode Recovery source. At reset generation, the processor always restarts the application program at address 0020H, and the STOP mode flag is set. Reading the STOP mode flag does not clear it. The user must clear the STOP mode flag with software.

Note: Failure to clear the STOP mode flag can result in undefined behavior.

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The Z8Plus provides a dedicated Stop-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin PB0 (I/O Port B, bit 0) triggers an SMR. To use this mode, pin PB0 must be configured as an input and the special function selected before the STOP mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM} . Program execution starts at address 20h, after the POR delay.

Notes: 1. The PB0 input, when used for Stop-Mode Recovery, does not initialize the control registers.

The STOP mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the device's operating range
- Output current sourcing is minimized
- All inputs (digital and analog) are at the Low or High rail voltages
- 2. For detailed information about flag settings, see the <u>Z8Plus User's Manual</u>.

OSCILLATOR OPERATION

The Z8Plus MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).



Figure 14. Pierce Oscillator with Internal Feedback Circuit

One drawback to the Pierce oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements. A \times B = 1; where A = VO/VI is the gain of the amplifier, and B = VI/VO is the gain of the feedback element. The total phase shift around the loop is forced to 0 (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1 , combined with the crystal resistance, provides an additional phase shift.

Start-up time may be affected if C_1 and C_2 are increased dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it ceases to operate.

For fast and reliable oscillator start-up over the manufacturing process range, the load capacitors should be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8Plus oscillator pins should be as short and wide as possible to reduce parasitic inductance and resistance. The components (caps, the crystal, and resistors) should be placed as close as possible to the oscillator pins of the Z8Plus.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC} , address/data lines, and system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8Plus device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8Plus device V_{SS} (GND) pin. It should not be shared with any other system-ground trace or components except at the Z8Plus device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-Up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the C_1 and C_2 capacitors require reduction. The amplifier gain is either not adequate at frequency, or the crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C₁ or C₂ should be made smaller, or a low-resistance crystal should be used.



Figure 20. 8-Bit Standard Timers



Figure 21. 16-Bit Standard PWM Timer







A pair of READ/WRITE registers is utilized for each 8-bit timer. One register is defined to contain the auto-initialization value for the timer. The second register contains the current value for the timer. When a timer is enabled, the timer decrements the value in its count register and continues decrementing until it reaches 0. An interrupt is generated, and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer stops counting when the value reaches 0. Control logic clears the appropriate control register bit to disable the timer. This operation is referred to as a *single-shot*. If auto-initialization is enabled, the timer counts from the initialization value. Software must not attempt to use timer registers for any other function.

User software is allowed to write to any WRITE register at any time; however, care should be taken if timer registers are updated while the timer is enabled. If software changes the count value while the timer is in operation, the timer continues counting from the updated value. **Note:** Unpredictable behavior can occur if the value updates at the same time that the timer reaches 0.

Similarly, if user software changes the initialization value register while the timer is active, the next time that the timer reaches 0, the timer initializes to the changed value.

Note: Unpredictable behavior can occur if the initialization value register is changed while the timer is in the process of being initialized.

The initialization value is determined by the exact timing of the WRITE operation. In all cases, the Z8Plus assigns a higher priority to the software WRITE than to a decrementer write-back. However, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software WRITE. A READ of either register can be conducted at any time, with no effect on the functionality of the timer. If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16bit timer. The interrupt for the combined timer is defined to be generated by timer T2 rather than T3. When a timer pair is specified to act as a single 16bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16bit timer, the auto-reload function is performed automatically.

All 16-bit timers continue counting while their interrupt requests are active and operate independently of each other.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt is responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the WRITE begin counting from the value in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source input only. Each enabled timer is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When **T01** is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it alternately initializes its count value using the Low auto-init pair, followed by the High auto-init pair. This functionality corresponds to a PWM. That is, the T1 interrupt defines the end of the High section of the waveform, and the T0 interrupt marks the end of the Low portion of the PWM waveform.

The PWM begins counting with whatever data is held in the count registers. After this value expires, the first reload depends on the state of the PB1 pin if T_{OUT} mode is selected. Otherwise, the Low value is applied first.

After the auto-initialization is completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt IRQ2 is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H; Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6; Figure 24) to configure PB1 for T_{OUT} operation for T0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 is capable of being a clock output for T0, toggling the PB1 output pin on each T0 timeout.

At end-of-count, the interrupt request line (IRQ0), clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when T0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, T0 is in Continuous Counting Mode, T_{OUT} exhibits a 50-percent duty cycle output. If the timer pair is selected (T01) as a PWM, the duty cycle depends on the High and Low reload values. At the end of each High time, PB1 toggles Low. At the end of each Low time, PB1 toggles HI.

RESET CONDITIONS

After a $\overline{\text{RESET}}$, the timers are disabled. See Table 8 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8Plus dedicates 14 lines to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide either standard input/output, or the following special functions: T0 output, comparator input, SMR input, and external interrupt inputs. All pins except PB5 include push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation. The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers (Figure 26).



Directional Control and Special Function Registers

Each port on the Z8Plus features a dedicated directional control register that determines (on a bit-wise basis) if a given port bit operates as input or output.

Each port on the Z8Plus features a special function register (SFR) that, in conjunction with the directional control register, implements (on a bit-by-bit basis) any special functionality that can be defined for each particular port bit.

Table 14. I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port features an Output Value Register and an input value register. For port bits configured as an input by means of the directional control register, the input value register

PORT B CONTROL REGISTERS













INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to $V_{\mbox{CC}}$ and $V_{\mbox{SS}}$ (Figure 43).



Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).



Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.



·	T						
SYMBOL		MILLIMETER		INCH			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	1.73	1.85	1.98	0.068	0.073	0.078	
A1	0.05	0.13	0.21	0.002	0.005	0.008	
A2	1.68	1.73	1.83	0.066	0.068	0.072	
8	0.25	0.30	0.38	0.010	0.012	0.015	
С	0.13	0.15	0.22	0.005	0.006	0.009	
D	7.07	7.20	7.33	0.278	0.283	0.289	
E	5.20	5.30	5.38	0.205	0.209	0.212	
e	0.65 TYP			0.0256 TYP			
н	7.65	7.80	7.90	0.301	0.307	0.311	
L	0.56	0.75	0.94	0.022	0.030	0.037	
Q1	0.74	0.78	0.82	0.029	0.031	0.032	

Figure 47. 20-Pin SSOP Package Diagram