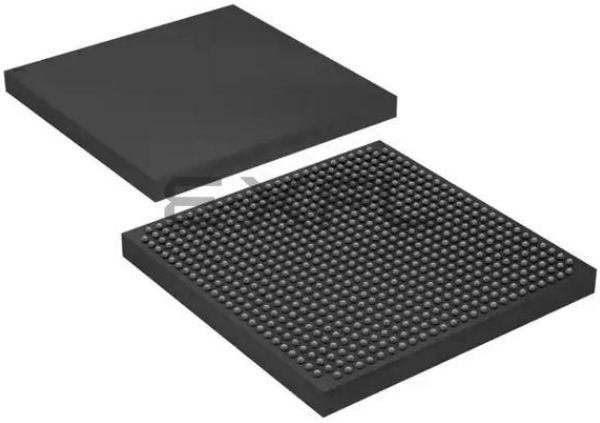

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

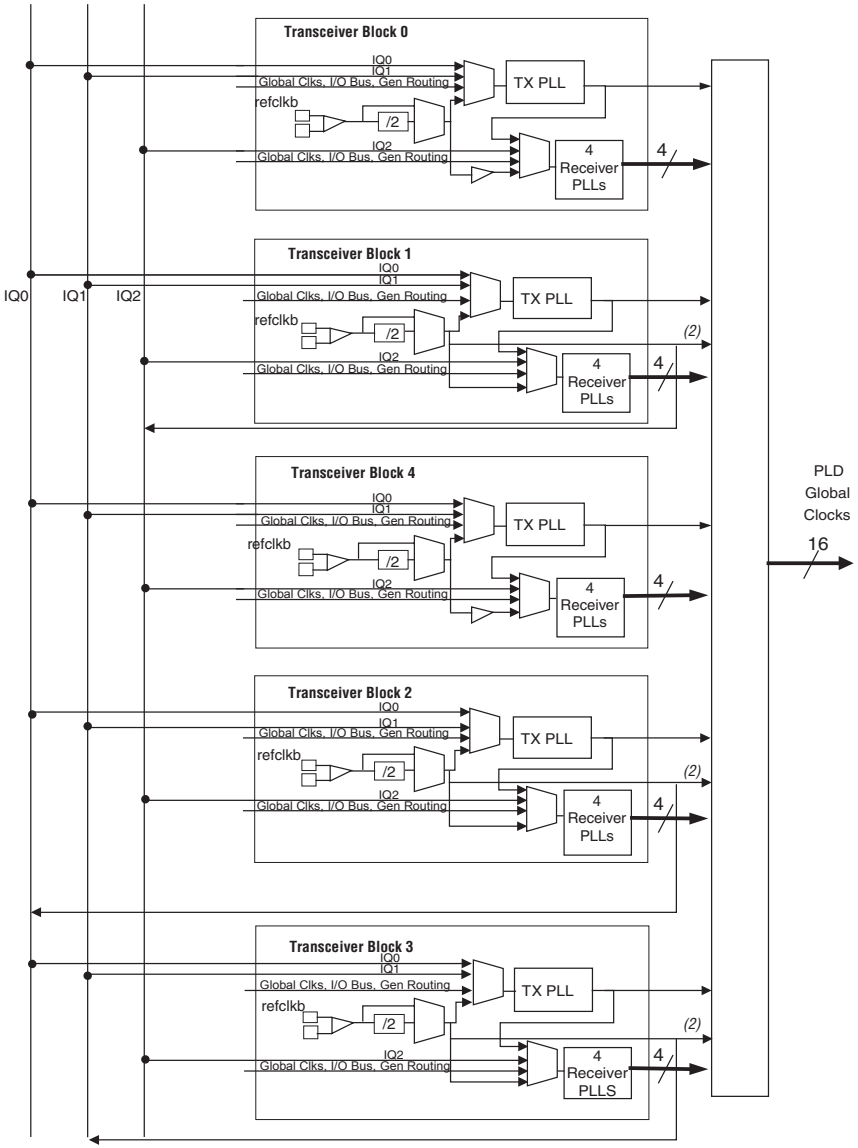
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1057 |
| Number of Logic Elements/Cells | 10570 |
| Total RAM Bits | 920448 |
| Number of I/O | 362 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1sgx10cf672c7 |

*Figure 2–27. EP1SGX40G Device Inter-Transceiver & Global Clock Connections* *Note (1)*




*Notes to Figure 2–27:*

(1) IQ lines are inter-transceiver block lines.

(2) If the /2 pre-divider is used, the path to drive the PLD logic array, local, or global clocks is not allowed.

(3) There are four receiver PLLs in each transceiver block.

*Figure 2–30. EP1SGX40 Receiver PLL Recovered Clock to Regional Clock Connection*

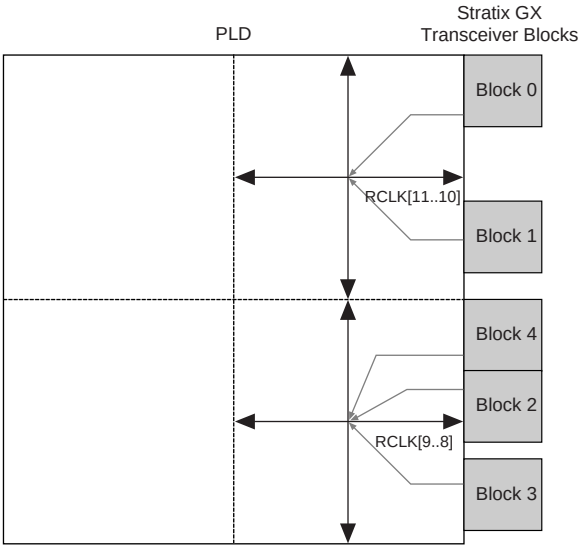
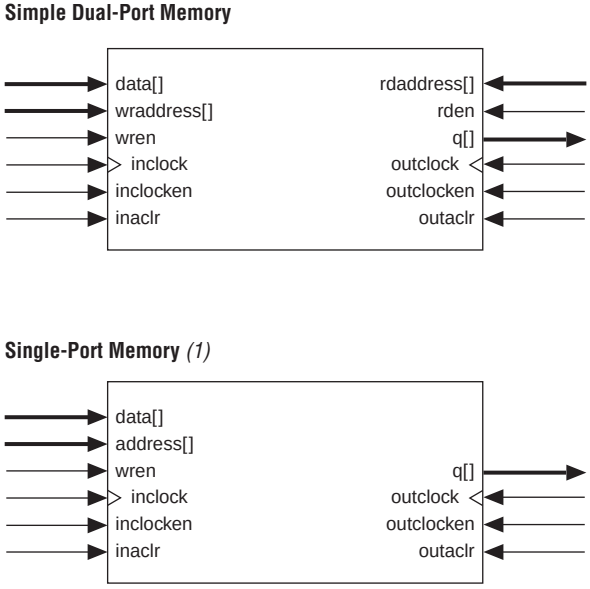



Figure 2–31 shows the possible recovered clock connection to the fast regional clock resource. The fast regional clocks can drive logic in their associated regions.

occurs or just read the don't care bits. Single-port memory supports non-simultaneous reads and writes, but the q[] port outputs the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see the *TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*. Figure 4–12 shows these different RAM memory port configurations for TriMatrix memory.

***Figure 4–12. Simple Dual-Port & Single-Port Memory Configurations***




***Note to Figure 4–12:***

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (WREN) signal derived from the global

single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix GX devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

### *M512 RAM Block*

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 512 × 1, 256 × 2, 128 × 4, 64 × 8 (64 × 9 bits with parity), and 32 × 16 (32 × 18 bits with parity). Mixed-width configurations are also possible, allowing different read and write widths. Table 4–3 summarizes the possible M512 RAM block configurations.

*Table 4–3. M512 RAM Block Configurations (Simple Dual-Port RAM)*

| Read Port | Write Port | | | | | | |
|---|---|---|---|---|---|---|---|
| | 512 × 1 | 256 × 2 | 128 × 4 | 64 × 8 | 32 × 16 | 64 × 9 | 32 × 18 |
| 512 × 1 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 256 × 2 | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| 128 × 4 | ✓ | ✓ | ✓ | | ✓ | | |
| 64 × 8 | ✓ | ✓ | | ✓ | | | |
| 32 × 16 | ✓ | ✓ | ✓ | | ✓ | | |
| 64 × 9 | | | | | | ✓ | |
| 32 × 18 | | | | | | | ✓ |

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

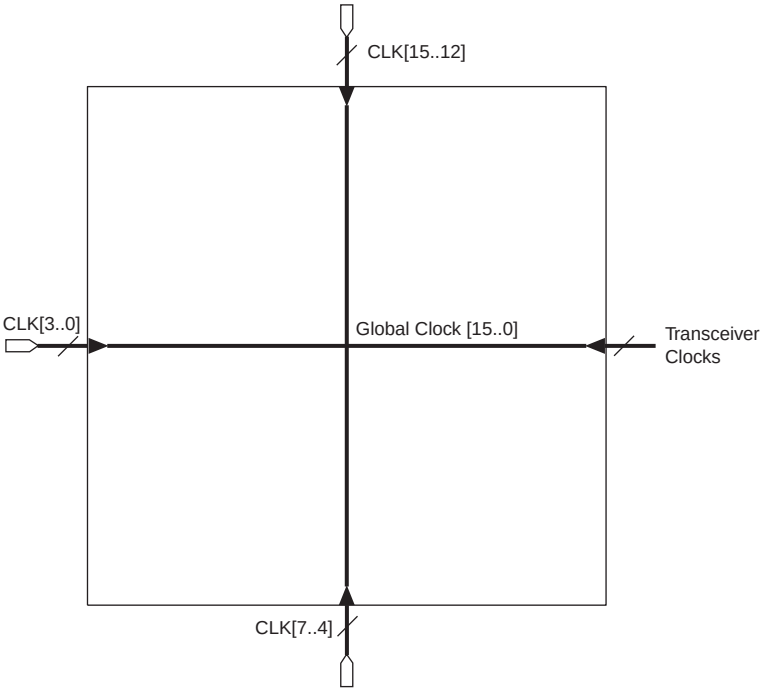
The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 4–96 for details on dedicated SERDES in Stratix GX devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, `inclr`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 4–14 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix GX devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 4–15 shows the M512 RAM block to logic array interface.

blocks facing to the left, and another 10 possible from the right adjacent LABs for M-RAM blocks facing to the right. For column interfacing, every M-RAM column unit connects to the right and left column lines, allowing each M-RAM column unit to communicate directly with three columns of LABs. Figures 4–20 through 4–22 show the interface between the M-RAM block and the logic array.

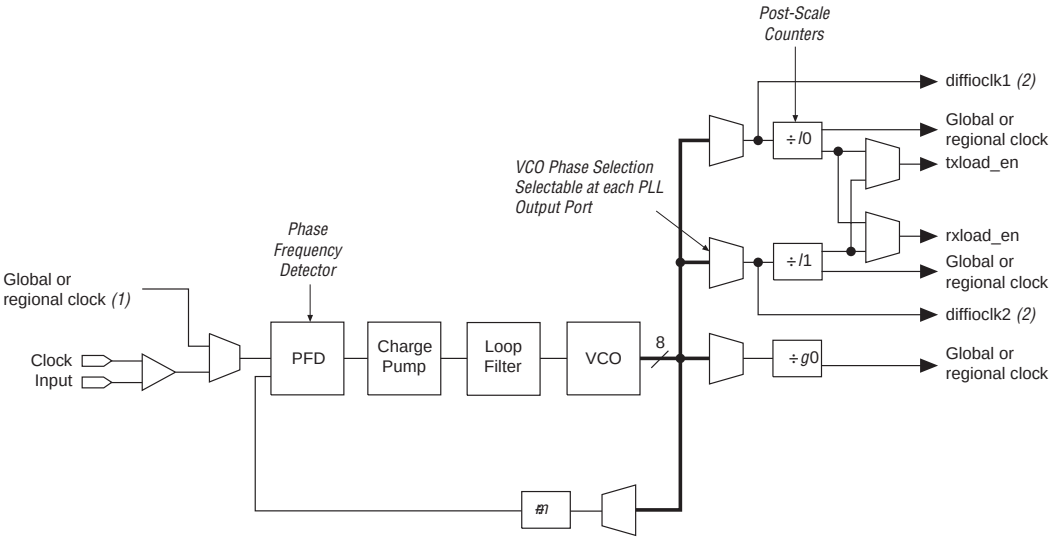
*Figure 4–41. Global Clock Resources*




### *Regional Clock Network*

There are four regional clock networks RCLK[3..0] within each quadrant of the Stratix GX device that are driven by the same dedicated CLK[7..0] and CLK[15..12] input pins, PLL outputs, or transceiver clocks. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 4–42.

*Figure 4–57. Stratix GX Device Fast PLL*




*Notes to Figure 4–57:*

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

### *Clock Multiplication & Division*

The Stratix GX device's fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

### *External Clock Outputs*

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output

*Table 6–18. PCI-X Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IPU}$ | Input pull-up voltage | | 0.7 × $V_{CCIO}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 × $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 × $V_{CCIO}$ | V |

*Table 6–19. GTL+ I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Termination voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{REF}$ | Reference voltage | | 0.88 | 1.0 | 1.12 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.1 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 36 mA *(1)* | | | 0.65 | V |

*Table 6–20. GTL I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Termination voltage | | 1.14 | 1.2 | 1.26 | V |
| $V_{REF}$ | Reference voltage | | 0.74 | 0.8 | 0.86 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.05 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.05 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 40 mA *(1)* | | | 0.4 | V |

*Table 6–21. SSTL-18 Class I Specifications (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $V_{REF}$ | Reference voltage | | 0.8 | 0.9 | 1.0 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.125 | | | V |

*Table 6–21. SSTL-18 Class I Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IL(DC)}$ | Low-level DC input voltage | | | | $V_{REF}$ – 0.125 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.275 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.275 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –6.7 mA *(1)* | $V_{TT}$ + 0.475 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 6.7 mA *(1)* | | | $V_{TT}$ – 0.475 | V |

*Table 6–22. SSTL-18 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $V_{REF}$ | Reference voltage | | 0.8 | 0.9 | 1.0 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.125 | | | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | | | $V_{REF}$ – 0.125 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.275 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.275 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –13.4 mA *(1)* | $V_{TT}$ + 0.630 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 13.4 mA *(1)* | | | $V_{TT}$ – 0.630 | V |

*Table 6–23. SSTL-2 Class I Specifications (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.18 | | 3.0 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |

| Table 6–38. DSP Block Internal Timing Microparameter Descriptions | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{SU}$ | Input, pipeline, and output register setup time before clock |
| $t_{H}$ | Input, pipeline, and output register hold time after clock |
| $t_{CO}$ | Input, pipeline, and output register clock-to-output delay |
| $t_{INREG2PIPE9}$ | Input register to DSP block pipeline register in 9 × 9-bit mode |
| $t_{INREG2PIPE18}$ | Input register to DSP block pipeline register in 18 × 18-bit mode |
| $t_{PIPE2OUTREG2ADD}$ | DSP block pipeline register to output register delay in two-multipliers adder mode |
| $t_{PIPE2OUTREG4ADD}$ | DSP Block Pipeline Register to output register delay in four-multipliers adder mode |
| $t_{PD9}$ | Combinational input to output delay for 9 × 9-bit mode |
| $t_{PD18}$ | Combinational input to output delay for 18 × 18-bit mode |
| $t_{PD36}$ | Combinational input to output delay for 36 × 36-bit mode |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

| Table 6–39. M512 Block Internal Timing Microparameter Descriptions | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{M512RC}$ | Synchronous read cycle time |
| $t_{M512WC}$ | Synchronous write cycle time |
| $t_{M512WERESU}$ | Write or read enable setup time before clock |
| $t_{M512WEREH}$ | Write or read enable hold time after clock |
| $t_{M512DATASU}$ | Data setup time before clock |
| $t_{M512DATAH}$ | Data hold time after clock |
| $t_{M512WADDRSU}$ | Write address setup time before clock |
| $t_{M512WADDRH}$ | Write address hold time after clock |
| $t_{M512RADDRSU}$ | Read address setup time before clock |
| $t_{M512RADDRH}$ | Read address hold time after clock |
| $t_{M512DATACO1}$ | Clock-to-output delay when using output registers |
| $t_{M512DATACO2}$ | Clock-to-output delay without output registers |
| $t_{M512CLKHL}$ | Minimum clock high or low time |
| $t_{M512CLR}$ | Minimum clear pulse width |

*Table 6–47. M512 Block Internal Timing Microparameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M512RC}$ | | 3,340 | | 3,816 | | 4,387 | ps |
| $t_{M512WC}$ | | 3,318 | | 3,590 | | 4,128 | ps |
| $t_{M512WERESU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512WERH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512DATASU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512DATAH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512WADDRASU}$ | 110 | | 123 | | 141 | | ps |
| $t_{M512WADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M512DATACO1}$ | | 424 | | 472 | | 541 | ps |
| $t_{M512DATACO2}$ | | 3,366 | | 3,846 | | 4,421 | ps |
| $t_{M512CLKHL}$ | 150 | | 167 | | 192 | | ps |
| $t_{M512CLR}$ | 170 | | 189 | | 217 | | ps |

*Table 6–48. M4K Block Internal Timing Microparameters (Part 1 of 2)*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{M4KRC}$ | | 3,807 | | 4,320 | | 4,967 | ps |
| $t_{M4KWC}$ | | 2,556 | | 2,840 | | 3,265 | ps |
| $t_{M4KWERESU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KWERH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KDATASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KDATAH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KWADDRASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KWADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KRADDRASU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KRADDRH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KDATABSU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KDATABH}$ | 34 | | 38 | | 43 | | ps |
| $t_{M4KADDRBSU}$ | 131 | | 149 | | 171 | | ps |
| $t_{M4KADDRBH}$ | 34 | | 38 | | 43 | | ps |

| Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INHPLL}$ | Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting | |
| $t_{OUTCOPLL}$ | Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting | $C_{LOAD}$ = 10 pF |

*Notes to Table 6–53:*
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

| Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-5 Speed Grade** | | **-6 Speed Grade** | | **-7 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{INSU}$ | 2.245 | | 2.332 | | 2.666 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.597 | 2.000 | 4.920 | 2.000 | 5.635 | ns |

| Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-5 Speed Grade** | | **-6 Speed Grade** | | **-7 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{INSU}$ | 2.114 | | 2.218 | | 2.348 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.728 | 2.000 | 5.078 | 2.000 | 6.004 | ns |
| $t_{INSUPLL}$ | 1.035 | | 0.941 | | 1.070 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.629 | 0.500 | 2.769 | 0.500 | 3.158 | ns |

*Table 6–59. EP1SGX10 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{OUTCO}$ | 2.000 | 5.231 | 2.000 | 5.293 | 2.000 | 5.822 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.804 | 0.500 | 2.627 | 0.500 | 2.765 | ns |

Tables 6–60 through 6–65 show the external timing parameters on column and row pins for EP1SGX25 devices.

*Table 6–60. EP1SGX25 Column Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.418 | | 2.618 | | 3.014 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.524 | 2.000 | 4.834 | 2.000 | 5.538 | ns |

*Table 6–61. EP1SGX25 Column Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.713 | | 1.838 | | 2.069 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.229 | 2.000 | 5.614 | 2.000 | 6.432 | ns |
| $t_{INSUPLL}$ | 1.061 | | 1.155 | | 1.284 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.661 | 0.500 | 2.799 | 0.500 | 3.195 | ns |

*Table 6–68. EP1SGX40 Column Pin Global Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.033 | | 2.184 | | 2.451 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 5.689 | 2.000 | 6.116 | 2.000 | 7.010 | ns |
| $t_{INSUPLL}$ | 1.228 | | 1.278 | | 1.415 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.594 | 0.500 | 2.732 | 0.500 | 3.113 | ns |

*Table 6–69. EP1SGX40 Row Pin Fast Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.450 | | 2.662 | | 3.046 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.880 | 2.000 | 5.241 | 2.000 | 6.004 | ns |

*Table 6–70. EP1SGX40 Row Pin Regional Clock External I/O Timing Parameters*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.398 | | 2.567 | | 2.938 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.000 | 4.932 | 2.000 | 5.336 | 2.000 | 6.112 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |

*Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 1 of 2)*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.965 | | 2.128 | | 2.429 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | ns |

*Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)*

| Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| 2.5-V LVTTL | 2 mA | | 830 | | 872 | | 1,002 | ps |
| | 8 mA | | 250 | | 263 | | 302 | ps |
| | 12 mA | | 140 | | 147 | | 169 | ps |
| | 16 mA | | 100 | | 105 | | 120 | ps |
| 1.8-V LVTTL | 2 mA | | 1,510 | | 1,586 | | 1,824 | ps |
| | 8 mA | | 420 | | 441 | | 507 | ps |
| | 12 mA | | 350 | | 368 | | 423 | ps |
| 1.5-V LVTTL | 2 mA | | 1,740 | | 1,827 | | 2,101 | ps |
| | 4 mA | | 1,160 | | 1,218 | | 1,400 | ps |
| | 8 mA | | 690 | | 725 | | 833 | ps |
| CTT | | | 50 | | 53 | | 61 | ps |
| SSTL-3 class I | | | 90 | | 95 | | 109 | ps |
| SSTL-3 class II | | | –50 | | –52 | | –60 | ps |
| SSTL-2 class I | | | 100 | | 105 | | 120 | ps |
| SSTL-2 class II | | | 20 | | 21 | | 24 | ps |
| LVDS *(1)* | | | –20 | | –21 | | –24 | ps |
| LVPECL *(1)* | | | 40 | | 42 | | 48 | ps |
| PCML *(1)* | | | –60 | | –63 | | –73 | ps |
| HyperTransport Technology *(1)* | | | 70 | | 74 | | 85 | ps |

*Table 6–76. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)*

| I/O Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 1,911 | | 2,011 | | 2,312 | ps |
| | 4 mA | | 1,911 | | 2,011 | | 2,312 | ps |
| | 8 mA | | 1,691 | | 1,780 | | 2,046 | ps |
| | 12 mA | | 1,471 | | 1,549 | | 1,780 | ps |
| | 24 mA | | 1,341 | | 1,412 | | 1,623 | ps |

*Table 6–85. Stratix GX Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2] Pins (Part 2 of 2)*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Unit |
|---|---|---|---|---|
| 1.5 V | 350 | 300 | 300 | MHz |
| LVCMOS | 400 | 350 | 300 | MHz |
| GTL | 200 | 167 | 125 | MHz |
| GTL+ | 200 | 167 | 125 | MHz |
| SSTL-3 class I | 167 | 150 | 133 | MHz |
| SSTL-3 class II | 167 | 150 | 133 | MHz |
| SSTL-2 class I | 150 | 133 | 133 | MHz |
| SSTL-2 class II | 150 | 133 | 133 | MHz |
| SSTL-18 class I | 150 | 133 | 133 | MHz |
| SSTL-18 class II | 150 | 133 | 133 | MHz |
| HSTL class I | 250 | 225 | 200 | MHz |
| HSTL class II | 225 | 225 | 200 | MHz |
| 3.3-V PCI | 250 | 225 | 200 | MHz |
| 3.3-V PCI-X 1.0 | 225 | 225 | 200 | MHz |
| Compact PCI | 400 | 350 | 300 | MHz |
| AGP 1× | 400 | 350 | 300 | MHz |
| AGP 2× | 400 | 350 | 300 | MHz |
| CTT | 300 | 250 | 200 | MHz |
| Differential HSTL | 225 | 225 | 200 | MHz |
| LVDS | 717 | 717 | 500 | MHz |
| LVPECL | 717 | 717 | 500 | MHz |
| PCML | 420 | 420 | 420 | MHz |
| HyperTransport technology | 420 | 420 | 420 | MHz |

## High-Speed I/O Specification

Table 6–86 provides high-speed timing specifications definitions.

*Table 6–86. High-Speed Timing Specifications & Definitions (Part 1 of 2)*

| High-Speed Timing Specification | Definitions |
|---|---|
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| $f_{HSCLK}$ | High-speed receiver/transmitter input and output clock frequency. |
| $t_{RISE}$ | Low-to-high transmission time. |

*Table 6–89. Enhanced PLL Specifications for -6 Speed Grades (Part 2 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency for internal global or regional clock | 0.3 | | 450 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(2)* | 0.3 | | 500 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Period jitter for external clock output *(5)* | | | ±100 ps for >200 MHz `outclk`<br>±20 mUI for <200 MHz `outclk` | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* *(10)* | *(8)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration *(10)* | 10 | | 400 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 800 *(7)* | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(9)* | 0.4 | 0.5 | 0.6 | % |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | | | ns |

*Table 6–90. Enhanced PLL Specifications for -7 Speed Grade (Part 1 of 3)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 565 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock period jitter | | | ±200 *(2)* | ps |
| $t_{EINJITTER}$ | External feedback clock period jitter | | | ±200 *(2)* | ps |

Table 6–91 describes the Stratix GX device fast PLL specifications.

*Table 6–91. Fast PLL Specifications for -5 & -6 Speed Grade Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | CLKIN frequency (for *m* = 1) *(1)* | 300 | 717 | MHz |
| | CLKIN frequency (for *m* = 2 to 19) | 300/*m* | 1,000/*m* | MHz |
| | CLKIN frequency (for *m* = 20 to 32) | 10 | 1,000/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(2)* | 9.4 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock | 9.375 | 717 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 1,000 | MHz |
| $t_{INDUTY}$ | CLKIN duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Period jitter for CLKIN pin | | ±200 | ps |
| $t_{DUTY}$ | Duty cycle for DFFIO 1× CLKOUT pin *(3)* | 45 | 55 | % |
| $t_{JITTER}$ | Period jitter for DIFFIO clock out *(3)* | | ±80 | ps |
| | Period jitter for internal global or regional clock | | ±100 ps for >200-MHz outclk<br>±20 mUI for <200-MHz outclk | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(3)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(4)*, *(5)* | 1 | 32 | Integer |
| $t_{ARESET}$ | Minimum pulse width on areset signal | 10 | | ns |

*Table 6–92. Fast PLL Specifications for -7 & -8 Speed Grades (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | CLKIN frequency (for *m* = 1) *(1)*, | 300 | 640 | MHz |
| | CLKIN frequency (for *m* = 2 to 19) | 300/*m* | 700/*m* | MHz |
| | CLKIN frequency (for *m* = 20 to 32) | 10 | 700/*m* | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(2)* | 9.375 | 420 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock | 9.4 | 500 | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 700 | MHz |
| $t_{INDUTY}$ | CLKIN duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Period jitter for CLKIN pin | | ±200 | ps |