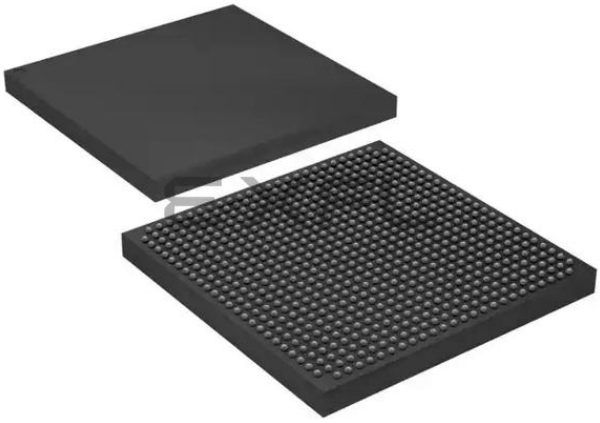

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

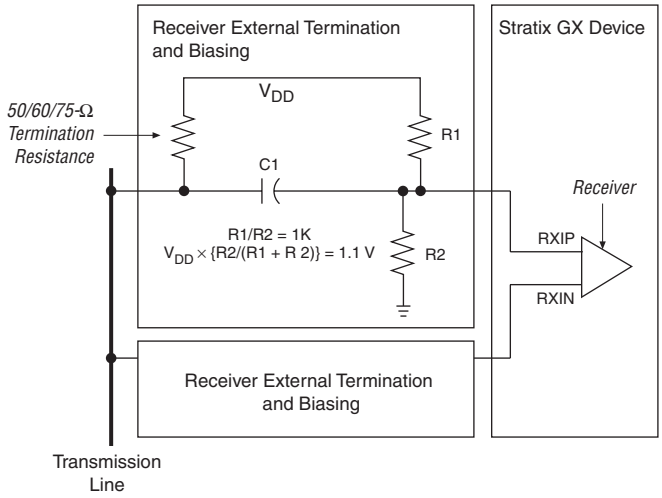
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	362
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx10df672c5

Figure 2–12. External Termination & Biasing Circuit



Programmable Equalizer

The programmable equalizer module boosts the high frequency components of the incoming signal to compensate for losses in the transmission medium. There are five possible equalization settings (0, 1, 2, 3, 4) to compensate for 0", 10", 20", 30", and 40" of FR4 trace. These settings should be interpreted loosely. The programmable equalizer can be set dynamically or statically.

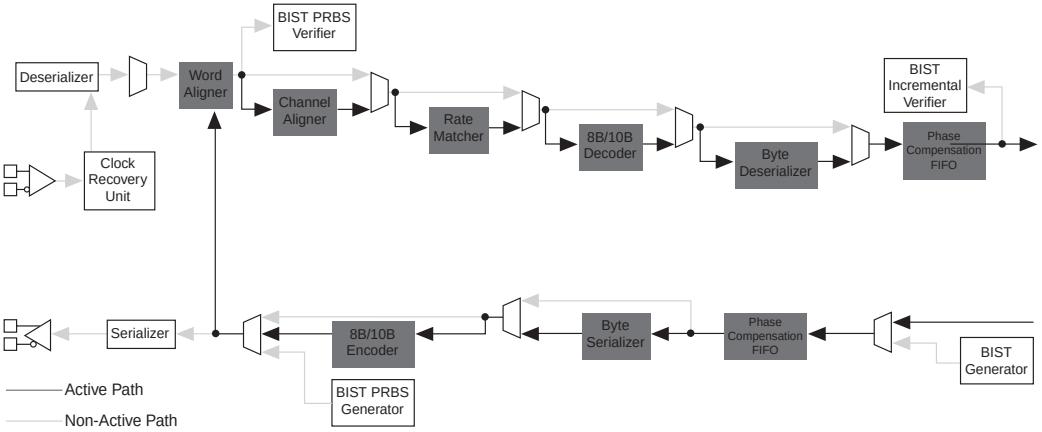
Receiver PLL & CRU

Each transceiver block has four receiver PLLs and CRUs, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, then the receiver PLL or CRU is powered down for the channel. Figure 2–13 is a diagram of the receiver PLL and CRU circuits.

Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not use in the loopback path. The received data is not retimed. Figure 2–22 shows the data path in parallel loopback mode. This option is not dynamically switchable. Reception of an external signal is not possible in this mode.

Figure 2–22. Data Path in Parallel Loopback Mode



Reverse Serial Loopback

The reverse serial loopback exercises the analog portion of the transceiver. This loopback mode is dynamically switchable through the `tx_srlpbk` port on a channel by channel basis. Asserting `rxanalogreset` in reverse serial loopback mode powers down the receiver buffer and CRU, preventing data loopback. Figure 2–23 shows the data path in reverse serial loopback mode.

Figure 2–24. BIST PRBS Data Path

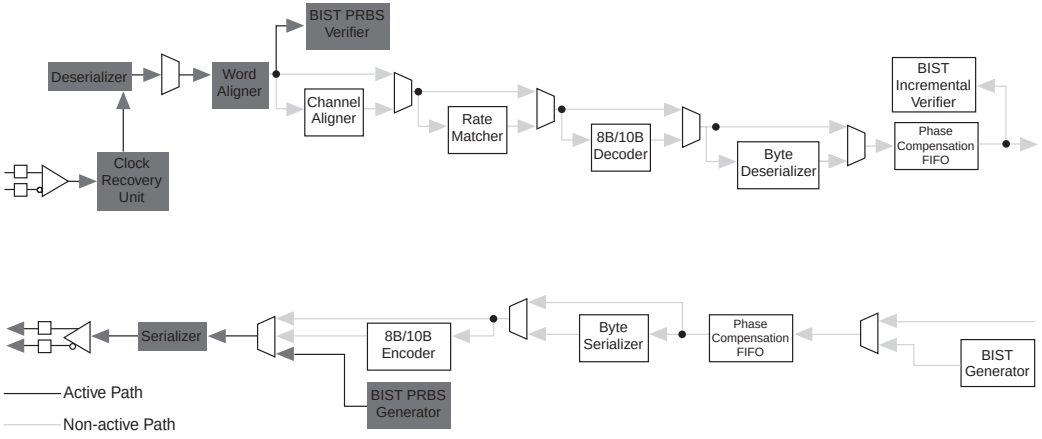


Figure 2–25. BIST Incremental Data Path

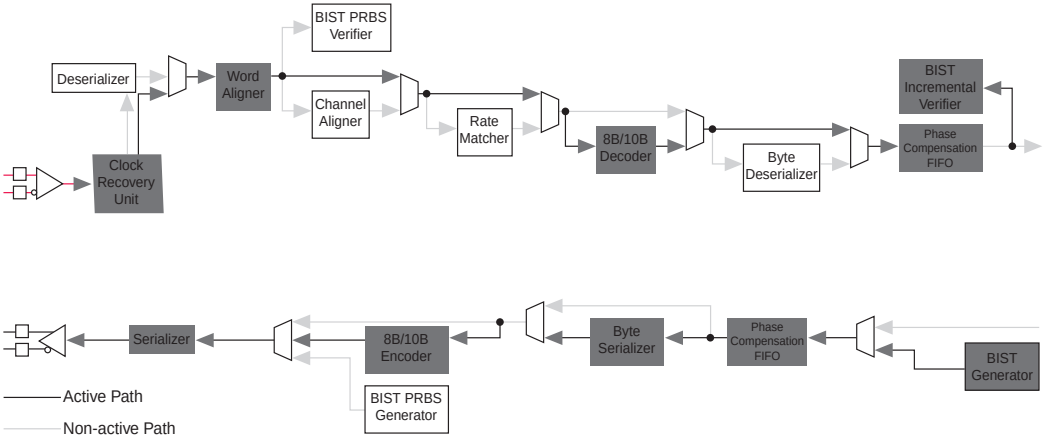


Table 2–9 shows the BIST data output and verifier alignment pattern.

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 1 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 8-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 10-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111

The logic array sends parallel data to the SERDES transmitter circuit when the TXLOADEN signal is asserted. This signal is generated by the high-speed counter circuitry of the logic array low-frequency clock's rising edge. The data is then transferred from the parallel register into the serial shift register by the TXLOADEN signal on the third rising edge of the high-frequency clock.

Figure 3–3 shows the block diagram of a single SERDES transmitter channel and Figure 3–4 shows the timing relationship between the data and clocks in Stratix GX devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

Figure 3–3. Stratix GX High-Speed Interface Serialized in ×10 Mode

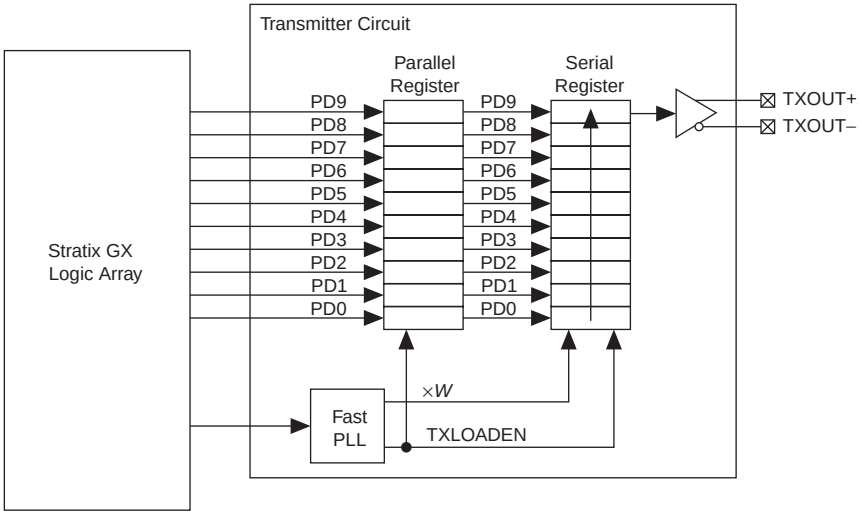
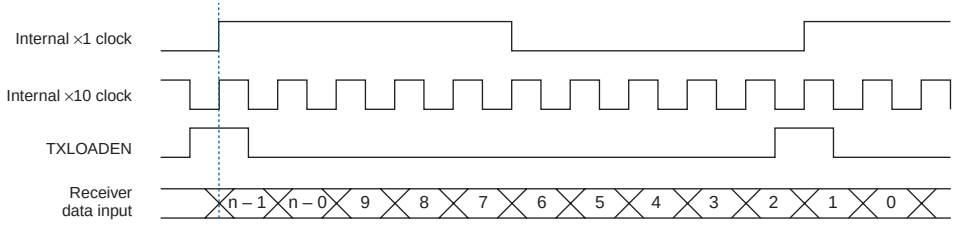
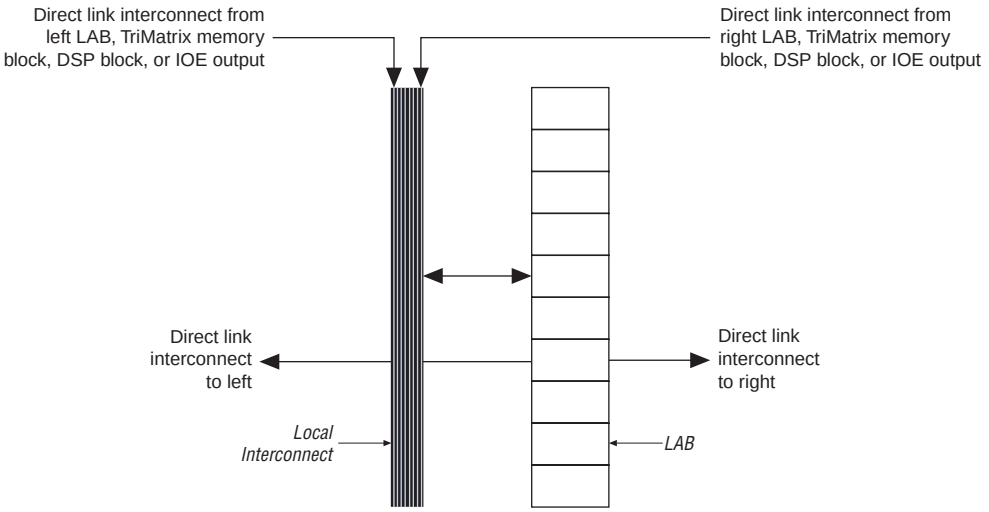


Figure 3–4. Transmitter Timing Diagram



M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 4–2 shows the direct link connection.

Figure 4–2. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal turns off the LAB-wide clock.

LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix GX devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 4–9 shows the LUT chain and register chain interconnects.

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 4–4 and 4–5 summarize the possible M4K RAM block configurations.

Table 4–4. M4K RAM Block Configurations (Simple Dual-Port)

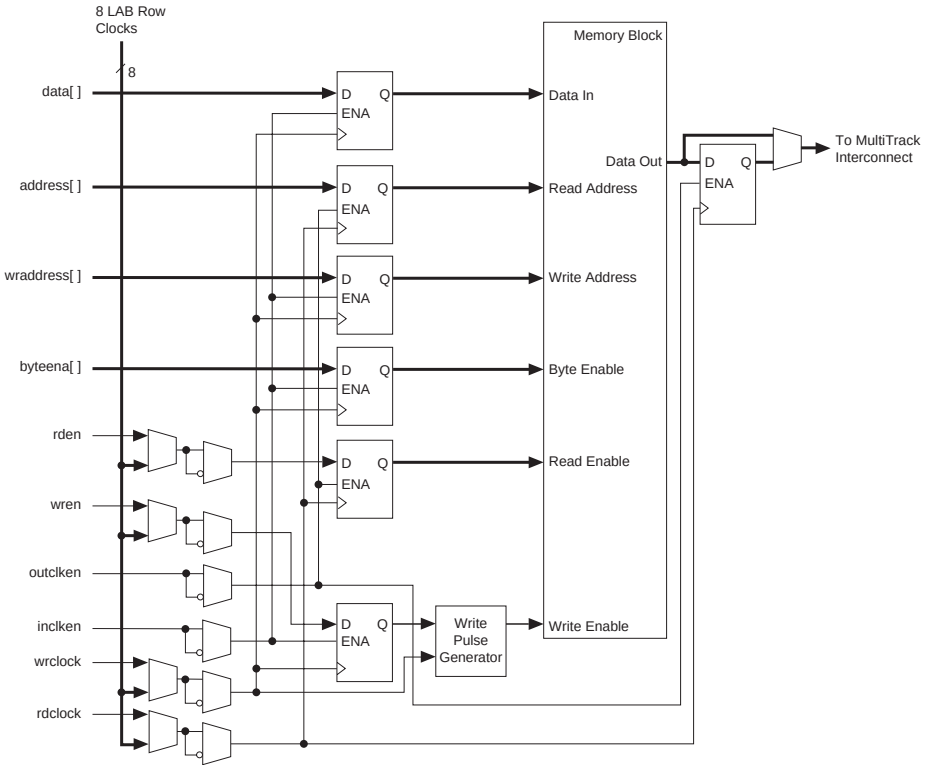
Read Port	Write Port								
	4K 1	2K × 2	1K ° 4	512 ° 8	256 ° 16	128 ° 32	512 ° 9	256 ° 18	128 ° 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 4–5. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 4–26. Read/Write Clock Mode in Simple Dual-Port Mode *Note (1)*



Note to Figure 4–26:
(1) All registers shown except the `rden` register have asynchronous clear ports.

Single-Port Mode

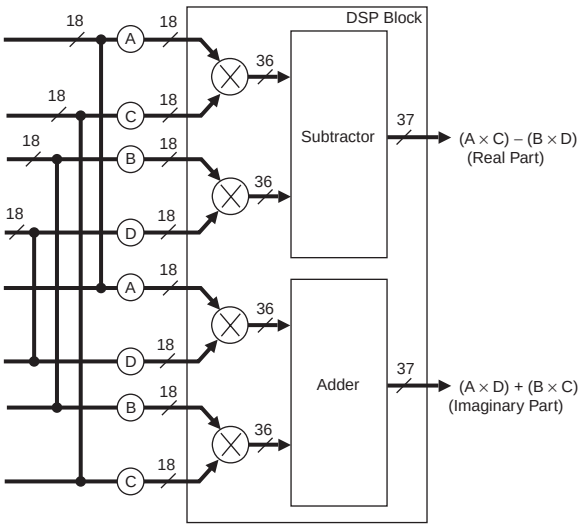
The memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 4–27. A single block in a memory block can support up to two single-port mode RAM blocks in the M4K RAM blocks if each RAM block is less than or equal to 2K bits in size.

You can use the two-multipliers adder mode for complex multiplications, which are written as:

$$(a + jb) \times (c + jd) = [(a \times c) - (b \times d)] + j \times [(a \times d) + (b \times c)]$$

The two-multipliers adder mode allows a single DSP block to calculate the real part $[(a \times c) - (b \times d)]$ using one subtractor and the imaginary part $[(a \times d) + (b \times c)]$ using one adder, for data widths up to 18 bits. Two complex multiplications are possible for data widths up to 9 bits using four adder/subtractor/accumulator blocks. Figure 4–37 shows an 18-bit two-multipliers adder.

Figure 4–37. Two-Multipliers Adder Mode Implementing Complex Multiply



Four-Multipliers Adder Mode

In the four-multipliers adder mode, the DSP block adds the results of two first -stage adder/subtractor blocks. One sum of four 18 × 18-bit multipliers or two different sums of two sets of four 9 × 9-bit multipliers can be implemented in a single DSP block. The product width for each multiplier must be the same size. The four-multipliers adder mode is useful for FIR filter applications. Figure 4–38 shows the four multipliers adder mode.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (that is, implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 4–15 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 4–15. Multiplier Size & Configurations per DSP block

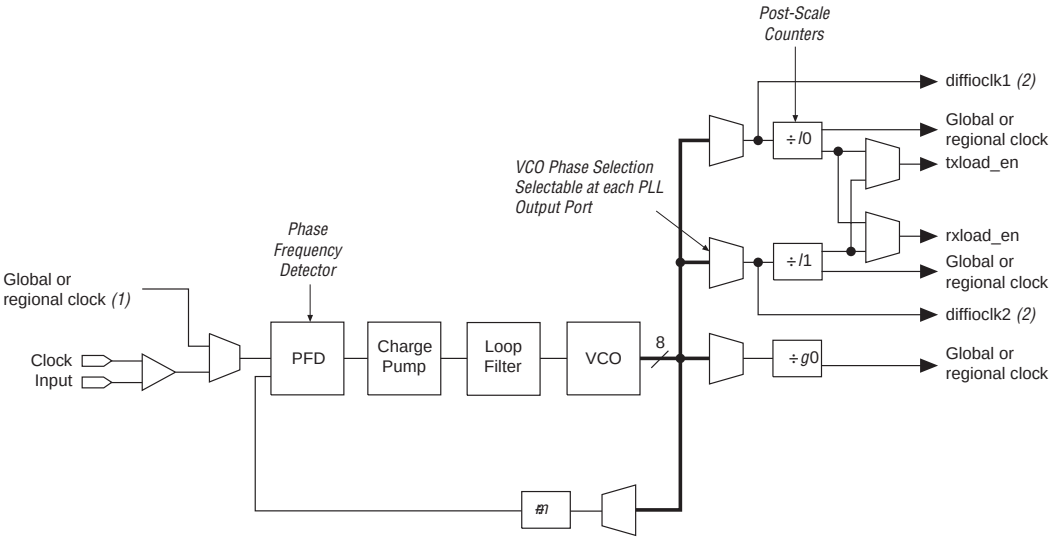
DSP Block Mode	9 × 9	18 × 18	36 × 36 *(1)*
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

Note to Table 4–15:
(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP Block Interface

Stratix GX device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

Figure 4–57. Stratix GX Device Fast PLL



Notes to Figure 4–57:

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

The Stratix GX device's fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output

Table 4–23 shows the number of DQ and DQS buses that are supported per device.

Table 4–23. DQS & DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×16 Groups	Number of ×32 Groups
EP1SGX10	672-pin FineLine BGA	12 *(2)*	0	0
EP1SGX25	672-pin FineLine BGA	16 *(3)*	8	4
	1,020-pin FineLine BGA	20	8	4
EP1SGX40	1,020-pin FineLine BGA	20	8	4

Notes to Table 4–23:

(1) See the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2* for V_{REF} guidelines.

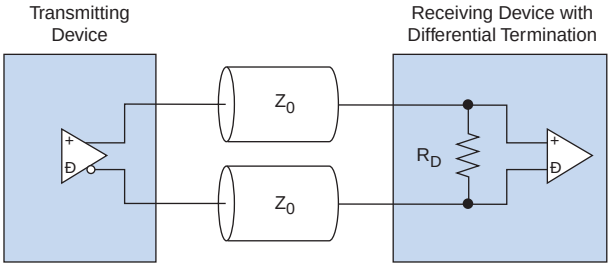
(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.

(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and clocks DQ input registers with the DQS signal.

Two separate single phase-shifting reference circuits are located on the top and bottom of the Stratix GX device. Each circuit is driven by a system reference clock through the `CLK` pins that is the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase-shift circuitry on the bottom of the device. The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device shift by the same degree amount. For example, all 10 DQS pins on the top of the device can be shifted by 90° and all 10 DQS pins on the bottom of the device can be shifted by 72°. The reference circuits require a maximum of 256 system reference clock cycles to set the correct phase on the DQS delay elements. Figure 4–68 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 4–70. LVDS Input Differential On-Chip Termination



I/O banks on the left and right side of the device support LVDS receiver (far-end) differential termination.

Table 4–29 shows the Stratix GX device differential termination support.

Table 4–29. Differential Termination Supported by I/O Banks

Differential Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)
Differential termination *(1)*, *(2)*	LVDS		✓

Notes to Table 4–29:
(1) Clock pin CLK0, CLK2, CLK9, CLK11, and pins FPLL[7..10]CLK do not support differential termination.
(2) Differential termination is only supported for LVDS because of a 3.3-V V_{CCIO}.

Table 4–30 shows the termination support for different pin types.

Table 4–30. Differential Termination Support Across Pin Types

Pin Type	R_D
Top and bottom I/O banks (3, 4, 7, and 8)	
DIFFIO_RX[]	✓
CLK[0,2,9,11],CLK[4-7],CLK[12-15]	
CLK[1,3,8,10]	✓
FCLK	
FPLL[7..10]CLK	

The differential on-chip resistance at the receiver input buffer is 118 Ω ±20 %.

Table 4–36. Stratix GX JTAG Timing Parameters & Values (Part 2 of 2)

Symbol	Parameter	Min (ns)	Max (ns)
t_{JPH}	JTAG port hold time	45	
t_{JPCO}	JTAG port clock to output		25
t_{JPZX}	JTAG port high impedance to valid output		25
t_{JPXZ}	JTAG port valid output to high impedance		25
t_{JSSU}	Capture register setup time	20	
t_{JSH}	Capture register hold time	45	
t_{JSCO}	Update register clock to output		35
t_{JSZX}	Update register high impedance to valid output		35
t_{JSXZ}	Update register valid output to high impedance		35

Partial Reconfiguration

The enhanced PLLs within the Stratix GX device family support partial reconfiguration of their multiply, divide, and time delay settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL. See the *Stratix GX Architecture* chapter of the *Stratix GX Device Handbook, Volume 1* for more information on Stratix GX PLLs.

Remote Update Configuration Modes

Stratix GX devices also support remote configuration using an Altera enhanced configuration device (for example, EPC16, EPC8, and EPC4 devices) with page mode selection. Factory configuration data is stored in the default page of the configuration device. This is the default configuration which contains the design required to control remote updates and handle or recover from errors. You write the factory configuration once into the flash memory or configuration device. Remote update data can update any of the remaining pages of the configuration device. If there is an error or corruption in a remote update configuration, the configuration device reverts back to the factory configuration information.

There are two remote configuration modes: remote and local configuration. You can use the remote update configuration mode for all three configuration modes: serial, parallel synchronous, and parallel asynchronous. Configuration devices (for example, EPC16 devices) only support serial and parallel synchronous modes. Asynchronous parallel mode allows remote updates when an intelligent host is used to configure the Stratix GX device. This host must support page mode settings similar to an EPC16 device.

Remote Update Mode

When the Stratix GX device is first powered-up in remote update programming mode, it loads the configuration located at page address `000`. The factory configuration should always be located at page address `000`, and should never be remotely updated. The factory configuration contains the required logic to perform the following operations:

- Determine the page address/load location for the next application's configuration data
- Recover from a previous configuration error

Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 2 of 2) *Note (7), (12), (13)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C

Table 6–3. Stratix GX Device DC Operating Conditions *Note (12)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 6–4. Stratix GX Transceiver Block Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	2.4	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCG}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
Receiver input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V
`refclkb` input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 3 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade *(1)*			-6 Commercial & Industrial Speed Grade *(1)*			-7 Commercial & Industrial Speed Grade *(1)*			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter	f = 42.5 kHz at 1.0625 Gbps			1.5			1.5			1.5	UI
	f = 637 kHz at 1.0625 Gbps			0.1			0.1			0.1	UI
Deterministic jitter	2.125 Gbps			0.33			0.33			0.33	UI
Total jitter	2.125 Gbps			0.62			0.62			0.62	UI
Sinusoidal jitter	f = 85 kHz at 2.125 Gbps			1.5			1.5			1.5	UI
	f = 1,274 kHz at 2.125 Gbps			0.1			0.1			0.1	UI
Serial Rapid I/O Receiver Jitter Tolerance using 8B/10B Encoded CJPAT *Note (2)*											
Deterministic jitter	1.25 Gbps			0.45			0.45			0.45	UI
Total jitter	1.25 Gbps			0.71			0.71			0.71	UI
Deterministic jitter	2.5 Gbps			0.41			0.41			0.41	UI
Total jitter	2.5 Gbps			0.65			0.65			0.65	UI
Deterministic jitter	3.125 Gbps			0.36			0.36			N/A	UI
Total jitter	3.125 Gbps			0.60			0.60			N/A	UI
SONET Receiver Jitter Tolerance using PRBS23 *Note (2)*											
Sinusoidal jitter	f = 6 kHz at 2.48832 Gbps			1.5			1.5			1.5	UI
	f = 1 MHz at 2.48832 Gbps			0.15			0.15			0.15	UI
XAUI Receiver Jitter Tolerance using 8B/10B Encoded CJPAT *Note (2)*											
Deterministic jitter	3.125 Gbps			0.37			0.37			N/A	UI
Total jitter	3.125 Gbps			0.65			0.65			N/A	UI

Table 6–23. SSTL-2 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Table 6–24. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Table 6–25. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(1)*			V_{TT} – 0.6	V

Table 6–26. SSTL-3 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V

Table 6–35. Stratix GX Device Performance (Part 2 of 3) *Notes (1), (2)*

Applications		Resources Used			Performance			
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
TriMatrix memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	317.76	277.62	241.48	MHz
	FIFO 32 × 18 bit	30	1	0	319.18	278.86	242.54	MHz
TriMatrix memory M4K block	Simple dual-port RAM 128 × 36 bit	0	1	0	290.86	255.55	222.27	MHz
	True dual-port RAM 128 × 18 bit	0	1	0	290.86	255.55	222.27	MHz
	FIFO 128 × 36 bit	34	1	0	290.86	255.55	222.27	MHz
TriMatrix memory M-RAM block	Single port RAM 4K × 144 bit	1	1	0	255.95	223.06	194.06	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	MHz
	Single port RAM 8K × 72 bit	0	1	0	278.94	243.19	211.59	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	MHz
	Single port RAM 16K × 36 bit	0	1	0	280.66	254.32	221.28	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	MHz

Table 6–40. M4K Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Table 6–41. M-RAM Block Internal Timing Microparameter Descriptions (Part 1 of 2)	
Symbol	**Parameter**
t_{MRAMRC}	Synchronous read cycle time
t_{MRAMWC}	Synchronous write cycle time
$t_{MRAMWERESU}$	Write or read enable setup time before clock
$t_{MRAMWEREH}$	Write or read enable hold time after clock
$t_{MRAMBESU}$	Byte enable setup time before clock
$t_{MRAMBEH}$	Byte enable hold time after clock
$t_{MRAMDATAASU}$	A port data setup time before clock
$t_{MRAMDATAAH}$	A port data hold time after clock
$t_{MRAMADDRASU}$	A port address setup time before clock
$t_{MRAMADDRAH}$	A port address hold time after clock