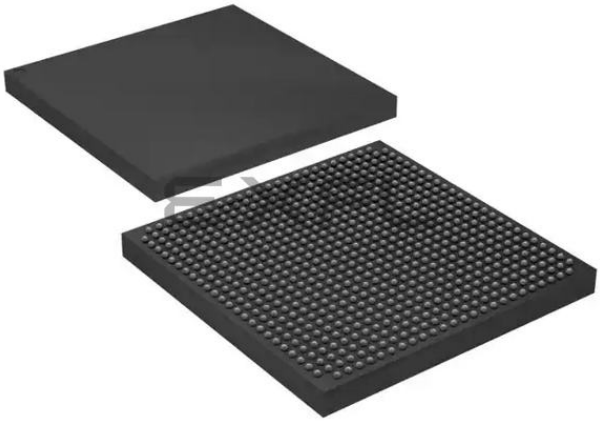


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	362
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx10df672c5n

- Pattern detector and word aligner supports programmable patterns
- 8B/10B encoder/decoder performs 8- to 10-bit encoding and 10- to 8-bit decoding
- Rate matcher compliant with IEEE 802.3-2002 for GigE mode and with IEEE 802-3ae for XAUI mode
- Channel bonding compliant with IEEE 802.3ae (for XAUI mode only)
- Device can bypass some transceiver block features if necessary

- FPGA features are as follows:
  - 10,570 to 41,250 logic elements (LEs); see Table 1–1
  - Up to 3,423,744 RAM bits (427,968 bytes) available without reducing logic resources
  - TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in-out (FIFO) buffers
  - Up to 16 global clock networks with up to 22 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to eight general usage phase-locked loops (four enhanced PLLs and four fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 45 channels for 1-Gbps performance
  - Support for source-synchronous bus standards, including 10-Gigabit Ethernet XSBI, Parallel RapidIO, UTOPIA IV, Network Packet Streaming Interface (NPSI), HyperTransport™ technology, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
  - Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - Support for remote configuration updates
  - Dynamic phase alignment on LVDS receiver channels

Figure 2–30. EP1SGX40 Receiver PLL Recovered Clock to Regional Clock Connection

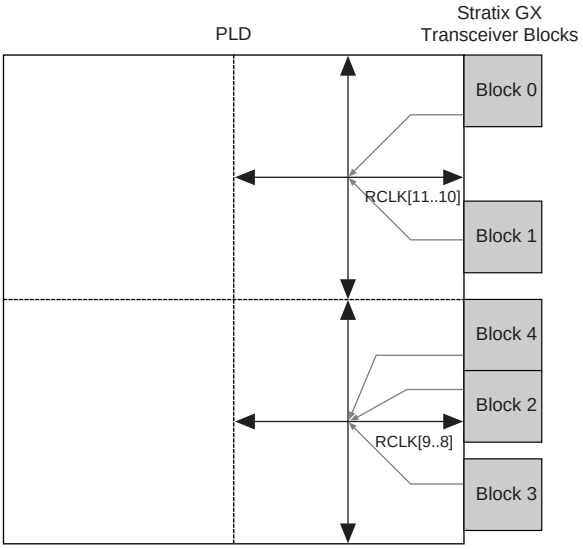


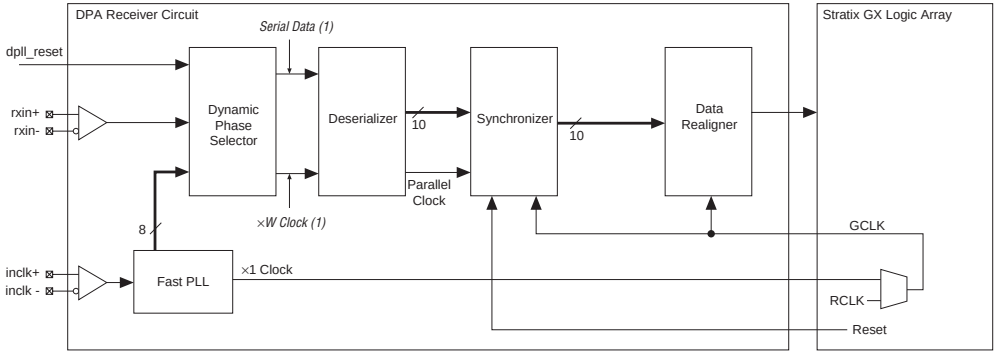
Figure 2–31 shows the possible recovered clock connection to the fast regional clock resource. The fast regional clocks can drive logic in their associated regions.

DPA Operation

The DPA receiver circuitry contains the dynamic phase selector, the deserializer, the synchronizer, and the data realigner (see Figure 3–8). This section describes the DPA operation, synchronization and data realignment. In the SERDES with DPA mode, the source clock is fed to the fast PLL through the dedicated clock input pins. This clock is multiplied by the multiplication value *W* to match the serial data rate.

For information on the deserializer, see "Principles of SERDES Operation" on page 3–1.

Figure 3–8. DPA Receiver Circuit



Note to Figure 3–8:
(1) These are phase-matched and retimed high-speed clocks and data.

The dynamic phase selector matches the phase of the high-speed clock and data before sending them to the deserializer.

The fast PLL supplies eight phases of the same clock (each a separate tap from a four-stage differential VCO) to all the differential channels associated with the selected fast PLL. The DPA circuitry inside each channel locks to a phase closest to the serial data's phase and sends the retimed data and the selected clock to the deserializer. The DPA circuitry automatically performs this operation and is not something you select. Each channel's DPA circuit can independently choose a different clock phase. The data phase detection and the clock phase selection process is automatic and continuous. The eight phases of the clock give the DPA circuit a granularity of one eighth of the unit interval (UI) or 125 ps at 1 Gbps. Figure 3–9 illustrates the clocks generated by the fast PLL circuitry and their relationship to a data stream.

Figure 3–10. Misaligned Captured Bits

The dynamic phase selector and synchronizer align the clock and data based on the power-up of both communicating devices, and the channel to channel skew. However, the dynamic phase selector and synchronizer cannot determine the byte boundary, and the data may need to be byte-aligned. The dynamic phase aligner's data realignment circuitry shifts data bits to correct bit misalignments.

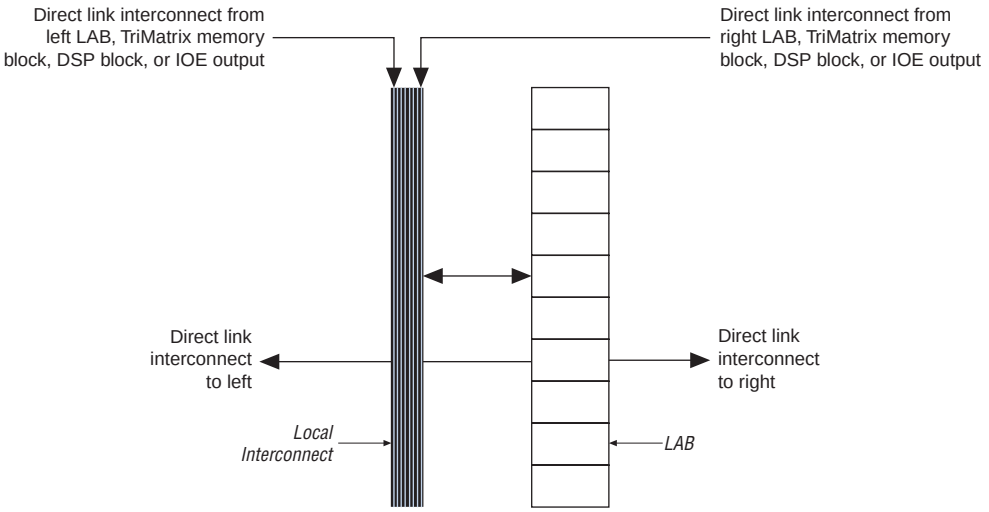
The Stratix GX circuitry contains a data-realignment feature controlled by the logic array. Stratix GX devices perform data realignment on the parallel data after the deserialization block. The data realignment can be performed per channel for more flexibility. The data alignment operation requires a state machine to recognize a specific pattern. The procedure requires the bits to be slipped on the data stream to correctly align the incoming data to the start of the byte boundary.

The DPA uses its realignment circuitry and the global clock for data realignment. Either a device pin or the logic array asserts the internal `rx_channel_data_align` node to activate the DPA data-realignment circuitry. Switching this node from low to high activates the realignment circuitry and the data being transferred to the logic array is shifted by one bit. The data realignment block cannot be bypassed. However, if the `rx_channel_data_align` is not turned on (through the `altvlds` MegaWizard Plug-In Manager), or when it is not toggled, it only acts as a register latency.

A state machine and additional logic can monitor the incoming parallel data and compare it against a known pattern. If the incoming data pattern does not match the known pattern, you can activate the `rx_channel_data_align` node again. Repeat this process until the realigner detects the desired match between the known data pattern and incoming parallel data pattern.

M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 4–2 shows the direct link connection.

Figure 4–2. Direct Link Connection

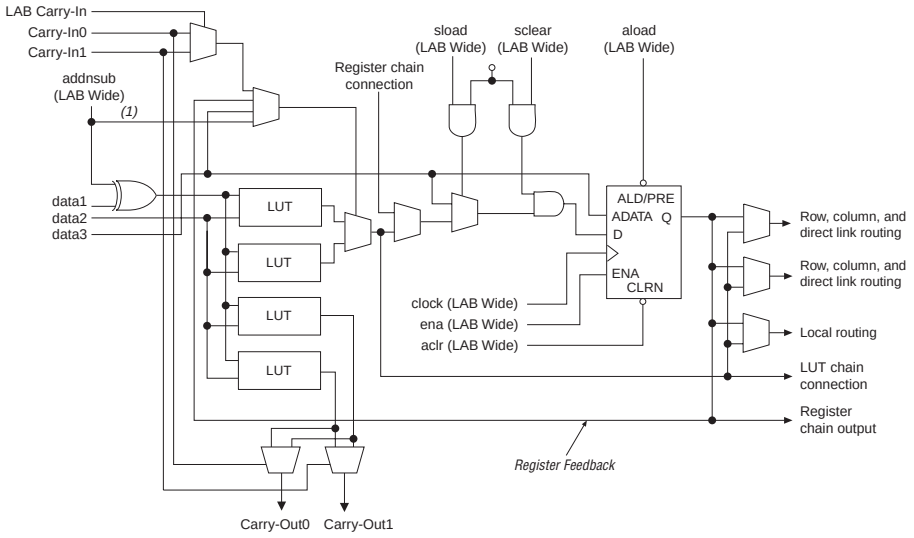


LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal turns off the LAB-wide clock.

Figure 4–6. LE in Dynamic Arithmetic Mode



Note to Figure 4–6:
(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Because the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix GX architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 4–7 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 4–96 for details on dedicated SERDES in Stratix GX devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, `inclr`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 4–14 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix GX devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 4–15 shows the M512 RAM block to logic array interface.

Figure 4–22. M-RAM Column Unit Interface to Interconnect

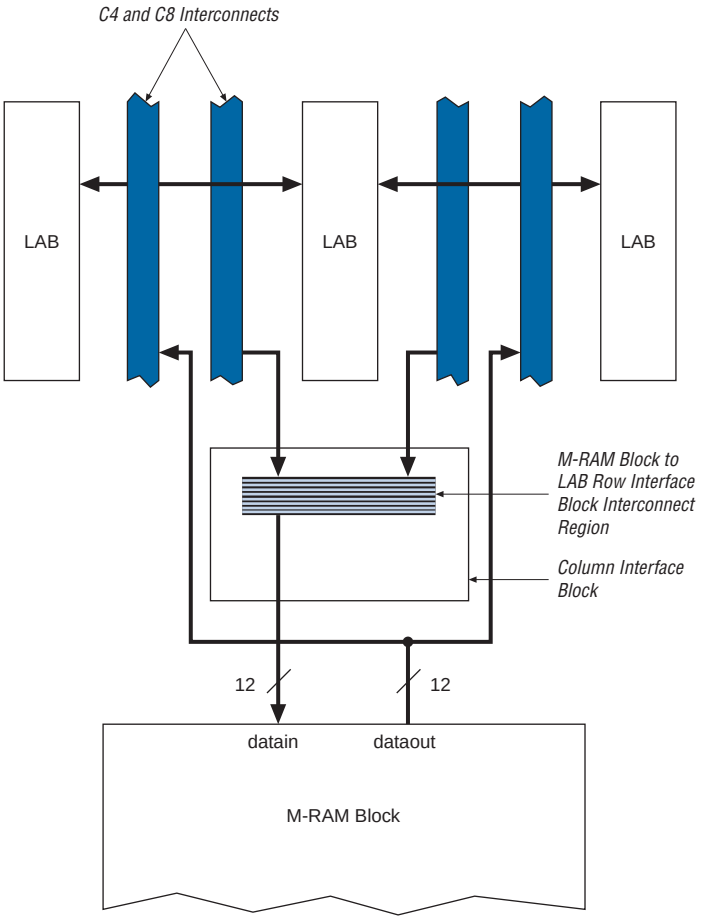
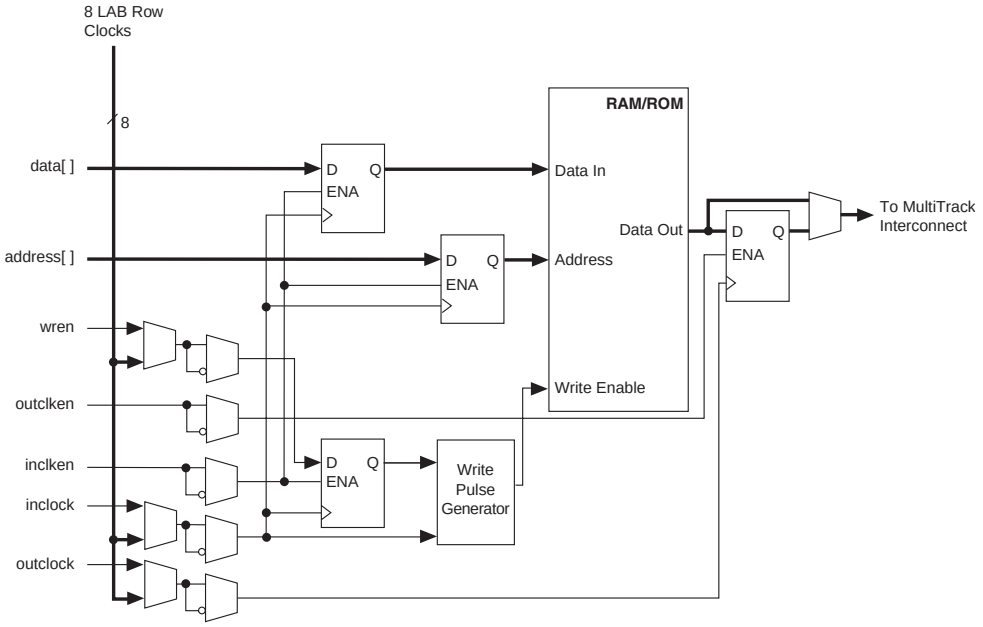


Figure 4–27. Single-Port Mode



Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

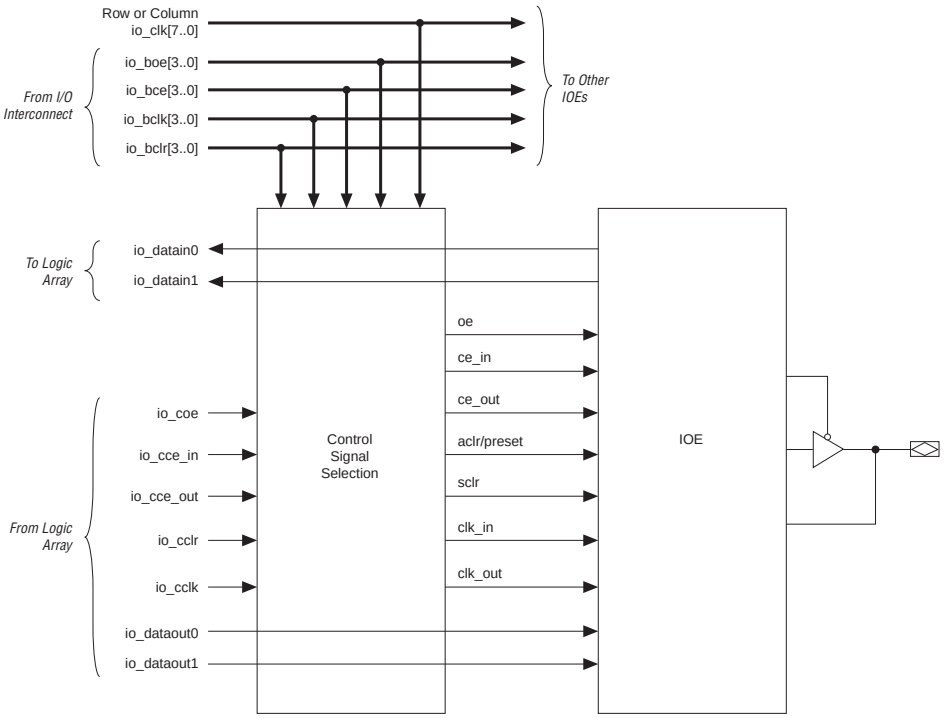
Each Stratix GX device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix GX devices have more DSP blocks per column (see Table 4–12). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix GX DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but

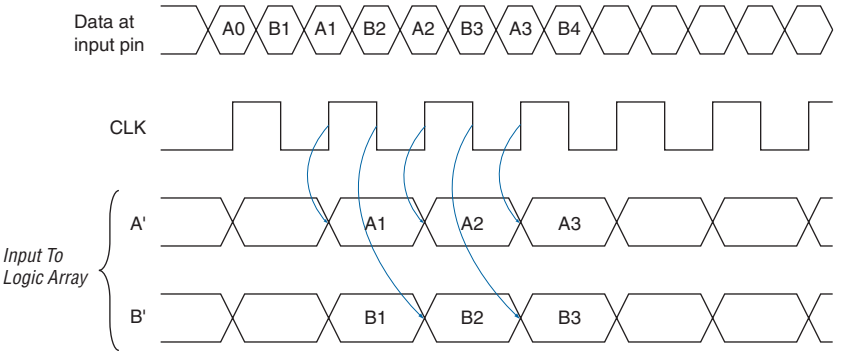
Stratix GX devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 4–68). Figure 4–61 illustrates the signal paths through the I/O block.

Figure 4–61. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 4–62 illustrates the control signal selection.

Figure 4–65. Input Timing Diagram in DDR Mode



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 4–66 shows the IOE configured for DDR output. Figure 4–67 shows the DDR output timing diagram.

Table 4–35. 32-Bit Stratix GX Device IDCODE (Part 2 of 2)

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1SGX40	0000	0010 0000 0100 0101	000 0110 1110	1

Notes to Table 4–35:
(1) The most significant bit (MSB) is at the left end of the string.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 4–72 shows the timing requirements for the JTAG signals.

Figure 4–72. Stratix GX JTAG Waveforms

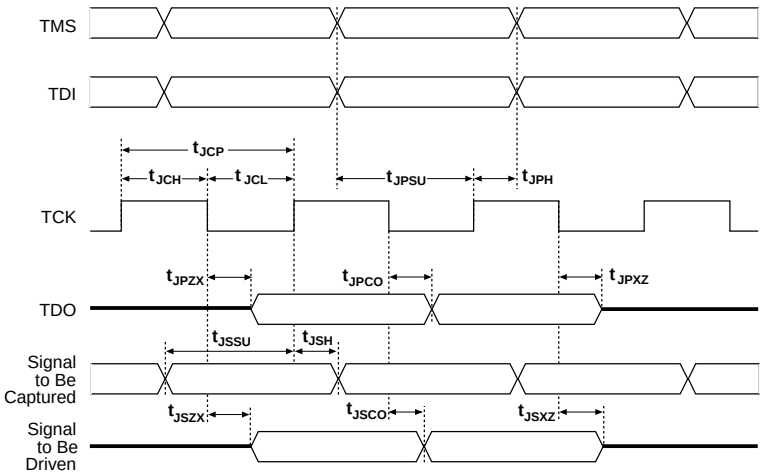


Table 4–36 shows the JTAG timing parameters and values for Stratix GX devices.

Table 4–36. Stratix GX JTAG Timing Parameters & Values (Part 1 of 2)

Symbol	Parameter	Min (ns)	Max (ns)
t_{JCP}	TCK clock period	100	
t_{JCH}	TCK clock high time	50	
t_{JCL}	TCK clock low time	50	
t_{JPSU}	JTAG port setup time	20	

and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

SRAM configuration elements allow Stratix GX devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

Configuration Schemes

You can load the configuration data for a Stratix GX device with one of five configuration schemes (see Table 5–1), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix GX device. A configuration device can automatically configure a Stratix GX device at system power-up.

You can configure multiple Stratix GX devices in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 5–1. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	ByteBlasterMV™ or MasterBlaster™ download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file (.jam or .jbc)

Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 2 of 2) *Note (7), (12), (13)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C

Table 6–3. Stratix GX Device DC Operating Conditions *Note (12)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 6–4. Stratix GX Transceiver Block Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	2.4	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCG}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
Receiver input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V
`refclkb` input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V

Table 6–16. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage (single ended)	R_L = 100 Ω	380	485	820	mV
ΔV_{OD}	Change in between high and low	R_L = 100 Ω			50	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	650	780	mV
ΔV_{OCM}	Change in between high and low	R_L = 100 Ω			50	mV
V_{ID}	Differential input voltage swing (single-ended)		300		900	mV
V_{ICM}	Input common mode voltage		300		900	mV
R_L	Receiver differential input resistor, external		90	100	110	Ω

Table 6–17. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 6–18. PCI-X Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V

Table 6–18. PCI-X Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 6–19. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(1)*			0.65	V

Table 6–20. GTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.14	1.2	1.26	V
V_{REF}	Reference voltage		0.74	0.8	0.86	V
V_{IH}	High-level input voltage		V_{REF} + 0.05			V
V_{IL}	Low-level input voltage				V_{REF} – 0.05	V
V_{OL}	Low-level output voltage	I_{OL} = 40 mA *(1)*			0.4	V

Table 6–21. SSTL-18 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V

Table 6–32. CTT I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤ V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 6–33. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	25		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–25		–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		–160		–200		–300		–500	µA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Tables 6–14 through 6–33:

(1) Drive strength is programmable according to values in the *Stratix GX Architecture* chapter of the *Stratix GX Device Handbook, Volume 1*.

(2) V_{REF} specifies the center point of the switching range.

Power Consumption

Detailed power consumption information for Stratix GX devices will be released when available.

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.245		2.332		2.666		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.597	2.000	4.920	2.000	5.635	ns

Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.114		2.218		2.348		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.728	2.000	5.078	2.000	6.004	ns
$t_{INSUPLL}$	1.035		0.941		1.070		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.629	0.500	2.769	0.500	3.158	ns

Table 6–77. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,930		2,031		2,335	ps
	4 mA		1,930		2,031		2,335	ps
	8 mA		1,710		1,800		2,069	ps
	12 mA		1,490		1,569		1,803	ps
3.3-V LVTTL	4 mA		1,953		2,055		2,363	ps
	8 mA		1,733		1,824		2,097	ps
	12 mA		1,513		1,593		1,831	ps
	16 mA		1,453		1,530		1,759	ps
2.5-V LVTTL	2 mA		2,632		2,769		3,183	ps
	8 mA		2,052		2,160		2,483	ps
	12 mA		1,942		2,044		2,350	ps
	16 mA		1,902		2,002		2,301	ps
1.8-V LVTTL	2 mA		4,537		4,773		5,489	ps
	8 mA		3,447		3,628		4,172	ps
	12 mA		3,377		3,555		4,088	ps
1.5-V LVTTL	2 mA		6,575		6,917		7,954	ps
	4 mA		5,995		6,308		7,253	ps
	8 mA		5,525		5,815		6,686	ps
CTT			1,410		1,485		1,707	ps
SSTL-3 class I			1,450		1,527		1,755	ps
SSTL-3 class II			1,310		1,380		1,586	ps
SSTL-2 class I			1,797		1,892		2,175	ps
SSTL-2 class II			1,717		1,808		2,079	ps
LVDS *(1)*			1,340		1,411		1,622	ps
LVPECL *(1)*			1,400		1,474		1,694	ps
3.3-V PCML *(1)*			1,300		1,369		1,573	ps
HyperTransport technology *(1)*			1,430		1,506		1,731	ps

Note to Tables 6–72 through 6–77:
(1) These parameters are only available on the left side row I/O pins.

Table 6–87. High-Speed I/O Specifications (Part 4 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	110	170	200	ps
	LVPECL	90	130	160	90	130	160	100	135	160	ps
	PCML	105	140	175	105	140	175	110	145	175	ps
t_{DUTY}	LVDS (*J* = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (*J* =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100	µs

Notes to Table 6–87:
(1) When J = 4, 7, 8, and 10, the SERDES block is used.
(2) When J = 2 or J = 1, the SERDES is bypassed.
(3) Number of parallel CLK cycles.
(4) Number of repetitions.

PLL Timing

Tables 6–88 through 6–90 describe the Stratix GX device enhanced PLL specifications.

Table 6–88. Enhanced PLL Specifications for -5 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*		684	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(2)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(2)*	ps
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		500	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		526	MHz