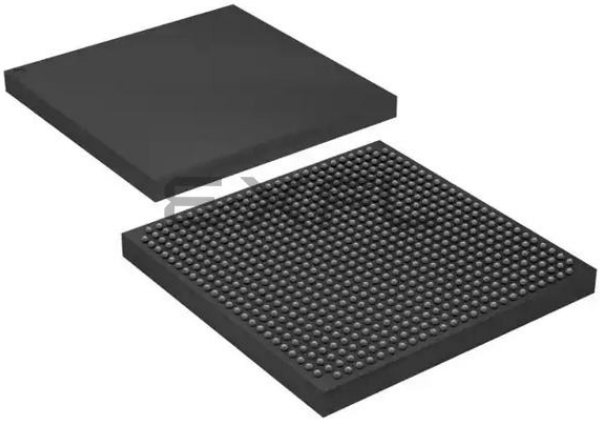

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	362
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx10df672i6

Revision History

The table below shows the revision history for Chapters 1 through 7.

Chapter(s)	Date / Version	Changes Made	Comments
1	February 2005, v1.0	Initial Release.	
2	June 2006, v1.1	• Updated "Serial Loopback" section. • Updated Figures 2–1 through 2–3. • Updated Figure 2–13. • Updated Figures 2–26 and 2–27.	
	February 2005, v1.0	Initial Release.	
3	August 2005, v1.1	Added Note (3) to Figure 3-7.	
4	February 2005, v1.0	Initial Release.	
5	February 2005, v1.0	Initial Release.	
6	June 2006, v1.2	• Updated "Operating Conditions" section. • Updated Table 6–4. • Updated note 3 in Table 6–6. • Added note 12 in Table 6–7. • Updated Figure 6–1. • Added Figure 6–2. • Updated Tables 6–13 through 6–16.	• Changed V_{OD} to V_{ID} for receiver input voltage and `refclkb` input voltage in Table 6–4. • Changed value for undershoot during transition from -0.5 V to -2.0 V in note 3 of Table 6–6. • Changed value of V_{OCM} from mV to V in Table 6–15. • Changed unit value of W to Ω.
	August 2005, v1.1	Updated Tables 6-7 and 6-50.	
7	February 2005, v1.0	Initial Release.	

Receiver State Machine

The receiver state machine operates in GIGE and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with `9'h1FE`. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group. Table 2–8 shows the code conversion. The conversion adheres to the IEEE 802.3ae specification.

Table 2–8. Code Conversion

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal Data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code group	Invalid XGMII character
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups

Byte Deserializer

The byte deserializer takes a single width word (8 or 10 bits) from the transceiver logic and converts it into double-width words (16 or 20 bits) to the phase compensation FIFO buffer. The byte deserializer is bypassed when single width mode (8 or 10 bits) is used at the PLD interface.

Phase Compensation FIFO Buffer

The receiver phase compensation FIFO buffer resides in the transceiver block at the programmable logic device (PLD) boundary. This buffer compensates for the phase difference between the recovered clock within the transceiver and the recovered clock after it has transferred to the PLD core. The phase compensation FIFO buffer is four words deep and cannot be bypassed.

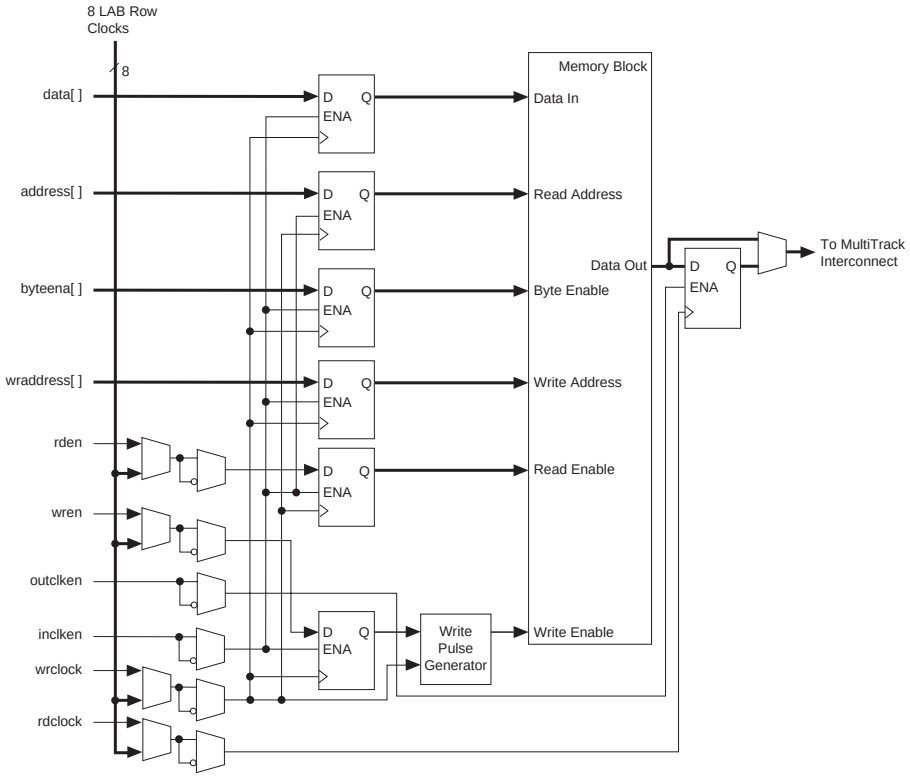
High-Speed Serial Bus Protocols

With wide, serial data rate range, Stratix GX devices can support multiple, high-speed serial bus protocols. Table 2–12 shows some of the protocols that Stratix GX devices can support.

Table 2–12. High-Speed Serial Bus Protocols

Bus Transfer Protocol	Stratix GX (Gbps) (Supports up to 3.1875 Gbps)
SONET backplane	2.488
10 Gigabit Ethernet XAUI	3.125
10 Gigabit fibre channel	3.1875
InfiniBand	2.5
Fibre channel (1G, 2G)	1.0625, 2.125
Serial RapidIO™	1.25, 2.5, 3.125
PCI Express	2.5
SMPTE 292M	1.485

Figure 4–25. Input/Output Clock Mode in Simple Dual-Port Mode *Note (1)*



Note to Figure 4–25:
(1) All registers shown except the `rden` register have asynchronous clear ports.

Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. You can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 4–26 shows a memory block in read/write clock mode.

Figure 4–48. PLL Floorplan

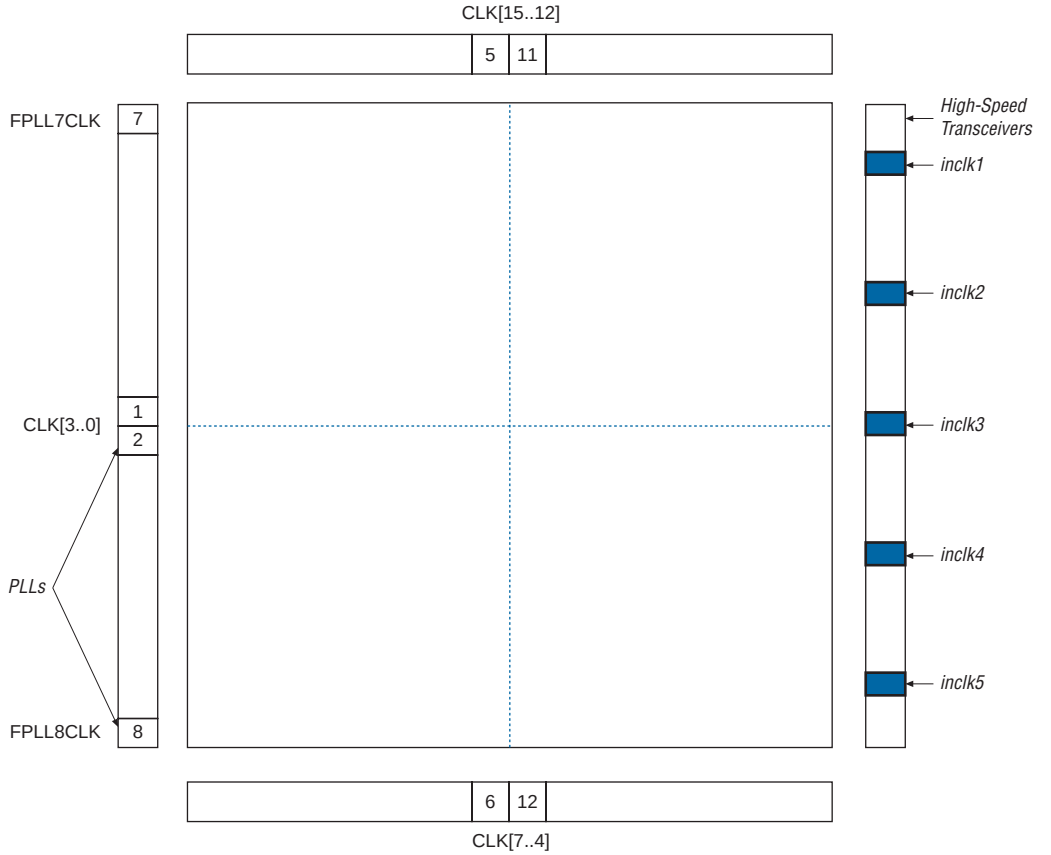


Figure 4–49 shows the global and regional clock connections from the PLL outputs and the CLK pins.

requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

During switchover, the PLL VCO continues to run and either slows down or speeds up, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The preliminary specification for the maximum time to relock is 100 µs.

For more information on clock switchover, see *AN313: Implementing Clock Switchover in Stratix & Stratix GX Devices*.

PLL Reconfiguration

The PLL reconfiguration feature enables system logic to change Stratix GX device enhanced PLL counters and delay elements without reloading a Programmer Object File (**.pof**). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. You can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or t_{CO} delays in end systems.

Clock delay elements at each PLL output port implement variable delay. Figure 4–53 shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20 µs for the enhanced PLL using a input shift clock rate of 25 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

The areset signals are reset/resynchronization inputs for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the areset signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

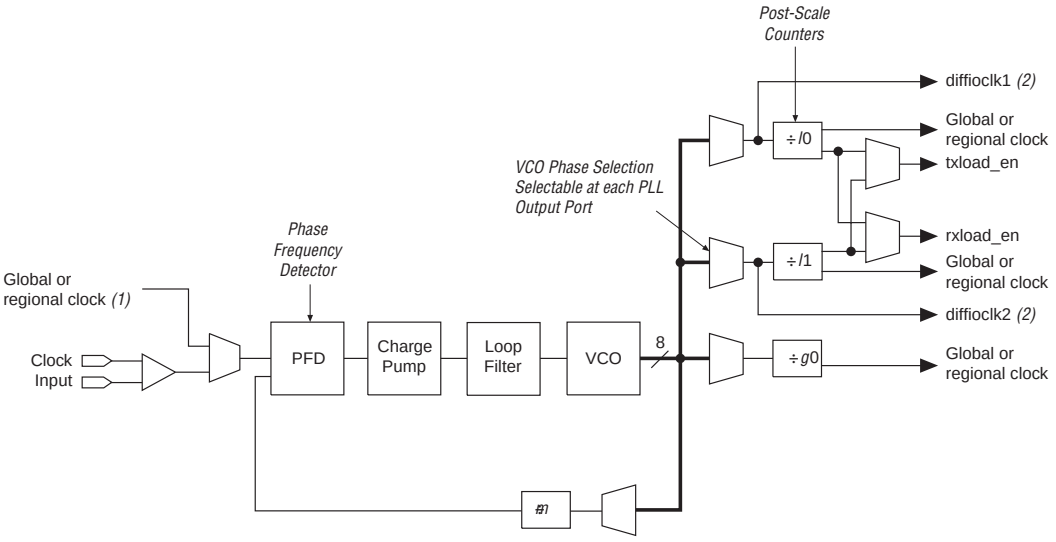
The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters resets, clearing the PLL output and placing the PLL out of lock. The VCO sets back to its nominal setting (~700 MHz). When driven low again, the PLL resynchronizes to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency starts at a higher value than desired as the PLL locks. If the system cannot tolerate this, the clkena signal can disable the output clocks until the PLL locks.

The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a clkloss status signal to trigger pfdena.

The clkena signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own clkena signal. The clkena signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The clkena signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 4–56 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the clkena signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The extclkena signals work in the same way as the clkena signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period

Figure 4–57. Stratix GX Device Fast PLL



Notes to Figure 4–57:

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

The Stratix GX device's fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output

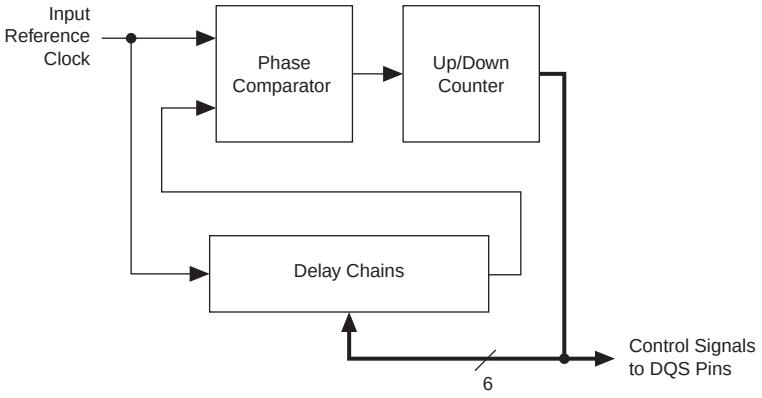
pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank.

Table 4–20 shows the I/O standards supported by fast PLL input pins.

Table 4–20. Fast PLL Port Input Pin I/O Standards

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL	✓	
3.3-V GTL+	✓	
1.5V HSTL class I	✓	
1.5V HSTL class II	✓	
SSTL-18 class I	✓	
SSTL-18 class II	✓	
SSTL-2 class I	✓	
SSTL-2 class II	✓	
SSTL-3 class I	✓	
SSTL-3 class II	✓	
AGP (1× and 2×)	✓	
CTT	✓	

Figure 4–68. Simplified Diagram of the DQS Phase-Shift Circuitry



See the *External Memory Interfaces* chapter of the *Stratix GX Device Handbook, Volume 2* for more information on external memory interfaces.

Programmable Drive Strength

The output buffer for each Stratix GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. The chapter *DC & Switching Characteristics* of the *Stratix GX Device Handbook, Volume 1* gives the specific sustaining current driven through this resistor and the overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix GX device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the output pin's bank. Table 4–26 shows which pin types support the weak pull-up resistor feature.

Table 4–26. Programmable Weak Pull-Up Resistor Support

Pin Type	Programmable Weak Pull-Up Resistor
I/O pins	✓
CLK[15..0]	
FCLK	✓
FPLL[7..10]CLK	
Configuration pins	
JTAG pins	✓ *(1)*

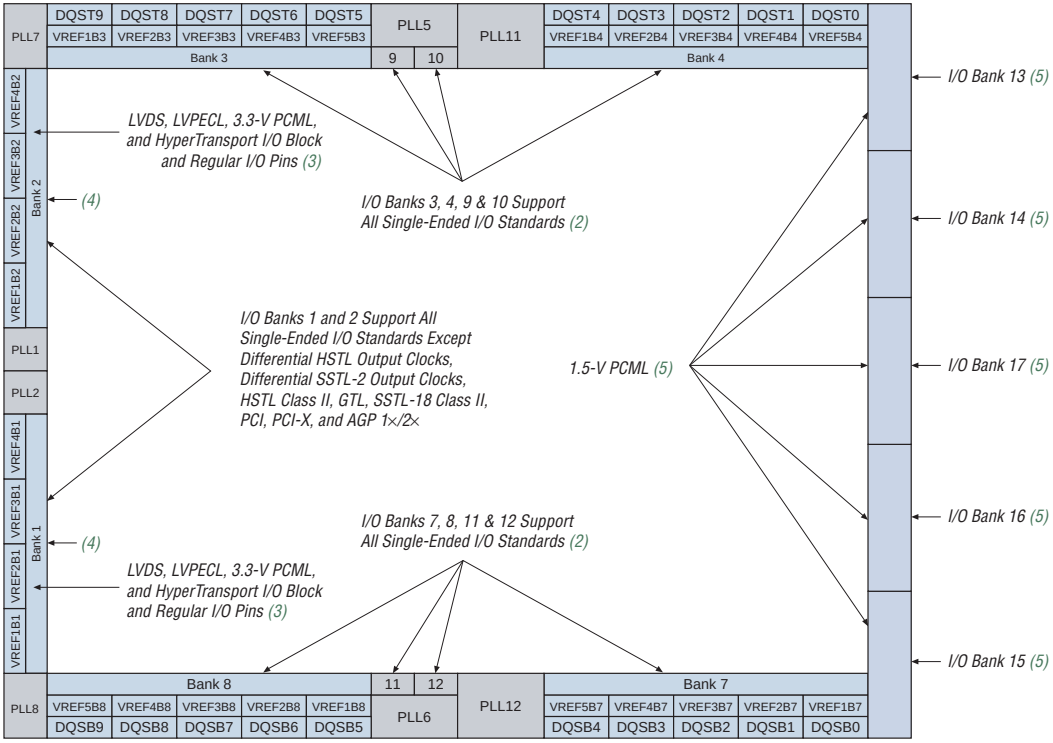
Note to Table 4–26:
(1) TDO pins do not support programmable weak pull-up resistors.

Advanced I/O Standard Support

Stratix GX device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)

Figure 4–69. Stratix GX I/O Banks *Notes (1), (2), (3)*



Notes to Figure 4–69:

(1) Figure 4–69 is a top view of the Stratix GX silicon die.

(2) Banks 9 through 12 are enhanced PLL external clock output banks.

(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix GX Device Handbook, Volume 2*.

(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled)

Figure 5–4. External Temperature-Sensing Diode

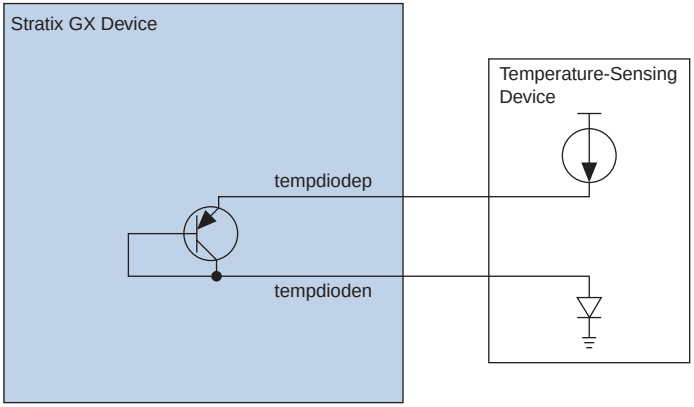


Table 5–2 shows the specifications for bias voltage and current of the Stratix GX temperature-sensing diode.

Table 5–2. Temperature-Sensing Diode Electrical Characteristics

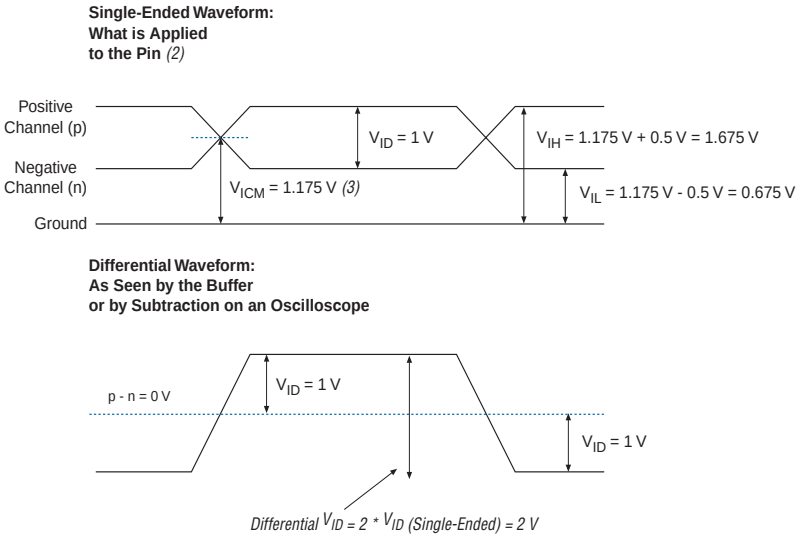
Parameter	Minimum	Typical	Maximum	Units
I_{BIAS} high	80	100	120	µA
I_{BIAS} low	8	10	12	µA
$V_{BP} - V_{BN}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	W

The temperature-sensing diode works for the entire operating range shown in Figure 5–5.

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 5 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade (1)			-6 Commercial & Industrial Speed Grade (1)			-7 Commercial & Industrial Speed Grade (1)			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fibre Channel Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.0625 Gbps Pre-emphasis = 0 V_{OD} = 1,200 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.125 Gbps Pre-emphasis= 1 V_{OD} = 1,200 mV			0.16			0.16			0.16	UI
Total jitter				0.33			0.33			0.33	UI
Serial Rapid I/O Short Run Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.25 Gbps Pre-emphasis = 1 V_{OD} = 1,600 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.5 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.15			0.15			0.15	UI
Total jitter				0.32			0.32			0.32	UI
Deterministic jitter	3.125 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.15			0.15			N/A	UI
Total jitter				0.32			0.32			N/A	UI
Serial Rapid I/O Long Run Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.25 Gbps Pre-emphasis = 1 V_{OD} = 1,600 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.5 Gbps Pre-emphasis = 2 V_{OD} = 1,400 mV			0.18			0.18			0.18	UI
Total jitter				0.35			0.35			0.35	UI
Deterministic jitter	3.125 Gbps Pre-emphasis = 2 V_{OD} = 1,400 mV			0.20			0.20			N/A	UI
Total jitter				0.37			0.37			N/A	UI
SONET Transmitter Jitter PRBS23 *Note (9)*											
Total jitter	2.48832 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.20			0.20			0.20	UI

Figure 6–2. Receiver Input Waveform Example with Values



Notes to Figure 6–2:

(1) The values in this figure are for example only.

(2) These values must meet the voltages specified in the section "Operating Conditions" on page 6–1.

(3) If internal termination is used, the common mode is generated after the pins.

Figure 6–3. Transmitter Output Waveforms for Differential I/O Standards

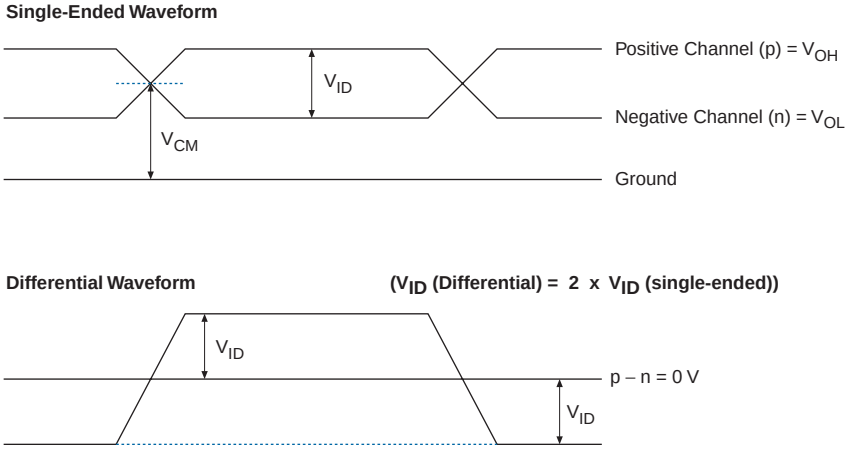


Table 6–48. M4K Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{M4KDATACO1}$		571		635		729	ps
$t_{M4KDATACO2}$		3,984		4,507		5,182	ps
$t_{M4KCLKHL}$	150		167		192		ps
t_{M4KCLR}	170		189		255		ps

Table 6–49. M-RAM Block Internal Timing Microparameters

Symbol	-5		-6		-7		Unit
	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562	ps
t_{MRAMWC}		3,654		4,127		4,746	ps
$t_{MRAMWERESU}$	25		25		28		ps
$t_{MRAMWERH}$	18		20		23		ps
$t_{MRAMDATASU}$	25		25		28		ps
$t_{MRAMDATAH}$	18		20		23		ps
$t_{MRAMWADDRASU}$	25		25		28		ps
$t_{MRAMWADDRH}$	18		20		23		ps
$t_{MRAMRADDRASU}$	25		25		28		ps
$t_{MRAMRADDRH}$	18		20		23		ps
$t_{MRAMDATABSU}$	25		25		28		ps
$t_{MRAMDATABH}$	18		20		23		ps
$t_{MRAMADDRBSU}$	25		25		28		ps
$t_{MRAMADDRBH}$	18		20		23		ps
$t_{MRAMDATACO1}$		1,038		1,053		1,210	ps
$t_{MRAMDATACO2}$		4,362		4,939		5,678	ps
$t_{MRAMCLKHL}$	270		300		345		ps
$t_{MRAMCLR}$	135		150		172		ps

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		180		189		217	ps
1.5-V HSTL class I		120		126		144	ps
1.5-V HSTL class II		120		126		144	ps
1.8-V HSTL class I		70		73		83	ps
1.8-V HSTL class II		70		73		83	ps

Table 6–73. Stratix GX I/O Standard Row Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		30		31		35	ps
1.8-V LVTTL		150		157		180	ps
1.5-V LVTTL		210		220		252	ps
GTL		0		0		0	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		80		84		96	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		0		0		0	ps
1.5-V HSTL class I		130		136		156	ps

Table 6–87. High-Speed I/O Specifications (Part 2 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSDR} Device operation (LVDS, LVPECL, HyperTransport technology)	*J* = 10	300		840	300		840	300		840	Mbps
	J = 8	300		840	300		840	300		840	Mbps
	J = 7	300		840	300		840	300		840	Mbps
	J = 4	300		840	300		840	300		840	Mbps
	J = 2	100		624	100		624	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		462	100		462	100		462	Mbps
$f_{HSDRDPA}$ (LVDS, LVPECL)	J=10	300		1000	300		840	300		840	Mbps
	J=8	300		1000	300		840	300		840	Mbps
f_{HSCLK} (Clock frequency) (PCML) f_{HSCLK} = f_{HSDR} / W	*W* = 1 to 30	10		400	10		400	10		311	MHz
f_{HSDR} Device operation (PCML)	*J* = 10	300		400	300		400	300		311	Mbps
	J = 8	300		400	300		400	300		311	Mbps
	J = 7	300		400	300		400	300		311	Mbps
	J = 4	300		400	300		400	300		311	Mbps
	J = 2	100		400	100		400	100		300	Mbps
	J = 1	100		250	100		250	100		200	Mbps
DPA Run Length				6400			6400			6400	UI
DPA Jitter Tolerance$_{(p-p)}$	all data rates			0.44			0.44			0.44	UI
DPA Minimum Eye opening (p-p)		0.56			0.56			0.56			UI
DPA Receiver Latency		5		9	5		9	5		9	*(3)*

Table 6–87. High-Speed I/O Specifications (Part 3 of 4) *Notes (1), (2)*

Symbol	Conditions			-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA Lock Time	Standard	Training Pattern	Transition Density										
	SPI-4, CSIX	0000 0000 0011 1111 1111	10%	256			256			256			*(4)*
	Rapid IO	0000 1111	25%	256			256			256			*(4)*
		1001 0000	50%	256			256			256			*(4)*
	Misc	1010 1010	100 %	256			256			256			*(4)*
		0101 0101		256			256			256			*(4)*
TCCS	All					200			200			300	ps
SW	PCML (J = 4, 7, 8, 10)			750			750			800			ps
	PCML (J = 2)			900			900			1,200			ps
	PCML (J = 1)			1,500			1,500			1,700			ps
	LVDS and LVPECL (J = 1)			500			500			550			ps
	LVDS, LVPECL, HyperTransport technology (J = 2 through 10)			440			440			500			ps
Input jitter tolerance (peak-to-peak)	All					250			250			250	ps
Output jitter (peak-to-peak)	All					160			160			200	ps
Output t_{RISE}	LVDS			80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology			110	170	200	110	170	200	120	170	200	ps
	LVPECL			90	130	150	90	130	150	100	135	150	ps
	PCML			80	110	135	80	110	135	80	110	135	ps

7. Reference & Ordering Information

SGX51007-1.0

Software

Stratix® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes hardware description language and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® logic analysis, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v6.2 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Stratix GX devices will be released on the Altera web site (**www.altera.com**).

Ordering Information

Figure 7–1 describes the ordering codes for Stratix GX devices.

Figure 7–1. Stratix GX Device Packaging Ordering Information