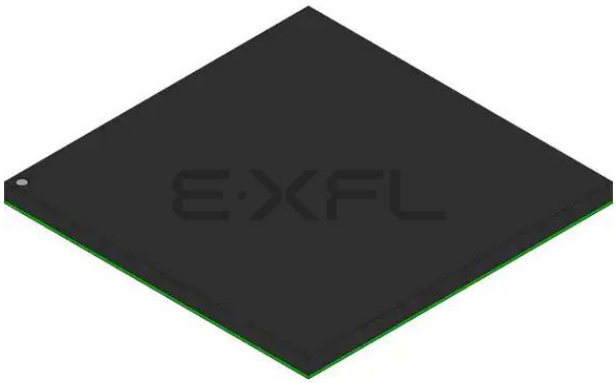

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

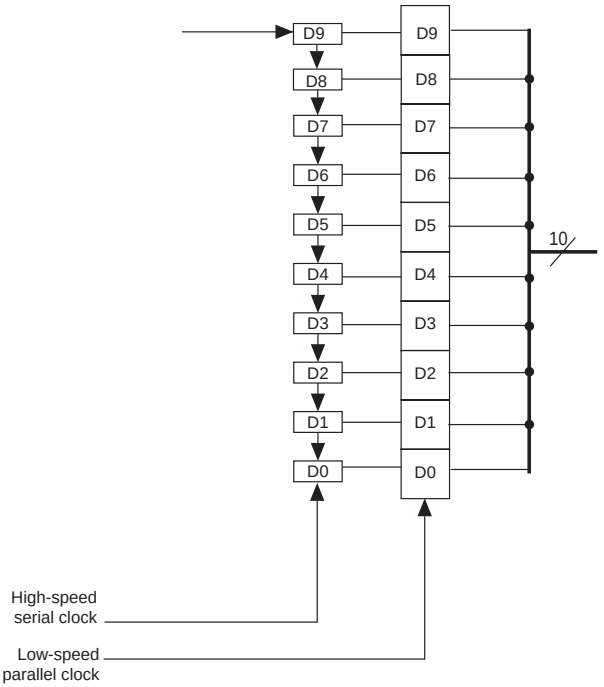
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx25cf672c5

Deserializer (Serial-to-Parallel Converter)

The deserializer converts the serial stream into a parallel 8- or 10-bit data bus. The deserializer receives the least significant bit first. Figure 2–14 is a diagram of the deserializer.

Figure 2–14. Deserializer



Word Aligner

The word aligner aligns the incoming data based on the specific byte boundaries. The word aligner has three customizable modes of operation: bit-slip mode, 16-bit mode, and 10-bit mode, the last of which is available for the basic and SONET modes. The word aligner also has two non-customizable modes of operation, which are the XAUI and GIGE modes.

Figure 2–15 shows the word aligner in bit-slip mode.

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 2 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 16-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 20-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111
Incremental 10-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
Incremental 20-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
High frequency	1010101010		
Low frequency	0011111000		
Mixed frequency	0011111010 or 1100000101		

Note to Table 2–9:
(1) This output repeats.

Stratix GX Clocking

The Stratix GX global clock can be driven by certain REFCLKB pins, all transmitter PLL outputs, and all receiver PLL outputs. The REFCLKB pins (except for transceiver block 0 and transceiver block 4) can drive inter-transceiver and global clock lines as well as feed the transmitter and receiver PLLs. The output of the transmitter PLL can only feed global clock lines and the reference clock port of the receiver PLL.

Figures 2–26 and 2–27 are diagrams of the Inter-Transceiver line connections as well as the global clock connections for the EP1SGX25F and EP1SGX40G devices. For devices with fewer transceivers, ignore the information about the unavailable transceiver blocks.

Table 4–2. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Configurations	512 ×1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 4–2:

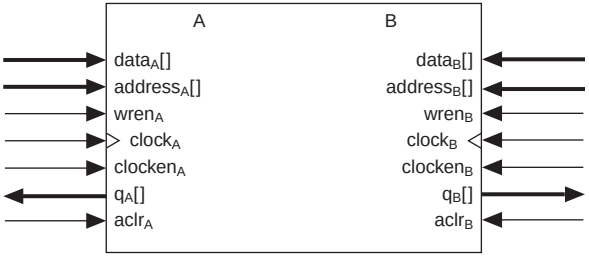
(1) See the *DC & Switching Characteristics* chapter of the *Stratix GX Device Handbook, Volume 1* for maximum performance information.

(2) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix GX device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Modes

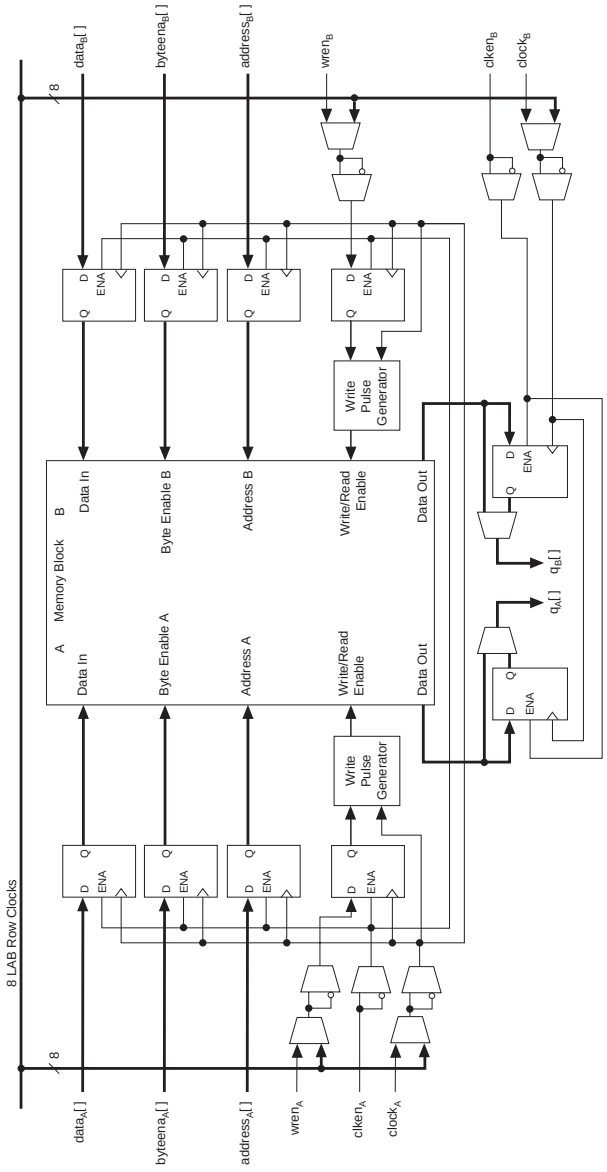
TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K and M-RAM memory blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 4–11 shows true dual-port memory.

Figure 4–11. True Dual-Port Memory Configuration



In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write and can either read old data before the write

Figure 4–24. Input/Output Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 4–24:

(1) All registers shown have asynchronous clear ports.

the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 4–28 shows one of the columns with surrounding LAB rows.

Figure 4–30. DSP Block Diagram for 9 × 9-Bit Configuration

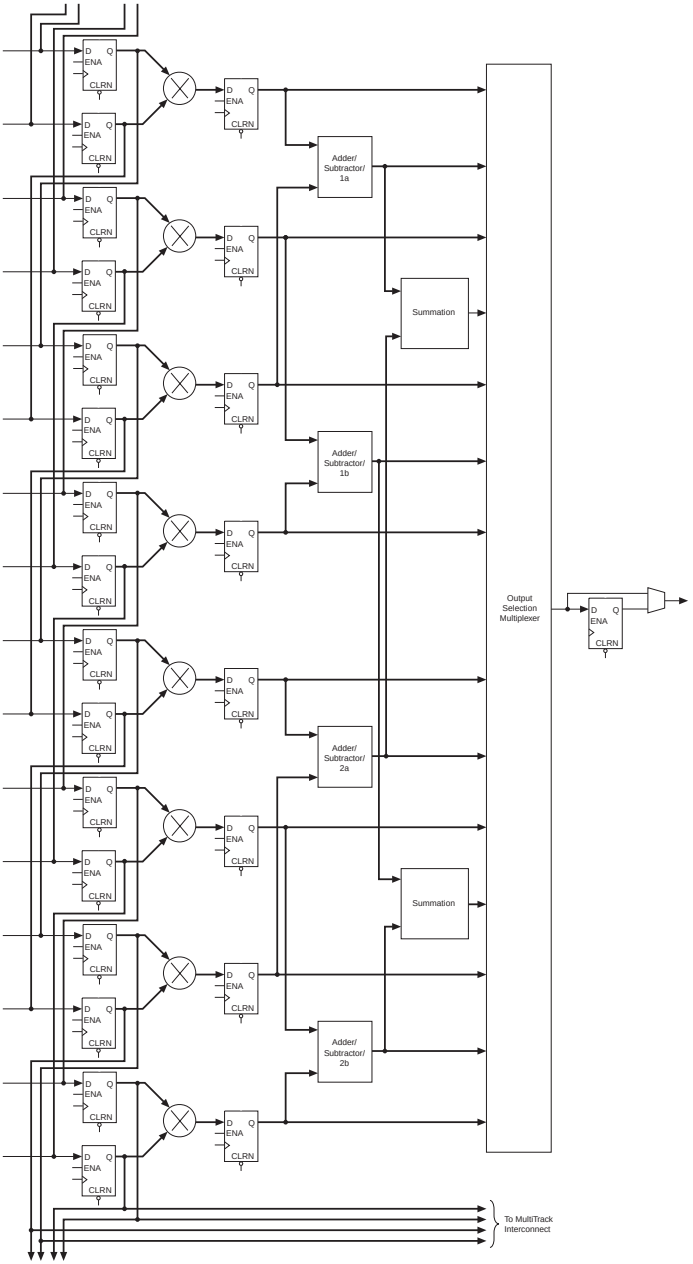
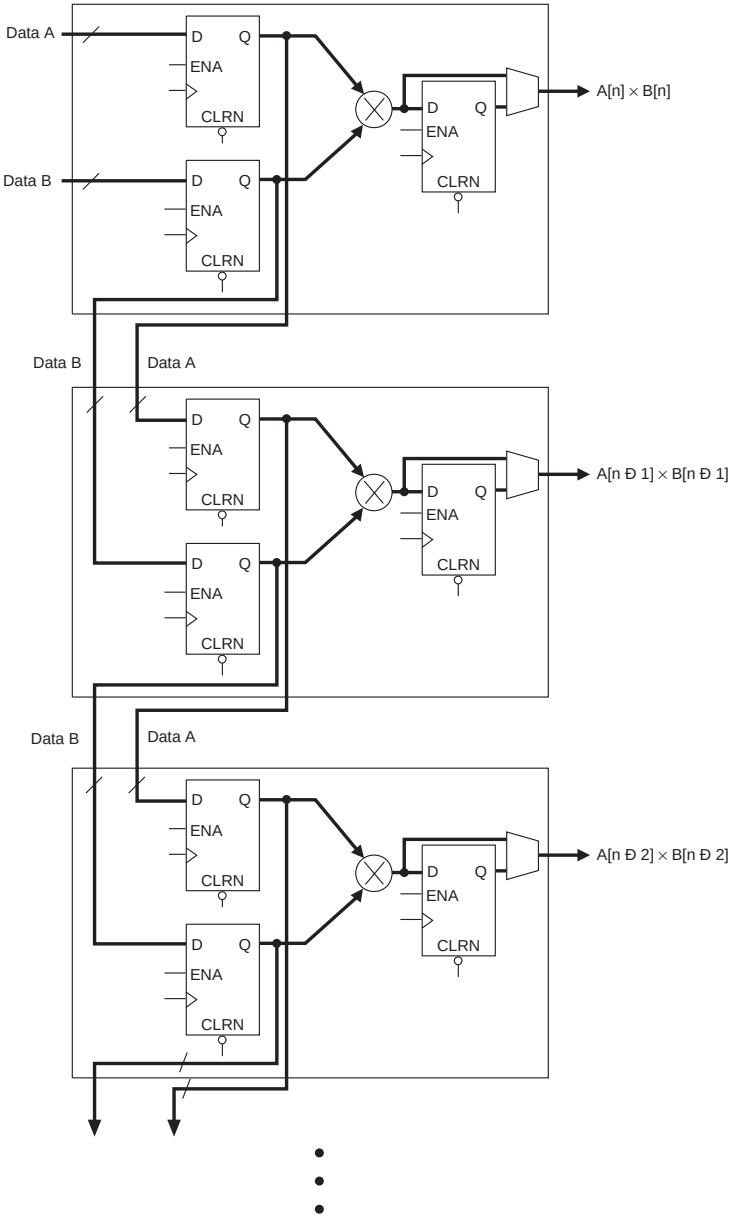


Figure 4–32. Multiplier Sub-Blocks Using Input Shift Register Connections *Note (1)*



Note to Figure 4–32:
(1) Either Data A or Data B input can be set to a parallel input for constant coefficient multiplication.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

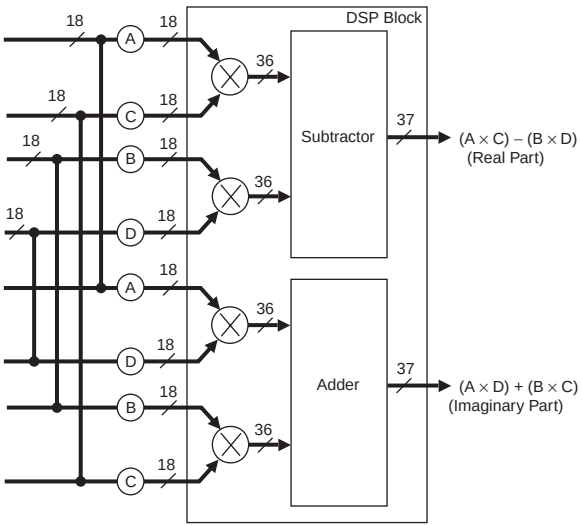
In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18 × 18-bit multipliers or eight 9 × 9-bit multipliers can drive their results directly out of one DSP block. See Figure 4–34.

You can use the two-multipliers adder mode for complex multiplications, which are written as:

$$(a + jb) \times (c + jd) = [(a \times c) - (b \times d)] + j \times [(a \times d) + (b \times c)]$$

The two-multipliers adder mode allows a single DSP block to calculate the real part $[(a \times c) - (b \times d)]$ using one subtractor and the imaginary part $[(a \times d) + (b \times c)]$ using one adder, for data widths up to 18 bits. Two complex multiplications are possible for data widths up to 9 bits using four adder/subtractor/accumulator blocks. Figure 4–37 shows an 18-bit two-multipliers adder.

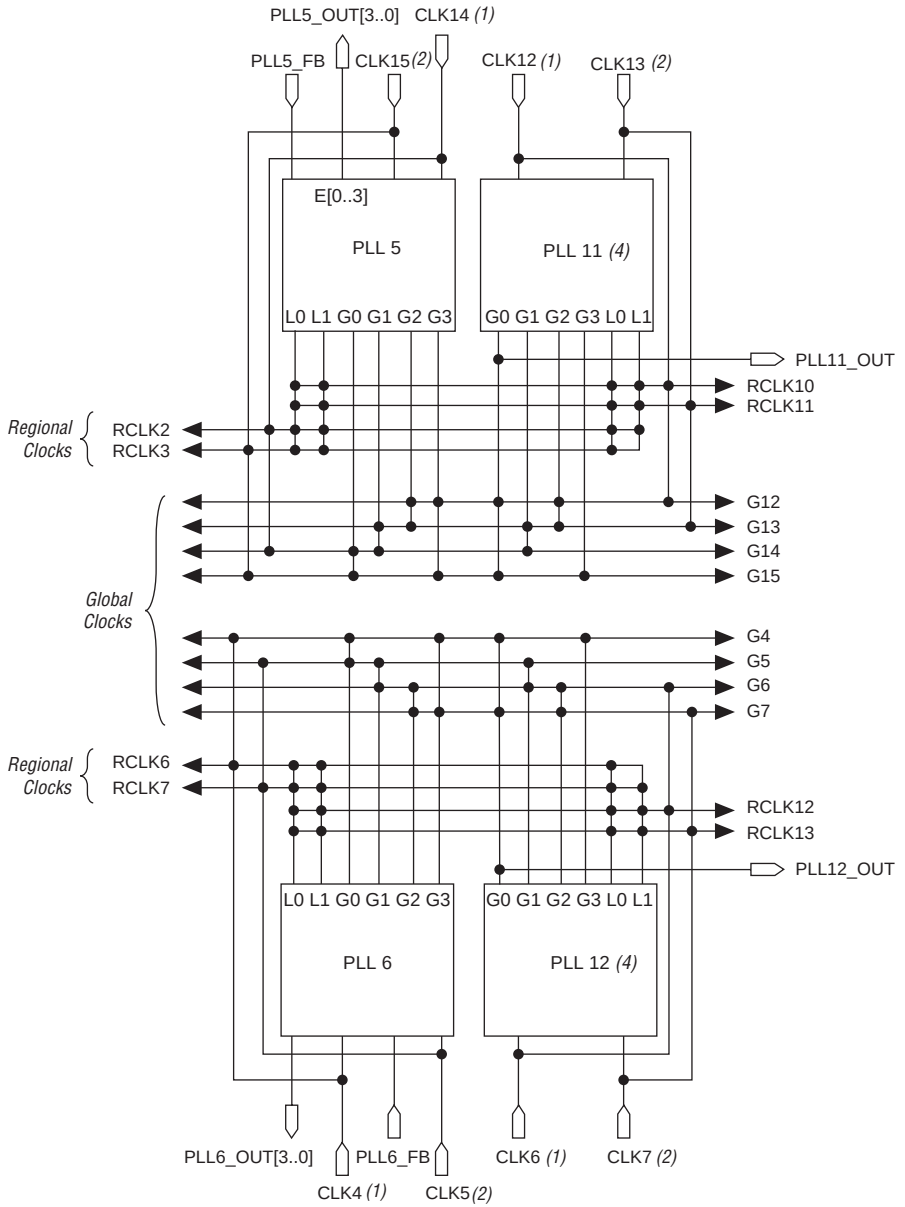
Figure 4–37. Two-Multipliers Adder Mode Implementing Complex Multiply



Four-Multipliers Adder Mode

In the four-multipliers adder mode, the DSP block adds the results of two first -stage adder/subtractor blocks. One sum of four 18 × 18-bit multipliers or two different sums of two sets of four 9 × 9-bit multipliers can be implemented in a single DSP block. The product width for each multiplier must be the same size. The four-multipliers adder mode is useful for FIR filter applications. Figure 4–38 shows the four multipliers adder mode.

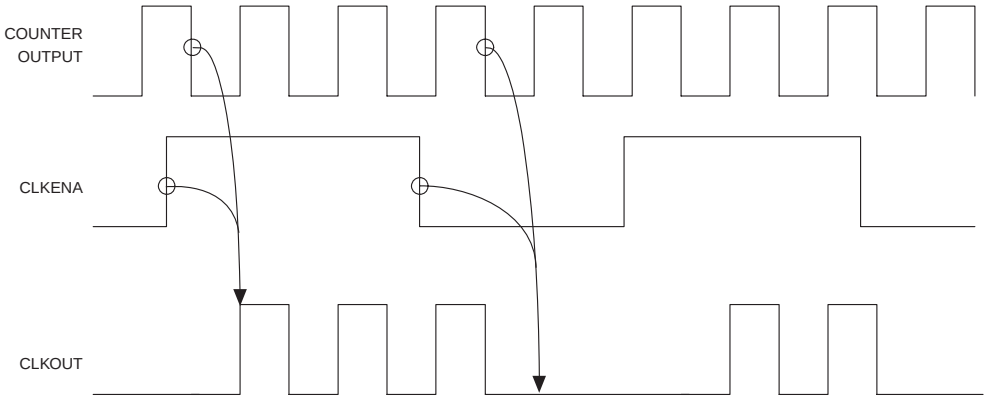
Figure 4–50. Global & Regional Clock Connections From Top Clock Pins & Enhanced PLL Outputs *Note (1)*



Note to Figure 4–50:
(1) PLLs 5, 6, 11, and 12 are enhanced PLLs.

unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

Figure 4–56. extclkena Signals



Fast PLLs

Stratix GX devices contain up to four fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 4–57 shows a diagram of the fast PLL.

Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 2 of 2) *Note (7), (12), (13)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C

Table 6–3. Stratix GX Device DC Operating Conditions *Note (12)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 6–4. Stratix GX Transceiver Block Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	2.4	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCG}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
Receiver input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V
`refclkb` input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V

Table 6–32. CTT I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤ V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 6–33. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	25		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–25		–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		–160		–200		–300		–500	µA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Tables 6–14 through 6–33:

(1) Drive strength is programmable according to values in the *Stratix GX Architecture* chapter of the *Stratix GX Device Handbook, Volume 1*.

(2) V_{REF} specifies the center point of the switching range.

Power Consumption

Detailed power consumption information for Stratix GX devices will be released when available.

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Table 6–35. Stratix GX Device Performance (Part 2 of 3) *Notes (1), (2)*

Applications		Resources Used			Performance			
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
TriMatrix memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	317.76	277.62	241.48	MHz
	FIFO 32 × 18 bit	30	1	0	319.18	278.86	242.54	MHz
TriMatrix memory M4K block	Simple dual-port RAM 128 × 36 bit	0	1	0	290.86	255.55	222.27	MHz
	True dual-port RAM 128 × 18 bit	0	1	0	290.86	255.55	222.27	MHz
	FIFO 128 × 36 bit	34	1	0	290.86	255.55	222.27	MHz
TriMatrix memory M-RAM block	Single port RAM 4K × 144 bit	1	1	0	255.95	223.06	194.06	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	MHz
	Single port RAM 8K × 72 bit	0	1	0	278.94	243.19	211.59	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	MHz
	Single port RAM 16K × 36 bit	0	1	0	280.66	254.32	221.28	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	MHz

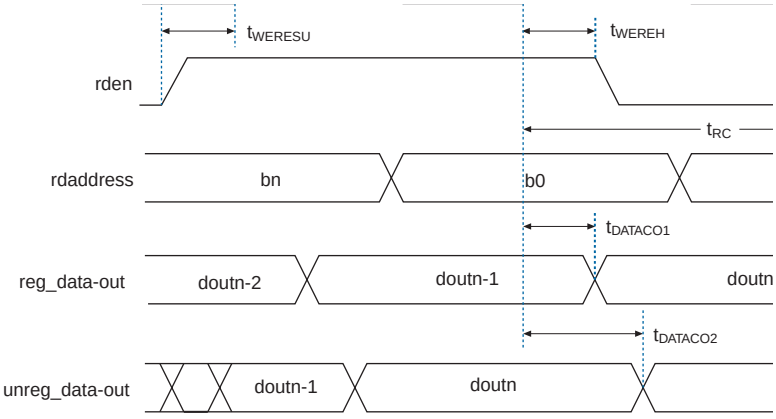
Table 6–38. DSP Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{SU}	Input, pipeline, and output register setup time before clock
t_{H}	Input, pipeline, and output register hold time after clock
t_{CO}	Input, pipeline, and output register clock-to-output delay
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode
$t_{PIPE2OUTREG4ADD}$	DSP Block Pipeline Register to output register delay in four-multipliers adder mode
t_{PD9}	Combinational input to output delay for 9 × 9-bit mode
t_{PD18}	Combinational input to output delay for 18 × 18-bit mode
t_{PD36}	Combinational input to output delay for 36 × 36-bit mode
t_{CLR}	Minimum clear pulse width
t_{CLKHL}	Minimum clock high or low time

Table 6–39. M512 Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Minimum clock high or low time
$t_{M512CLR}$	Minimum clear pulse width

Table 6–40. M4K Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width

Table 6–41. M-RAM Block Internal Timing Microparameter Descriptions (Part 1 of 2)	
Symbol	**Parameter**
t_{MRAMRC}	Synchronous read cycle time
t_{MRAMWC}	Synchronous write cycle time
$t_{MRAMWERESU}$	Write or read enable setup time before clock
$t_{MRAMWEREH}$	Write or read enable hold time after clock
$t_{MRAMBESU}$	Byte enable setup time before clock
$t_{MRAMBEH}$	Byte enable hold time after clock
$t_{MRAMDATAASU}$	A port data setup time before clock
$t_{MRAMDATAAH}$	A port data hold time after clock
$t_{MRAMADDRASU}$	A port address setup time before clock
$t_{MRAMADDRAH}$	A port address hold time after clock

Figure 6–5. Stratix GX Transceiver Reset & PLL Lock Time Waveform *Note (1)*



Note to Figure 6–5:

(1) Waveforms are for minimum pulse width timing and output timing only. Please refer to the *Stratix GX Transceiver User Guide* for the complete reset sequence.

Tables 6–44 through 6–50 show the internal timing microparameters for all Stratix GX devices.

Table 6–44. LE Internal Timing Microparameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	10		10		11		ps
t_{H}	100		100		114		ps
t_{CO}		156		176		202	ps
t_{LUT}		366		459		527	ps
t_{CLR}	100		100		114		ps
t_{PRE}	100		100		114		ps
t_{CLKHL}	100		100		114		ps

Table 6–47. M512 Block Internal Timing Microparameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{M512RC}		3,340		3,816		4,387	ps
t_{M512WC}		3,318		3,590		4,128	ps
$t_{M512WERESU}$	110		123		141		ps
$t_{M512WERH}$	34		38		43		ps
$t_{M512DATASU}$	110		123		141		ps
$t_{M512DATAH}$	34		38		43		ps
$t_{M512WADDRASU}$	110		123		141		ps
$t_{M512WADDRH}$	34		38		43		ps
$t_{M512DATACO1}$		424		472		541	ps
$t_{M512DATACO2}$		3,366		3,846		4,421	ps
$t_{M512CLKHL}$	150		167		192		ps
$t_{M512CLR}$	170		189		217		ps

Table 6–48. M4K Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{M4KRC}		3,807		4,320		4,967	ps
t_{M4KWC}		2,556		2,840		3,265	ps
$t_{M4KWERESU}$	131		149		171		ps
$t_{M4KWERH}$	34		38		43		ps
$t_{M4KDATASU}$	131		149		171		ps
$t_{M4KDATAH}$	34		38		43		ps
$t_{M4KWADDRASU}$	131		149		171		ps
$t_{M4KWADDRH}$	34		38		43		ps
$t_{M4KRADDRASU}$	131		149		171		ps
$t_{M4KRADDRH}$	34		38		43		ps
$t_{M4KDATABSU}$	131		149		171		ps
$t_{M4KDATABH}$	34		38		43		ps
$t_{M4KADDRBSU}$	131		149		171		ps
$t_{M4KADDRBH}$	34		38		43		ps

Table 6–50. Stratix GX Transceiver Reset & PLL Lock Time Parameters

Symbol	Min	Typ	Max	Units
$t_{ANALOGRESETPW}$ (5)	1			mS
$t_{DIGITALRESETPW}$ (5)	4			Parallel clock cycle
$t_{TX\_PLL\_LOCK}$ (3)			10	µS
$t_{RX\_FREQLOCK}$ (4)			5	mS
$t_{RX\_FREQLOCK2PHASELOCK}$ (2)			5	µS

Notes to Table 6–50:

(1) The minimum pulse width specified is associated with the power-down of circuits.

(2) The clock recovery unit (CRU) phase locked-to-data time is based on a data rate of 500 Mbps and 8B/10B encoded data.

(3) After `#pll_areset`, `pll_enable`, or PLL power-up, the time required for the transceiver PLL to lock to the reference clock.

(4) After `#rx_analogreset`, the time for the CRU to switch to lock-to-data mode.

(5) There is no maximum pulse width specification. The GXB can be held in reset indefinitely.

Routing delays vary depending on the load on a specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design. Contact Altera Applications Engineering for more details.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 6–6 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.