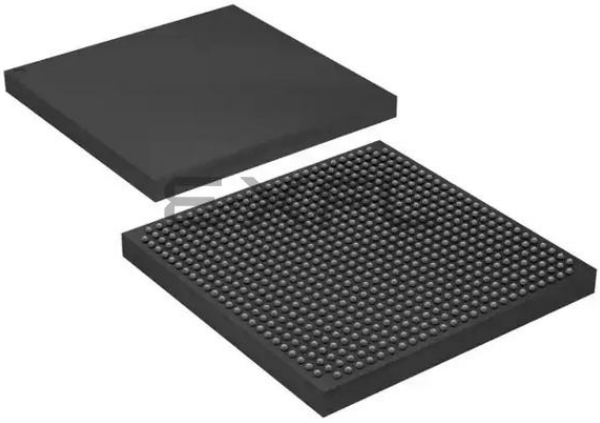

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

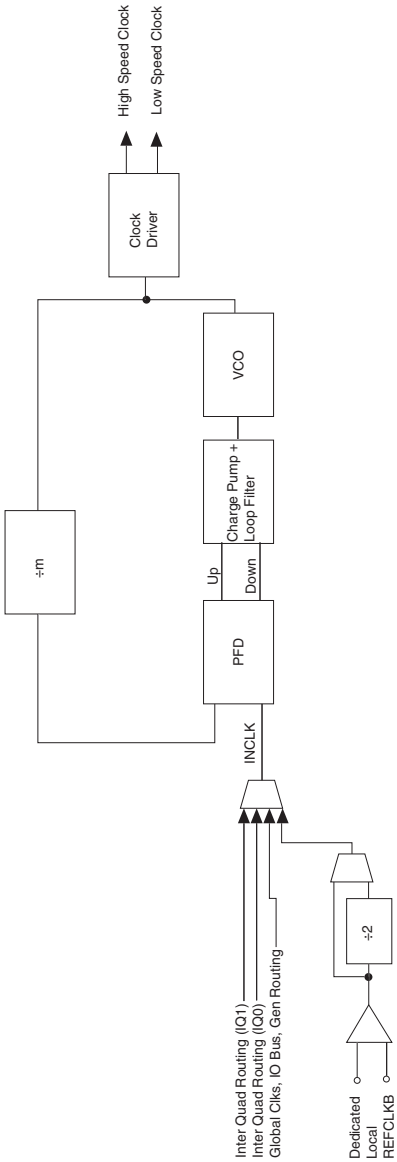
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx25cf672c6n

Figure 2–3. Transmitter PLL Block Diagram *Note (1)*



Note to Figure 2–3:
(1) The divider in the PLL divides by 4, 8, 10, 16, or 20.

The actual lock time for different data patterns varies depending on the data's transition density (how often the data switches between 1 and 0) and jitter characteristic. The DPA circuitry is designed to lock onto any data pattern with sufficient transition density, so the circuitry works with current and future protocols. Experiments and simulations show that the DPA circuitry locks when the data patterns listed in Table 3–4 are repeated for the specified number of times. There are other suitable patterns not shown in Table 3–4 and/or pattern lengths, but the lock time may vary. The circuit can adjust for any phase variation that may occur during operation.

Table 3–4. Training Patterns for Different Protocols

Protocols	Training Pattern	Number of Repetitions
SPI-4, NPSI	Ten 0's, ten 1's (00000000001111111111)	256
RapidIO	Four 0's, four 1's (00001111) or one 1, two 0's, one 1, four 0's (10010000)	
Other designs	Eight alternating 1's and 0's (10101010 or 01010101)	
SFI-4, XSBI	Not specified	

Phase Synchronizer

Each receiver has its own phase synchronizer. The receiver phase synchronizer aligns the phase of the parallel data from all the receivers to one global clock. The synchronizers in each channel consist of a 4-bit deep and *J*-bit wide FIFO buffer. The parallel clock writes to the FIFO buffer and the global clock (GCLK) reads from the FIFO buffer. The global and parallel clock inputs into the synchronizers must have identical frequencies and differ only in phase. The FIFO buffer never becomes full or empty (because the source and receive signals are frequency locked) when operating within the DPA specifications, and the operation does not require an empty/full flag or read/write enable signals.

Receiver Data Realignment In DPA Mode

While DPA operation aligns the incoming clock phase to the incoming data phase, it does not guarantee the parallelization boundary or byte boundary. When the dynamic phase aligner realigns the data bits, the bits may be shifted out of byte alignment, as shown in Figure 3–10.

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 4–4 and 4–5 summarize the possible M4K RAM block configurations.

Table 4–4. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K 1	2K × 2	1K ° 4	512 ° 8	256 ° 16	128 ° 32	512 ° 9	256 ° 18	128 ° 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 4–5. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 4–6 summarizes the byte selection.

Table 4–6. Byte Enable for M4K Blocks Notes (1), (2)

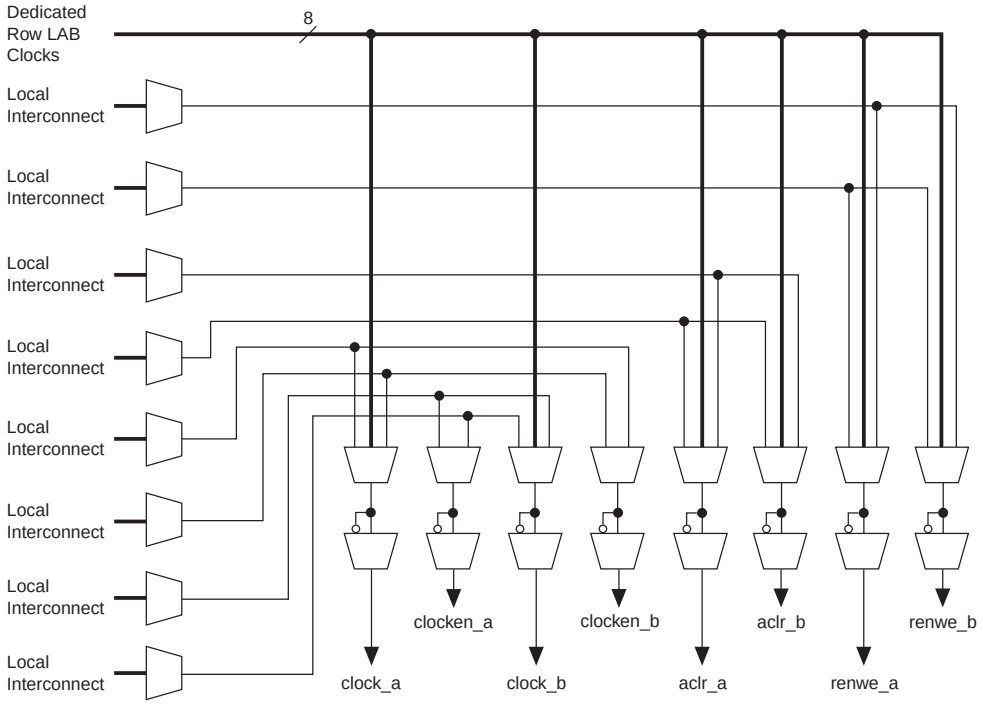
byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 4–6:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, that is, in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 4–16.

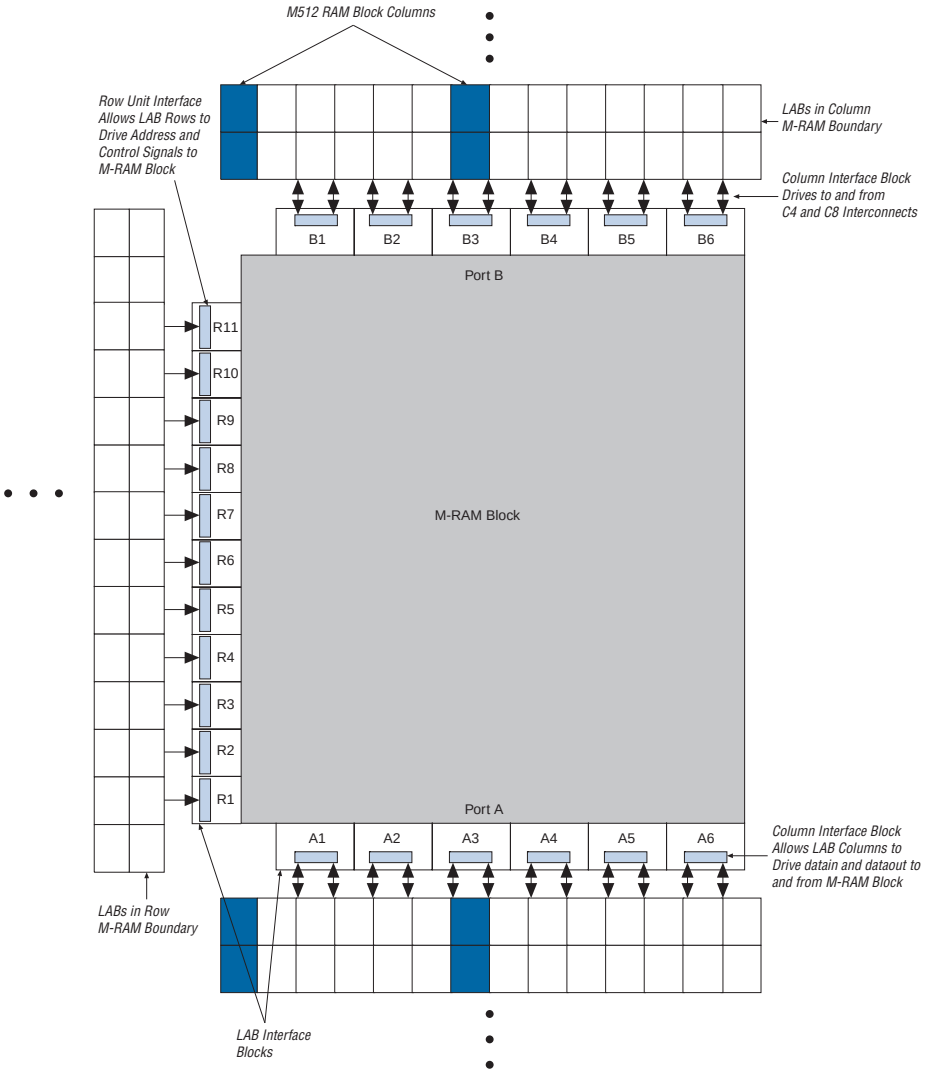
The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 4–17 shows the M4K RAM block to logic array interface.

Figure 4–18. M-RAM Block Control Signals



One of the M-RAM block's horizontal sides drive the address and control signal (clock, `renwe`, `byteena`, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 4–19 shows an example floorplan for the EP1SGX40 device and the location of the M-RAM interfaces.

Figure 4–20. Left-Facing M-RAM to Interconnect Interface *Notes (1), (2)*



Notes to Figure 4–20:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 4–24 and 4–25 show the memory block in input/output clock mode.

Figure 4–29. DSP Block Diagram for 18 × 18-Bit Configuration

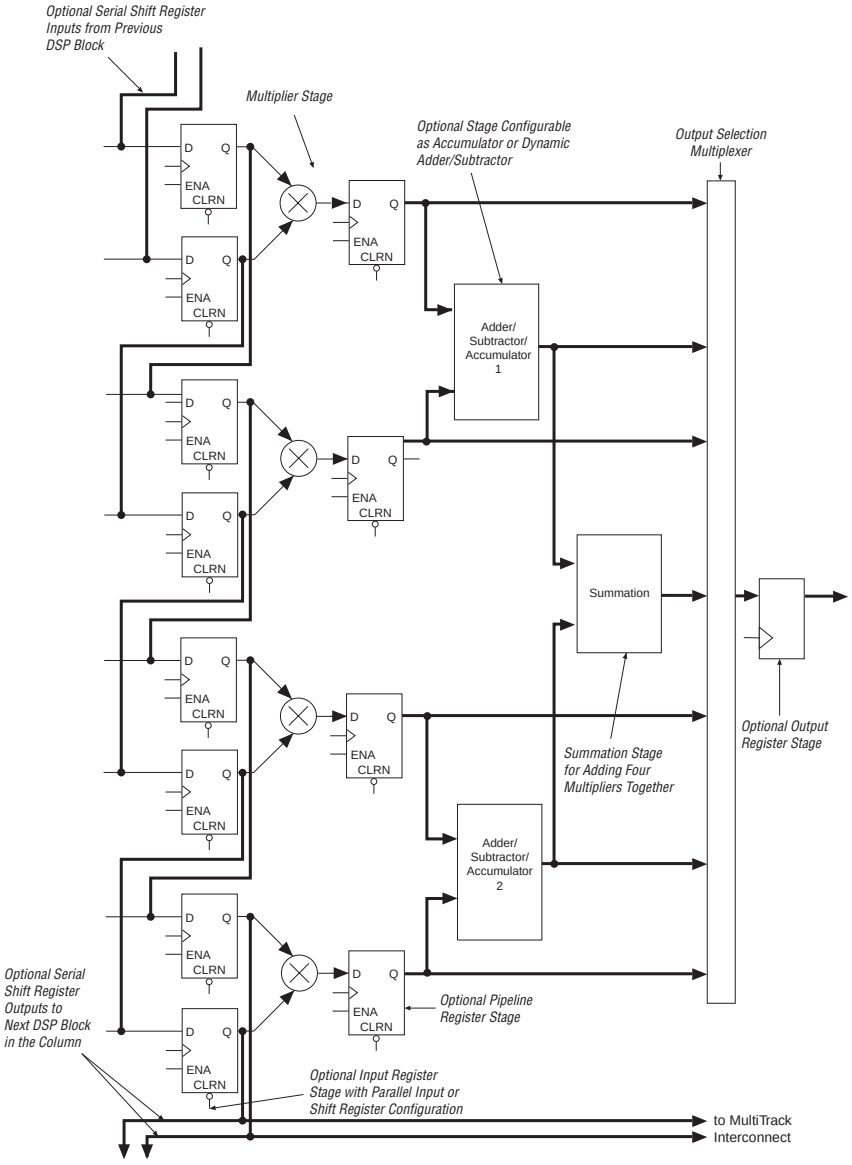


Table 4–13 shows the summary of input register modes for the DSP block.

Table 4–13. Input Register Modes

Register Input Mode	9 × 9	18 × 18	36 × 36
Parallel input	✓	✓	✓
Shift register input	✓	✓	

Multiplier

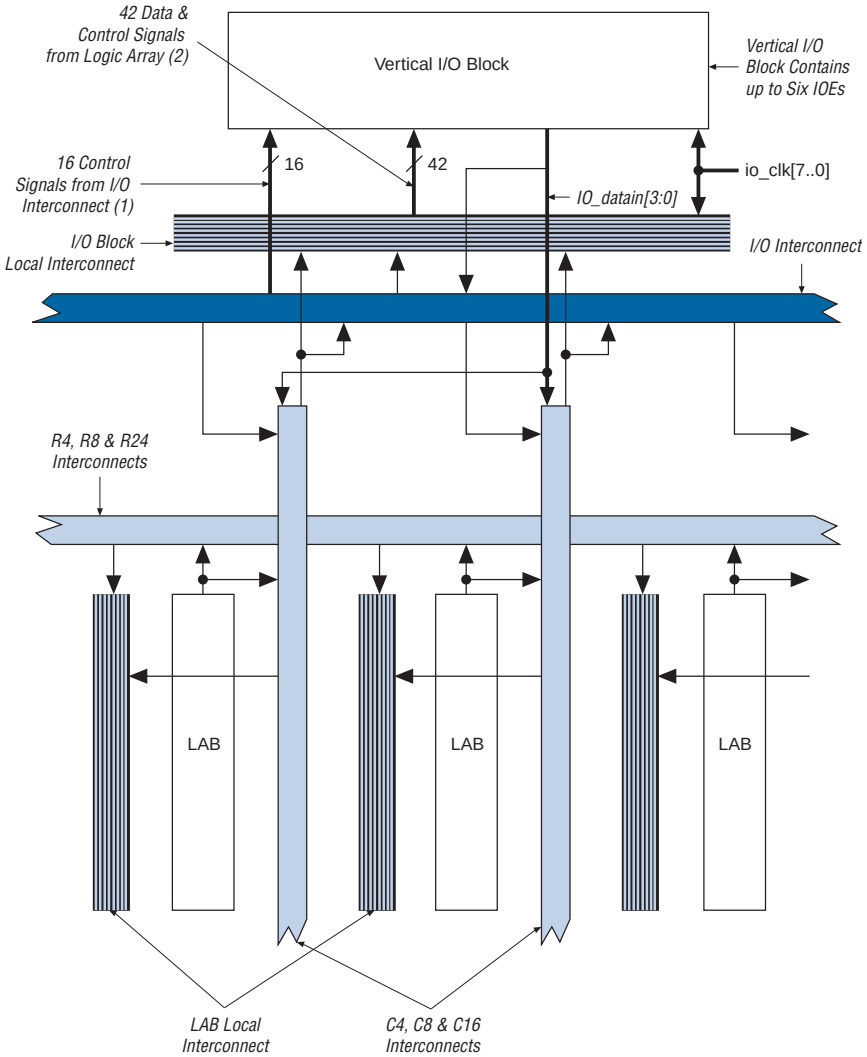
The multiplier supports 9 × 9-, 18 × 18-, or 36 × 36-bit multiplication. Each DSP block supports eight possible 9 × 9-bit or smaller multipliers. There are four multiplier blocks available for multipliers larger than 9 × 9 bits but smaller than 18 × 18 bits. There is one multiplier block available for multipliers larger than 18 × 18 bits but smaller than or equal to 36 × 36 bits. The ability to have several small multipliers is useful in applications such as video processing. Large multipliers greater than 18 × 18 bits are useful for applications such as the mantissa multiplication of a single-precision floating-point number.

The multiplier operands can be signed or unsigned numbers, where the result is signed if either input is signed as shown in Table 4–14. The `sign_a` and `sign_b` signals provide dynamic control of each operand's representation: a logic 1 indicates the operand is a signed number, a logic 0 indicates the operand is an unsigned number. These sign signals affect all multipliers and adders within a single DSP block and you can register them to match the data path pipeline. The multipliers are full precision (that is, 18 bits for the 18-bit multiply, 36-bits for the 36-bit multiply, and so on), regardless of whether `sign_a` or `sign_b` set the operands as signed or unsigned numbers.

Table 4–14. Multiplier Signed Representation

Data A	Data B	Result
Unsigned	Unsigned	Unsigned
Unsigned	Signed	Signed
Signed	Unsigned	Signed
Signed	Signed	Signed

Figure 4–60. Column I/O Block Connection to the Interconnect



Notes to Figure 4–60:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

Table 4–28. I/O Support by Bank (Part 2 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
SSTL-3 class II	✓	✓	✓
AGP (1× and 2×)	✓		✓
CTT	✓	✓	✓

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated VREF pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Differential On-Chip Termination

Stratix GX devices provide differential on-chip termination (LVDS I/O standard) to reduce reflections and maintain signal integrity. Differential on-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections. The internal termination is designed using transistors in the linear region of operation.

Stratix GX devices support internal differential termination with a nominal resistance value of 137.5 Ω for LVDS input receiver buffers. LVPECL signals require an external termination resistor. Figure 4–70 shows the device with differential termination.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Stratix GX devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix GX devices can also use the JTAG port for configuration together with either the Quartus II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix GX devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode. You can use this ability for JTAG testing before configuration when some of the Stratix GX pins drive or receive from other devices on the board using voltage-referenced standards. Because the Stratix GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows you to fully test I/O connection to other devices.

The enhanced PLL reconfiguration bits are part of the JTAG chain before configuration and after power-up. After device configuration, the PLL reconfiguration bits are not part of the JTAG chain.

Stratix GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® embedded logic analyzer. Stratix GX devices support the JTAG instructions shown in Table 4–33.

Table 4–33. Stratix GX JTAG Instructions (Part 1 of 2)

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap® embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

SRAM configuration elements allow Stratix GX devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

Configuration Schemes

You can load the configuration data for a Stratix GX device with one of five configuration schemes (see Table 5–1), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix GX device. A configuration device can automatically configure a Stratix GX device at system power-up.

You can configure multiple Stratix GX devices in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 5–1. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	ByteBlasterMV™ or MasterBlaster™ download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file (.jam or .jbc)

6. DC & Switching Characteristics

SGX51006-1.2

Operating Conditions

Stratix® GX devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 6–1 through 6–12 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and transceiver block absolute maximum ratings. Notes for Tables 6–1 through 6–6 immediately follow Table 6–6, notes for Table 6–7 immediately follow that table, and notes for Tables 6–8 through 6–12 immediately follow Table 6–12.

Table 6–1. Stratix GX Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 1 of 2) *Note (7), (12), (13)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4), (5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3), (6)*	–0.5	4.1	V

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 7 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade (1)			-6 Commercial & Industrial Speed Grade (1)			-7 Commercial & Industrial Speed Grade (1)			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output return loss	100 MHz to 2.5 GHz	–10			–10			–10			dB

Notes to Table 6–7:

(1) All numbers for the -6 and -7 speed grades are for both commercial and industrial unless specified otherwise in the Conditions column. Speed grade -5 is available only for commercial specifications.
(2) Not all V_{ID} and equalizer values will get the same results. The condition for the specification was that the V_{ID} before jitter was added is 1,000 mV and the equalizer was set to the maximum condition of 111 (equalizer control setting = 4 in the MegaWizard Plug-In Manager).
(3) Number of parallel clocks.
(4) Receive latency delay from serial receiver indata to parallel receiver data.
(5) Per IEEE Standard 802.3ae @ 3.125 for –5 and –6.
(6) The specification is for channel aligner tolerance.
(7) UI = Unit Interval.
(8) Run-length conditions are true for all data rates, but the average transition density must be enough to keep the receiver phase aligned and the overall data must be DC balanced.
(9) Not all combinations of V_{OD} and pre-emphasis will get the same results.
(10) The numbers are for 3.125-Gbps data rate for –5 and –6 devices and 2.5 Gbps for –7 devices.
(11) Transmitter latency delay from parallel transceiver data to serial transceiver out data.
(12) The receiver operates with a BER of better than 10^{-12} in the presence of an input signal as defined in the XAUI driver template for 3.125 Gbps and in the PCI Exp transmitter eye mask for 2.5 Gbps.

Table 6–8. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA (1)	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA (1)		0.45	V

Table 6–9. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V

Table 6–16. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage (single ended)	R_L = 100 Ω	380	485	820	mV
ΔV_{OD}	Change in between high and low	R_L = 100 Ω			50	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	650	780	mV
ΔV_{OCM}	Change in between high and low	R_L = 100 Ω			50	mV
V_{ID}	Differential input voltage swing (single-ended)		300		900	mV
V_{ICM}	Input common mode voltage		300		900	mV
R_L	Receiver differential input resistor, external		90	100	110	Ω

Table 6–17. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 6–18. PCI-X Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V

Table 6–26. SSTL-3 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(1)*			V_{TT} – 0.8	V

Table 6–27. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		0.39 × V_{CCIO}		0.41 × V_{CCIO}	V
V_{IH}	High-level input voltage *(2)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(2)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			0.1 × V_{CCIO}	V

Table 6–28. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(2)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(2)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			0.1 × V_{CCIO}	V

Table 6–29. 1.5-V HSTL Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.245		2.332		2.666		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.597	2.000	4.920	2.000	5.635	ns

Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.114		2.218		2.348		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.728	2.000	5.078	2.000	6.004	ns
$t_{INSUPLL}$	1.035		0.941		1.070		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.629	0.500	2.769	0.500	3.158	ns

Table 6–77. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,930		2,031		2,335	ps
	4 mA		1,930		2,031		2,335	ps
	8 mA		1,710		1,800		2,069	ps
	12 mA		1,490		1,569		1,803	ps
3.3-V LVTTL	4 mA		1,953		2,055		2,363	ps
	8 mA		1,733		1,824		2,097	ps
	12 mA		1,513		1,593		1,831	ps
	16 mA		1,453		1,530		1,759	ps
2.5-V LVTTL	2 mA		2,632		2,769		3,183	ps
	8 mA		2,052		2,160		2,483	ps
	12 mA		1,942		2,044		2,350	ps
	16 mA		1,902		2,002		2,301	ps
1.8-V LVTTL	2 mA		4,537		4,773		5,489	ps
	8 mA		3,447		3,628		4,172	ps
	12 mA		3,377		3,555		4,088	ps
1.5-V LVTTL	2 mA		6,575		6,917		7,954	ps
	4 mA		5,995		6,308		7,253	ps
	8 mA		5,525		5,815		6,686	ps
CTT			1,410		1,485		1,707	ps
SSTL-3 class I			1,450		1,527		1,755	ps
SSTL-3 class II			1,310		1,380		1,586	ps
SSTL-2 class I			1,797		1,892		2,175	ps
SSTL-2 class II			1,717		1,808		2,079	ps
LVDS *(1)*			1,340		1,411		1,622	ps
LVPECL *(1)*			1,400		1,474		1,694	ps
3.3-V PCML *(1)*			1,300		1,369		1,573	ps
HyperTransport technology *(1)*			1,430		1,506		1,731	ps

Note to Tables 6–72 through 6–77:
(1) These parameters are only available on the left side row I/O pins.

Table 6–91 describes the Stratix GX device fast PLL specifications.

Table 6–91. Fast PLL Specifications for -5 & -6 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{IN}	CLKIN frequency (for *m* = 1) *(1)*	300	717	MHz
	CLKIN frequency (for *m* = 2 to 19)	300/*m*	1,000/*m*	MHz
	CLKIN frequency (for *m* = 20 to 32)	10	1,000/*m*	MHz
f_{OUT}	Output frequency for internal global or regional clock *(2)*	9.4	420	MHz
f_{OUT_EXT}	Output frequency for external clock	9.375	717	MHz
f_{VCO}	VCO operating frequency	300	1,000	MHz
t_{INDUTY}	CLKIN duty cycle	40	60	%
$t_{INJITTER}$	Period jitter for CLKIN pin		±200	ps
t_{DUTY}	Duty cycle for DFFIO 1× CLKOUT pin *(3)*	45	55	%
t_{JITTER}	Period jitter for DIFFIO clock out *(3)*		±80	ps
	Period jitter for internal global or regional clock		±100 ps for >200-MHz outclk ±20 mUI for <200-MHz outclk	ps or mUI
t_{LOCK}	Time required for PLL to acquire lock	10	100	µs
m	Multiplication factors for *m* counter *(3)*	1	32	Integer
*l*0, *l*1, *g*0	Multiplication factors for *l*0, *l*1, and *g*0 counter *(4)*, *(5)*	1	32	Integer
t_{ARESET}	Minimum pulse width on areset signal	10		ns

Table 6–92. Fast PLL Specifications for -7 & -8 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{IN}	CLKIN frequency (for *m* = 1) *(1)*,	300	640	MHz
	CLKIN frequency (for *m* = 2 to 19)	300/*m*	700/*m*	MHz
	CLKIN frequency (for *m* = 20 to 32)	10	700/*m*	MHz
f_{OUT}	Output frequency for internal global or regional clock *(2)*	9.375	420	MHz
f_{OUT_EXT}	Output frequency for external clock	9.4	500	MHz
f_{VCO}	VCO operating frequency	300	700	MHz
t_{INDUTY}	CLKIN duty cycle	40	60	%
$t_{INJITTER}$	Period jitter for CLKIN pin		±200	ps