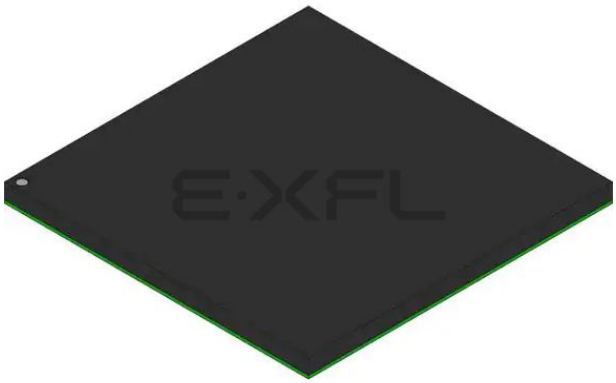

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx25cf672c7

2. Stratix GX Transceivers

SGX51002-1.1

Transceiver Blocks

Stratix® GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

There are up to 20 transceiver channels available on a single Stratix GX device. Table 2–1 shows the number of transceiver channels available on each Stratix GX device.

Table 2–1. Stratix GX Transceiver Channels

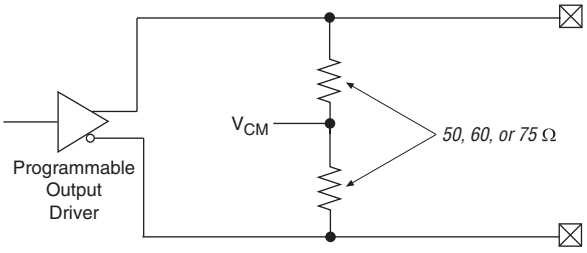
Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 2–1 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GIGE applications, in addition to channel bonding for XAUI applications.

Pre-emphasis percentage is defined as $V_{PP}/V_S - 1$, where V_{PP} is the differential emphasized voltage (peak-to-peak) and V_S is the differential steady-state voltage (peak-to-peak).

Programmable Transmitter Termination
The programmable termination can be statically set in the Quartus II software. The values are 100 Ω, 120 Ω, 150 Ω, and off. Figure 2–9 shows the setup for programmable termination.

Figure 2–9. Programmable Transmitter Termination



Receiver Path

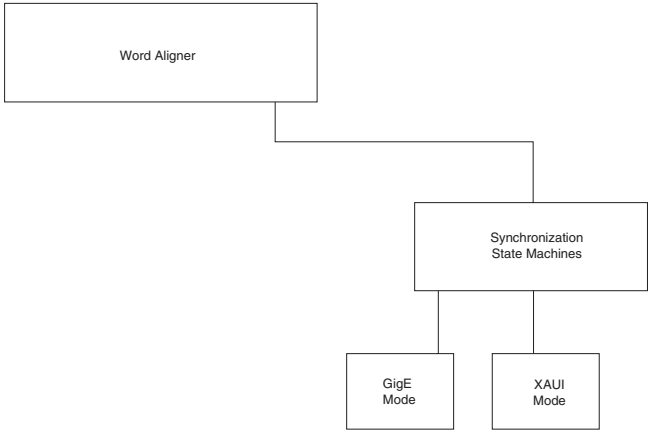
This section describes the data path through the Stratix GX receiver (refer to Figure 2–2 on page 2–4). Data travels through the Stratix GX receiver via the following modules:

- Input buffer
- Clock Recovery Unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

Receiver Input Buffer

The Stratix GX receiver input buffer supports the 1.5-V PCML I/O standard at a rate up to 3.1875 Gbps. Additional I/O standards, LVDS, 3.3-V PCML, and LVPECL can be supported when AC coupled. The common mode of the input buffer is 1.1 V. The receiver can support Stratix GX-to-Stratix GX DC coupling.

Figure 2–18. Word Aligner in XAUI Mode



In the XAUI and GIGE modes, the word alignment is controlled by a state machine that adheres to the IEEE 802.3ae standard for XAUI and the IEEE 802.3 standard for GIGE. The alignment pattern is predefined to be a /K28.5/ code group.

The XAUI mode is available only for the XAUI protocol, and the GIGE mode is available only for the GIGE protocol.

Channel Aligner

The channel aligner is available only in XAUI mode and bonds all four channels within a transceiver. The channel aligner adheres to the IEEE 802.3ae, clause 48 specification for channel bonding.

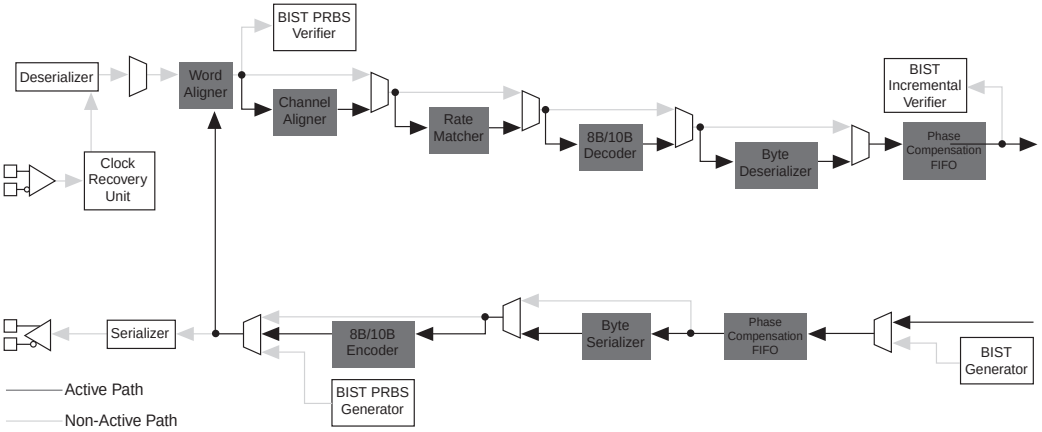
The channel aligner is a 16-word deep FIFO buffer with a state machine overlooking the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/s in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the rx_channelalign port goes high, signifying that all the channels in the transceiver have been bonded. The reception of four consecutive misaligned /A/s restarts the channel alignment sequence and de-asserts rx_channelalign.

Figure 2–19 shows misaligned channels before the channel aligner and the channel alignment after the channel aligner.

Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not use in the loopback path. The received data is not retimed. Figure 2–22 shows the data path in parallel loopback mode. This option is not dynamically switchable. Reception of an external signal is not possible in this mode.

Figure 2–22. Data Path in Parallel Loopback Mode



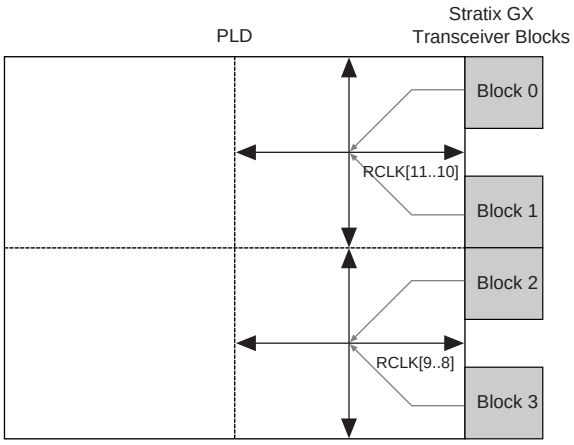
Reverse Serial Loopback

The reverse serial loopback exercises the analog portion of the transceiver. This loopback mode is dynamically switchable through the `tx_srlpbk` port on a channel by channel basis. Asserting `rxanalogreset` in reverse serial loopback mode powers down the receiver buffer and CRU, preventing data loopback. Figure 2–23 shows the data path in reverse serial loopback mode.

The receiver PLL can also drive the fast regional, regional clocks, and local routing adjacent to the associated transceiver block. Figures 2–28 through 2–31 show which fast regional and regional clock resource can be used by the recovered clock.

In the EP1SGX25 device, the receiver PLL recovered clocks from transceiver blocks 0 and 1 drive `RCLK[1..0]` while transceiver blocks 2 and 3 drive `RCLK[7..6]`. The regional clocks feed logic in their associated regions.

Figure 2–28. EP1SGX25 Receiver PLL Recovered Clock to Regional Clock Connection



In addition, the receiver PLL's recovered clocks can drive fast regional lines (`FCLK`) as shown Figure 2–29. The fast regional clocks can feed logic in their associated regions.

The logic array sends parallel data to the SERDES transmitter circuit when the TXLOADEN signal is asserted. This signal is generated by the high-speed counter circuitry of the logic array low-frequency clock's rising edge. The data is then transferred from the parallel register into the serial shift register by the TXLOADEN signal on the third rising edge of the high-frequency clock.

Figure 3–3 shows the block diagram of a single SERDES transmitter channel and Figure 3–4 shows the timing relationship between the data and clocks in Stratix GX devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

Figure 3–3. Stratix GX High-Speed Interface Serialized in ×10 Mode

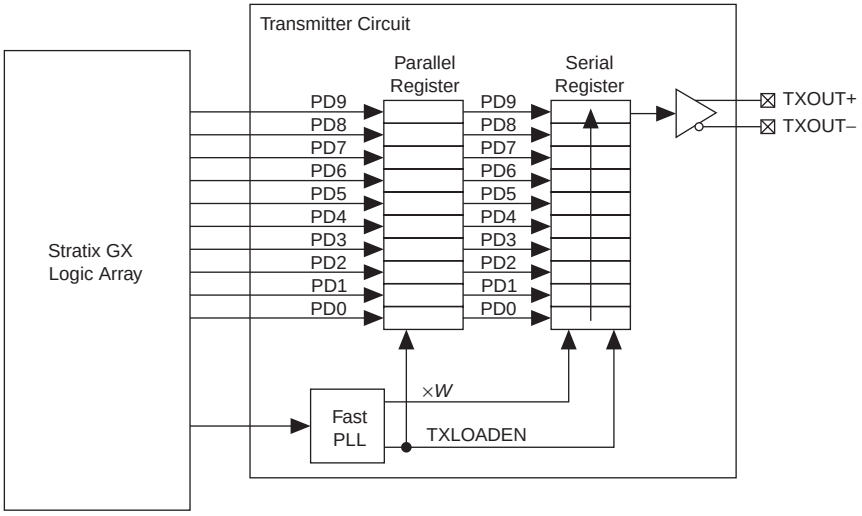
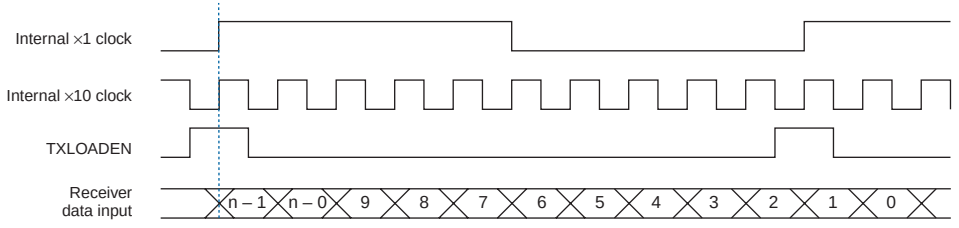


Figure 3–4. Transmitter Timing Diagram

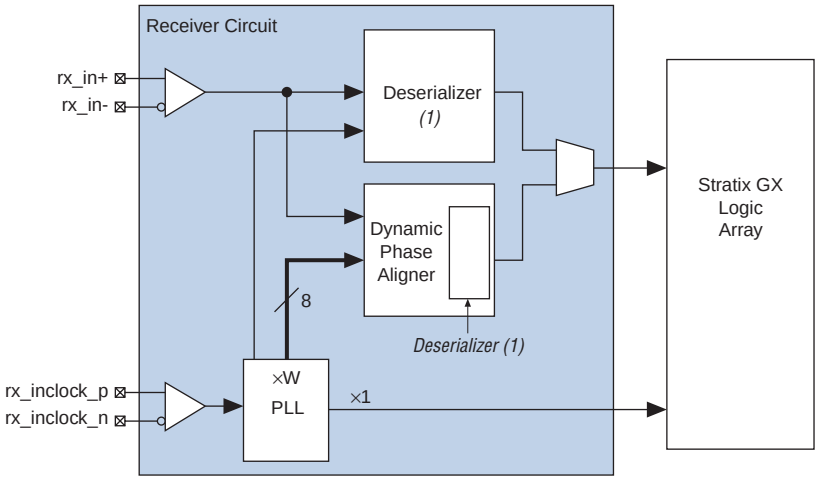


DPA Block Overview

Each Stratix GX receiver channel features a DPA block. The block contains a dynamic phase selector for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel by using a separate deserializer shown in Figure 3–5.

The dynamic phase aligner uses both the source clock and the serial data. The dynamic phase aligner automatically and continuously tracks fluctuations caused by system variations and self-adjusts to eliminate the phase skew between the multiplied clock and the serial data. Figure 3–5 shows the relationship between Stratix GX source-synchronous circuitry and the Stratix GX source-synchronous circuitry with DPA.

Figure 3–5. Source-Synchronous DPA Circuitry

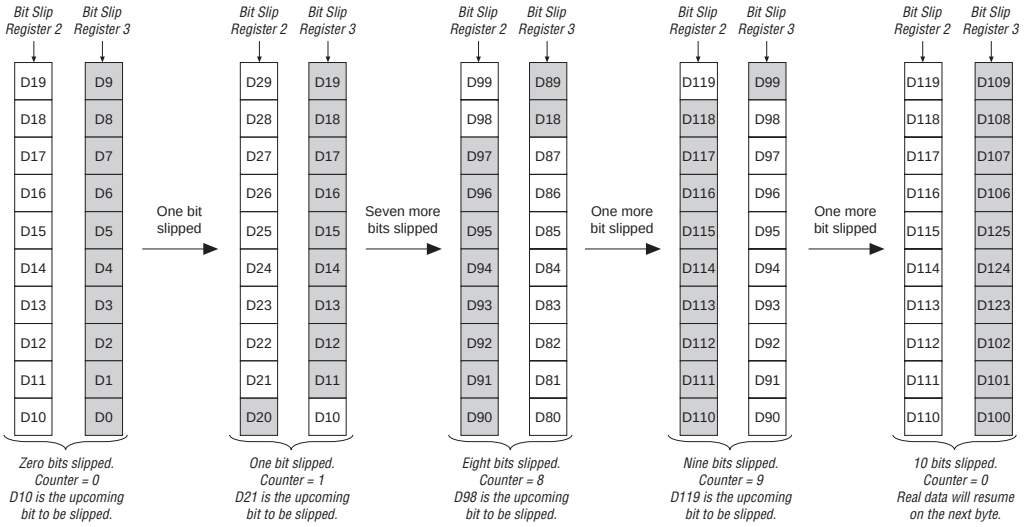


Note to Figure 3–5:

(1) Both deserializers are identical. The deserializer operation is described in the "Principles of SERDES Operation" section.

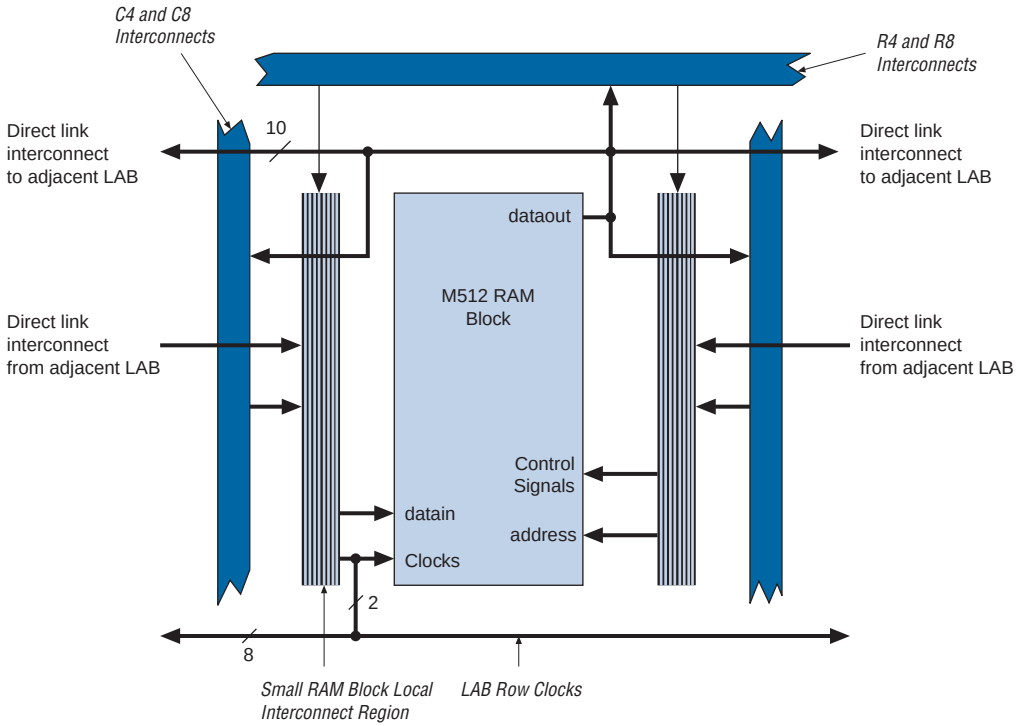
The DPA data-realignment circuitry allows further realignment beyond what the *J* multiplication factor allows. You can set the *J* multiplication factor to be 8 or 10. However, because data must be continuously clocked in on each low-speed clock cycle, the upcoming bit to be realigned and previous *n* –1 bits of data are selected each time the data realignment logic's counter passes *n* –1. At this point the data is selected entirely from bit-slip register 3 (see Figure 3–11) as the counter is reset to 0. The logic array receives a new valid byte of data on the next divided low speed clock cycle. Figure 3–11 shows the data realignment logic output selection from data in the data realignment register 2 and data realignment register 3 based on its current counter value upon continuous request of data slipping from the logic array.

Figure 3–11. DPA Data Realigner



Use the `rx_channel_data_align` signal within the device to activate the data realigner. You can use internal logic or an external pin to control the `rx_channel_data_align` signal. To ensure the rising edge of the `rx_channel_data_align` signal is latched into the control logic, the `rx_channel_data_align` signal should stay high for at least two low-frequency clock cycles.

Figure 4–15. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block implements buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 4–6 summarizes the byte selection.

Table 4–6. Byte Enable for M4K Blocks Notes (1), (2)

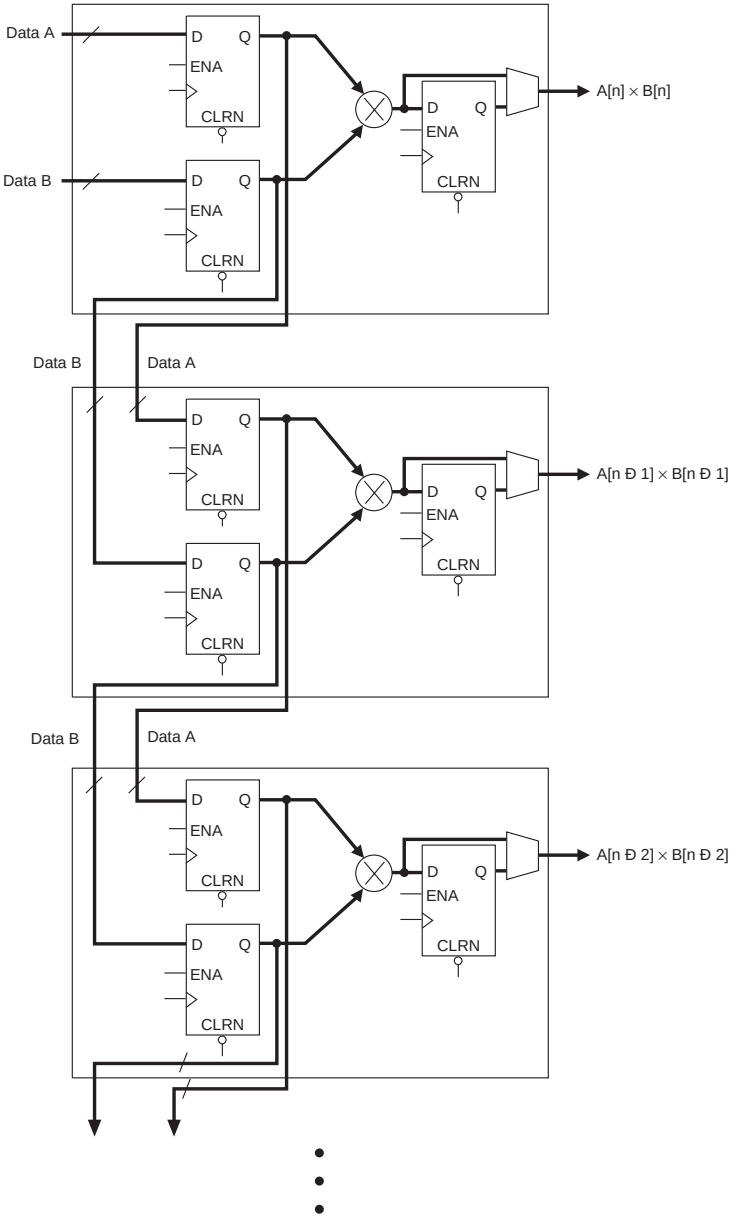
byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 4–6:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, that is, in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 4–16.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 4–17 shows the M4K RAM block to logic array interface.

Figure 4–32. Multiplier Sub-Blocks Using Input Shift Register Connections *Note (1)*



Note to Figure 4–32:
(1) Either Data A or Data B input can be set to a parallel input for constant coefficient multiplication.

These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 40 unique clock domains within EP1SGX10 and EP1SGX25 devices, and 48 unique clock domains within EP1SGX40 devices.

There are 12 dedicated clock pins (CLK[15..12], and CLK[7..0]) to drive either the global or regional clock networks. Three clock pins drive the top, bottom, and left side of the device. Enhanced and fast PLL outputs as well as an I/O interface can also drive these global and regional clock networks.

There are up to 20 recovered clocks (rxclkout[20..0]) and up to 5 transmitter clock outputs (coreclk_out) which can drive any of the global clock networks (CLK[15..0]), as shown in Figure 4–41.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 4–41 shows the 12 dedicated CLK pins and the transceiver clocks driving global clock networks.

Figure 4–43. EP1SGX25 & EP1SGX10 Device Fast Clock Pin Connections to Fast Regional Clocks

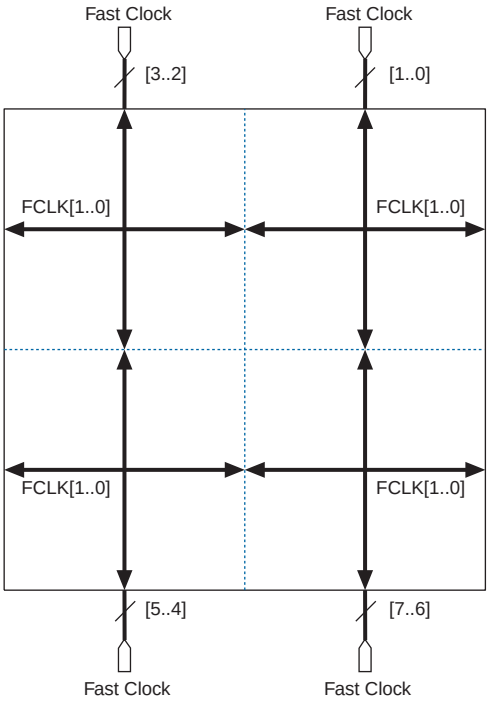
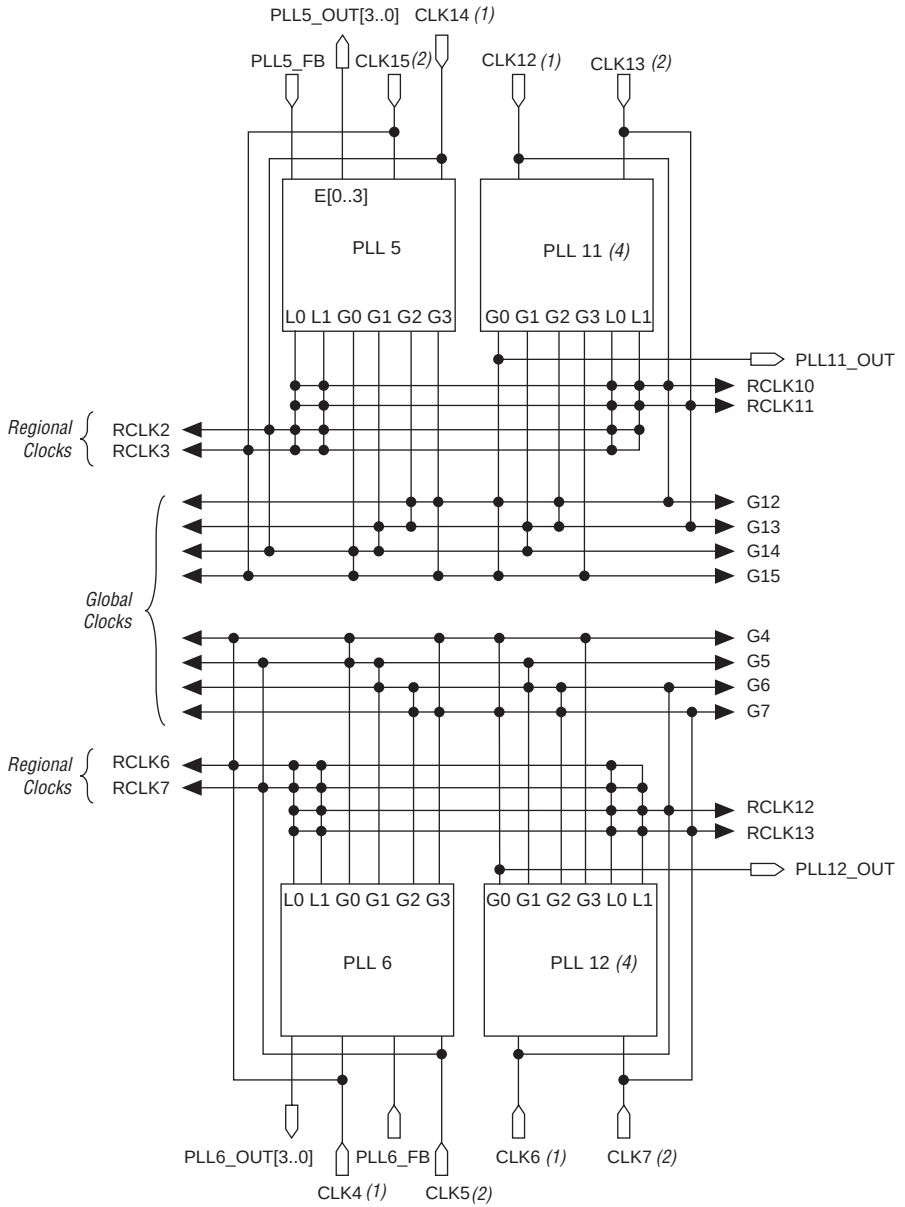


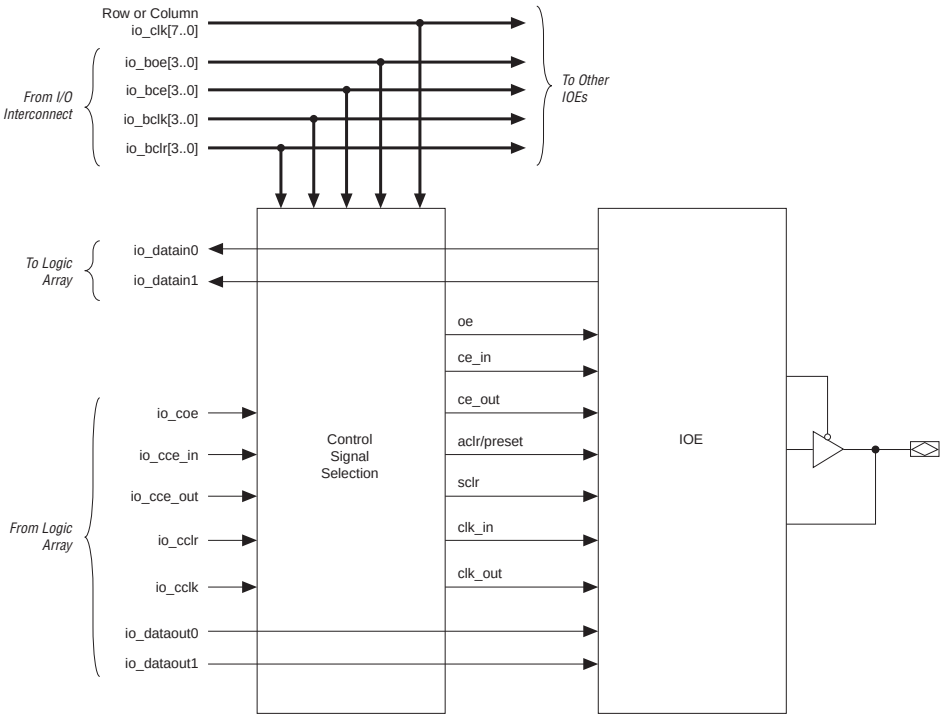
Figure 4–50. Global & Regional Clock Connections From Top Clock Pins & Enhanced PLL Outputs *Note (1)*



Note to Figure 4–50:
(1) PLLs 5, 6, 11, and 12 are enhanced PLLs.

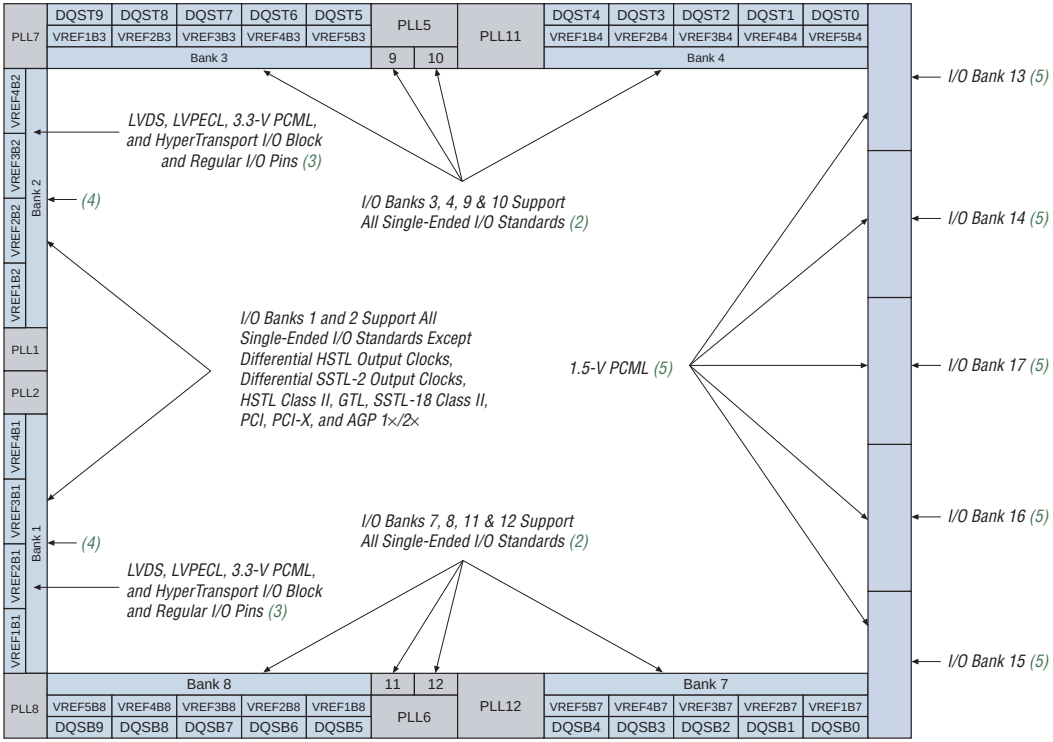
Stratix GX devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 4–68). Figure 4–61 illustrates the signal paths through the I/O block.

Figure 4–61. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 4–62 illustrates the control signal selection.

Figure 4–69. Stratix GX I/O Banks *Notes (1), (2), (3)*



Notes to Figure 4–69:

(1) Figure 4–69 is a top view of the Stratix GX silicon die.

(2) Banks 9 through 12 are enhanced PLL external clock output banks.

(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix GX Device Handbook, Volume 2*.

(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled)

Figure 5–5. Temperature Versus Temperature-Sensing Diode Voltage

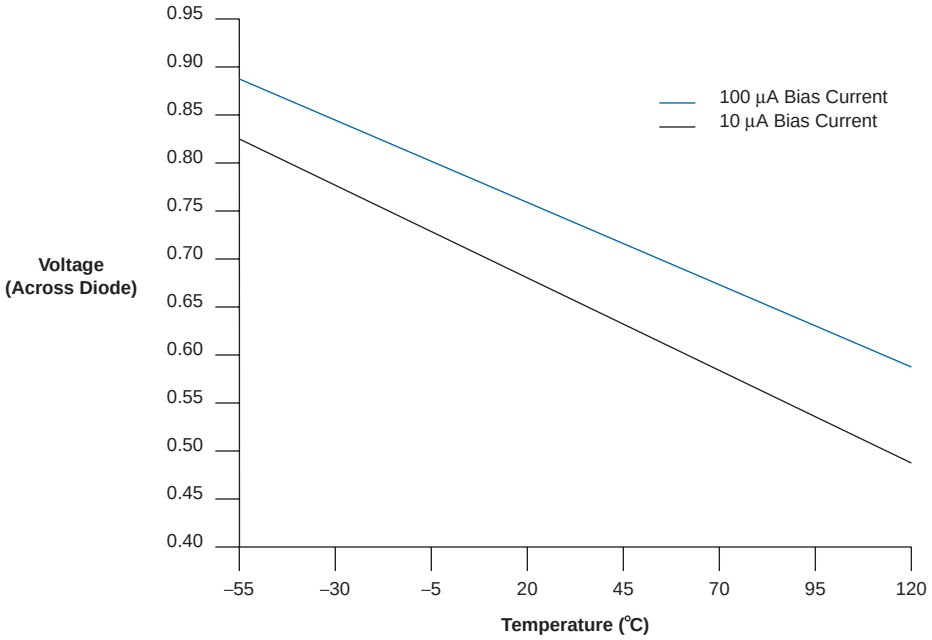


Table 6–48. M4K Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{M4KDATACO1}$		571		635		729	ps
$t_{M4KDATACO2}$		3,984		4,507		5,182	ps
$t_{M4KCLKHL}$	150		167		192		ps
t_{M4KCLR}	170		189		255		ps

Table 6–49. M-RAM Block Internal Timing Microparameters

Symbol	-5		-6		-7		Unit
	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562	ps
t_{MRAMWC}		3,654		4,127		4,746	ps
$t_{MRAMWERESU}$	25		25		28		ps
$t_{MRAMWERH}$	18		20		23		ps
$t_{MRAMDATASU}$	25		25		28		ps
$t_{MRAMDATAH}$	18		20		23		ps
$t_{MRAMWADDRASU}$	25		25		28		ps
$t_{MRAMWADDRH}$	18		20		23		ps
$t_{MRAMRADDRASU}$	25		25		28		ps
$t_{MRAMRADDRH}$	18		20		23		ps
$t_{MRAMDATABSU}$	25		25		28		ps
$t_{MRAMDATABH}$	18		20		23		ps
$t_{MRAMADDRBSU}$	25		25		28		ps
$t_{MRAMADDRBH}$	18		20		23		ps
$t_{MRAMDATACO1}$		1,038		1,053		1,210	ps
$t_{MRAMDATACO2}$		4,362		4,939		5,678	ps
$t_{MRAMCLKHL}$	270		300		345		ps
$t_{MRAMCLR}$	135		150		172		ps

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 6–74. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)

Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
GTL+		–110		–115		–133	ps
3.3-V PCI		–230		–241		–277	ps
3.3-V PCI-X 1.0		–230		–241		–277	ps
Compact PCI		–230		–241		–277	ps
AGP 1×		–30		–31		–36	ps
AGP 2×		–30		–31		–36	ps
CTT		50		53		61	ps
SSTL-3 class I		90		95		109	ps
SSTL-3 class II		–50		–52		–60	ps
SSTL-2 class I		100		105		120	ps
SSTL-2 class II		20		21		24	ps
SSTL-18 class I		230		242		278	ps
SSTL-18 class II		0		0		0	ps
1.5-V HSTL class I		380		399		459	ps
1.5-V HSTL class II		190		200		230	ps
1.8-V HSTL class I		380		399		459	ps
1.8-V HSTL class II		390		410		471	ps

Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		570		599		689	ps
	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	24 mA		0		0		0	ps
3.3-V LVTTL	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	16 mA		70		74		85	ps
	24 mA		0		0		0	ps