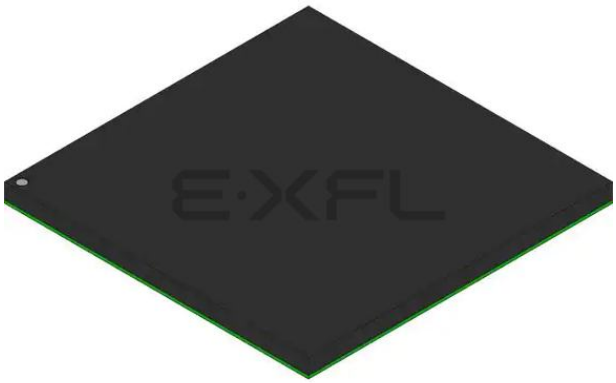
Altera - EP1SGX25CF672C7N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx25cf672c7n

Table 1–2. Stratix GX Package Options & I/O Pin Counts (Part 2 of 2) *Note (1)*

Device	672-Pin FineLine BGA	1,020-Pin FineLine BGA
EP1SGX25D	455	607
EP1SGX25F		607
EP1SGX40D		624
EP1SGX40G		624

Note to Table 1–2:

(1) The number of I/O pins listed for each package includes dedicated clock pins and dedicated fast I/O pins. However, these numbers do not include high-speed or clock reference pins for high-speed I/O standards.

Table 1–3. Stratix GX FineLine BGA Package Sizes

Dimension	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00
Area (mm^2)	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

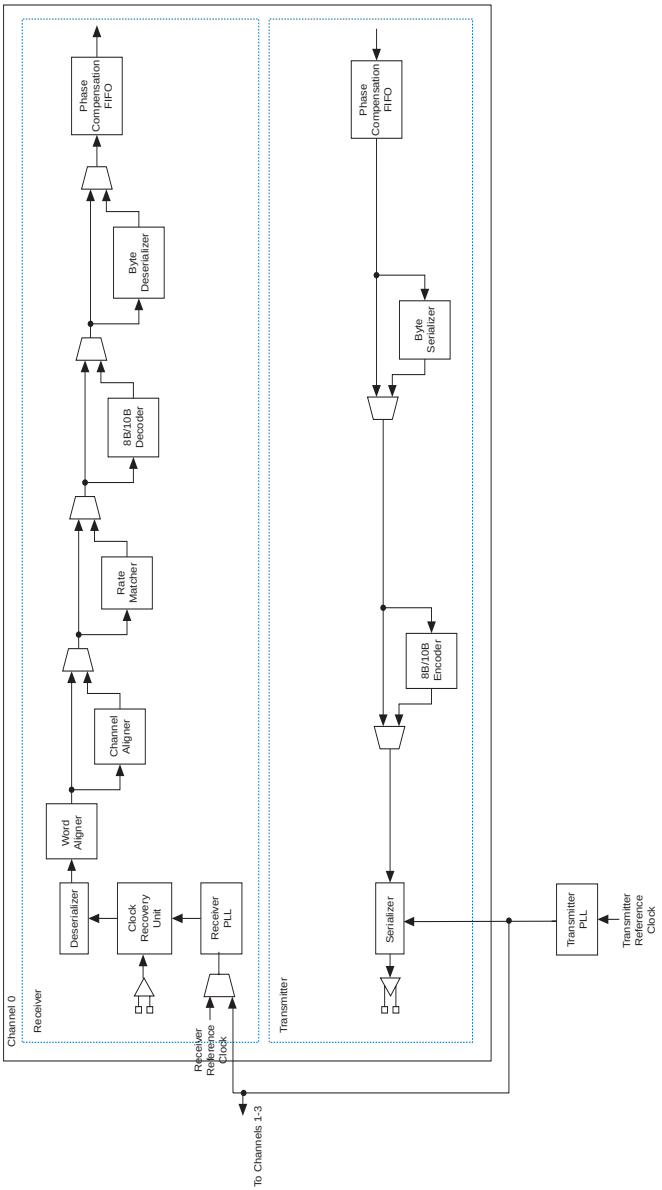
Table 1–4. Stratix GX Device Speed Grades

Device	672-Pin FineLine BGA	1,020-pin FineLine BGA
EP1SGX10	-5, -6, -7	
EP1SGX25	-5, -6, -7	-5, -6, -7
EP1SGX40		-5, -6, -7

High-Speed I/O Interface Functional Description

The Stratix GX device family supports high-speed serial transceiver blocks with CDR circuitry as well as source-synchronous interfaces. The channels on the right side of the device use an embedded circuit dedicated for receiving and transmitting high-speed serial data streams to and from the system board. These channels are clustered in a four-channel serial transceiver building block and deliver high-speed bidirectional point-to-point data transmissions to provide up to 3.1875 Gbps of full-duplex data transmission per channel. The channels on the left side of the device support source-synchronous data transfers at up to 1 Gbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards. Figure 1–1 shows the Stratix GX I/O blocks. The differential source-synchronous serial interface and the high-speed serial interface are described in the *Stratix GX Transceivers* chapter of the *Stratix GX Device Handbook, Volume 1*.

Figure 2–2. Stratix GX Transceiver ChanneL Note (1)

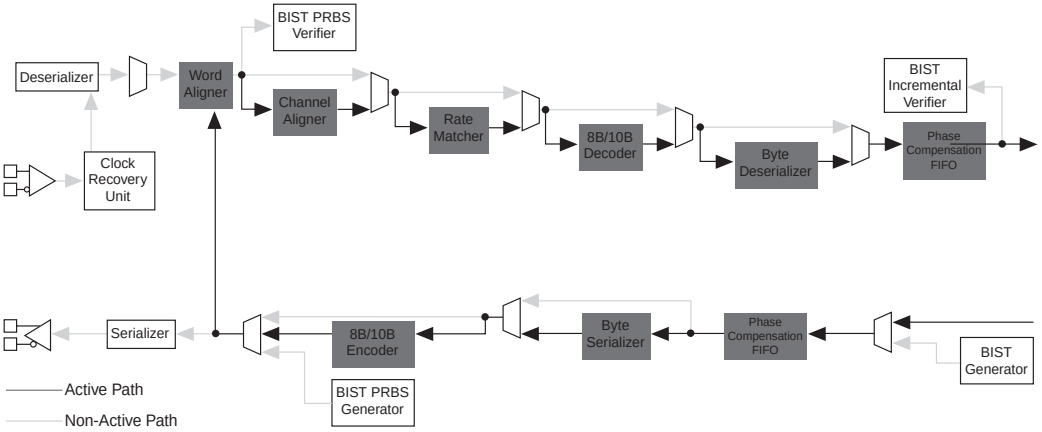


Note to Figure 2–2:
(1) There are four transceiver channels in a transceiver block.

Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not use in the loopback path. The received data is not retimed. Figure 2–22 shows the data path in parallel loopback mode. This option is not dynamically switchable. Reception of an external signal is not possible in this mode.

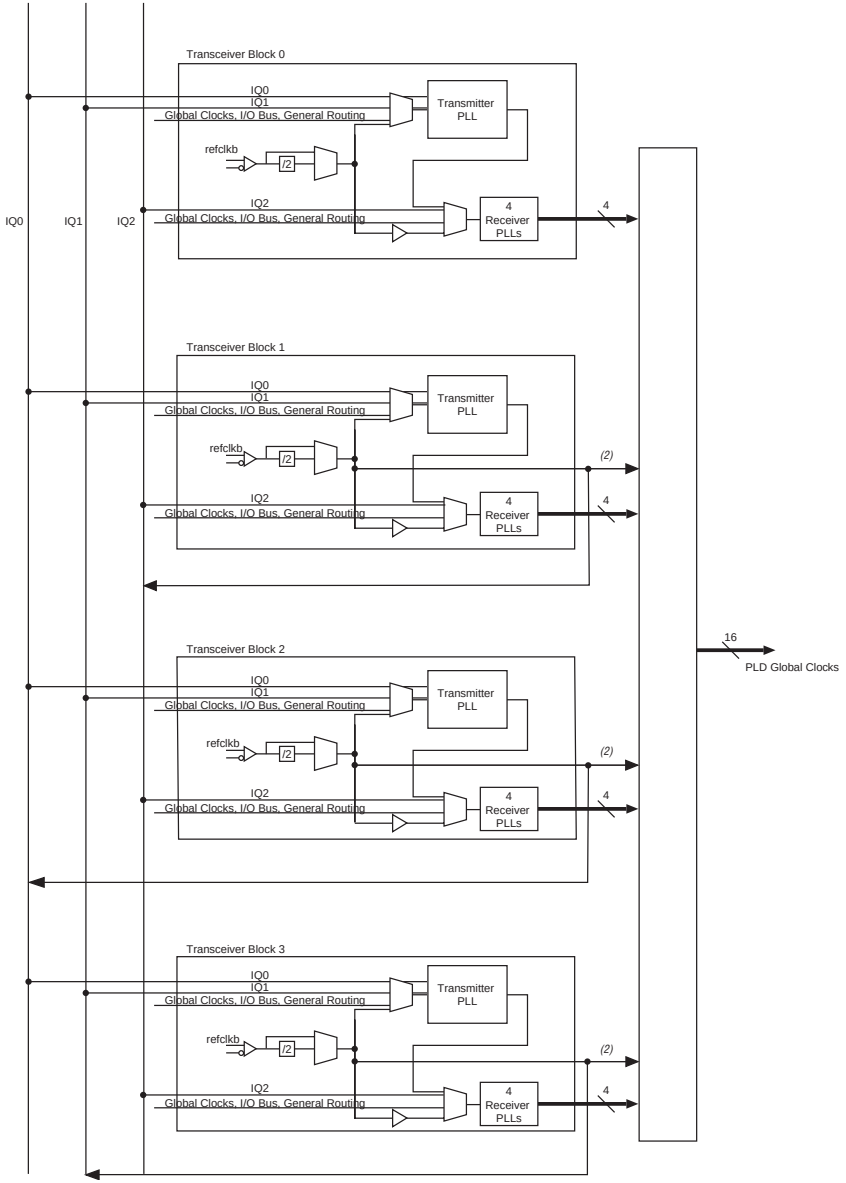
Figure 2–22. Data Path in Parallel Loopback Mode



Reverse Serial Loopback

The reverse serial loopback exercises the analog portion of the transceiver. This loopback mode is dynamically switchable through the `tx_srlpbk` port on a channel by channel basis. Asserting `rxanalogreset` in reverse serial loopback mode powers down the receiver buffer and CRU, preventing data loopback. Figure 2–23 shows the data path in reverse serial loopback mode.

Figure 2–26. EP1SGX25F Device Inter-Transceiver & Global Clock Connections *Note (1)*



Notes to Figure 2–26:

(1) IQ lines are inter-transceiver block lines.

(2) If the /2 pre-divider is used, the path to drive the PLD logic array, local, or global clocks is not allowed.

(3) There are four receiver PLLs in each transceiver block.

Figure 2–31. EP1SGX40 Receiver PLL Recovered Clock to Fast Regional Clock Connection

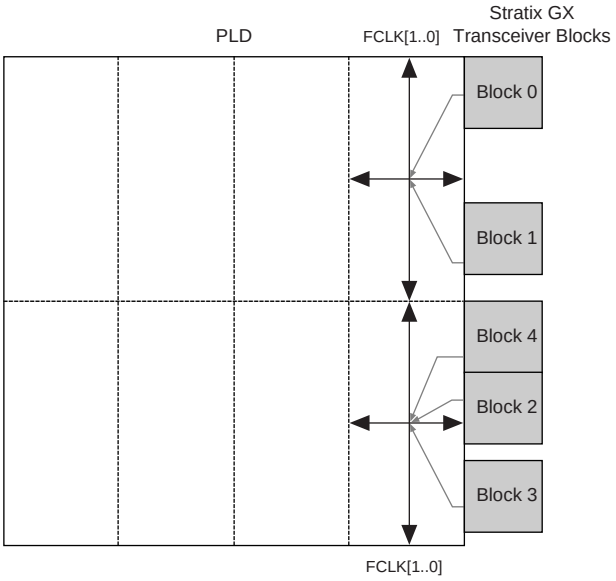


Table 2–10 summarizes the possible clocking connections for the transceivers.

Table 2–10. Possible Clocking Connections for Transceivers (Part 1 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
REFCLKB	✓	✓	✓ *(1)*	✓		✓ *(1)*
Transmitter PLL		✓	✓	✓	✓	
Receiver PLL			✓	✓	✓	
GCLK	✓	✓				
RCLK	✓	✓				
FCLK	✓	✓				

Table 2–10. Possible Clocking Connections for Transceivers (Part 2 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
IQ lines	✓ (2)	✓ (2)				

Notes to Table 2–10:

(1) REFCLKB from transceiver block 0 and transceiver block 4 does not drive the inter-transceiver lines or the GCLK lines.

(2) Inter-transceiver line 0 and inter-transceiver line 1 drive the transmitter PLL, while inter-transceiver line 2 drives the receiver PLLs.

Other Transceiver Features

Other important features of the Stratix GX transceivers are the power down and reset capabilities, the external voltage reference and bias circuitry, and hot swapping.

Individual Power-Down & Reset for the Transmitter & Receiver

Stratix GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed. The device can individually reset the receiver and transmitter blocks and the PLLs. The Stratix GX device can either globally power down and reset the transmitter and receiver channels or do each channel separately. Table 2–11 shows the connectivity between the reset signals and the Stratix GX logical blocks.

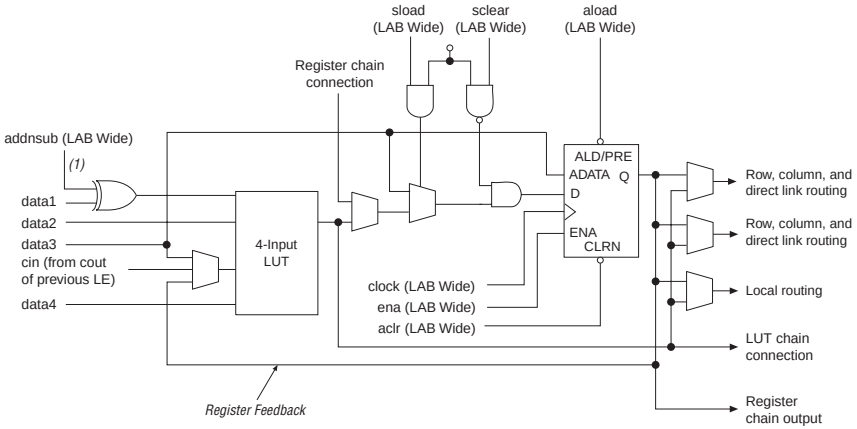
clock enable control for the register. These LAB-wide signals are available in all LE modes. The addnsub control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 4–5). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.

Figure 4–5. LE in Normal Mode



Note to Figure 4–5:
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

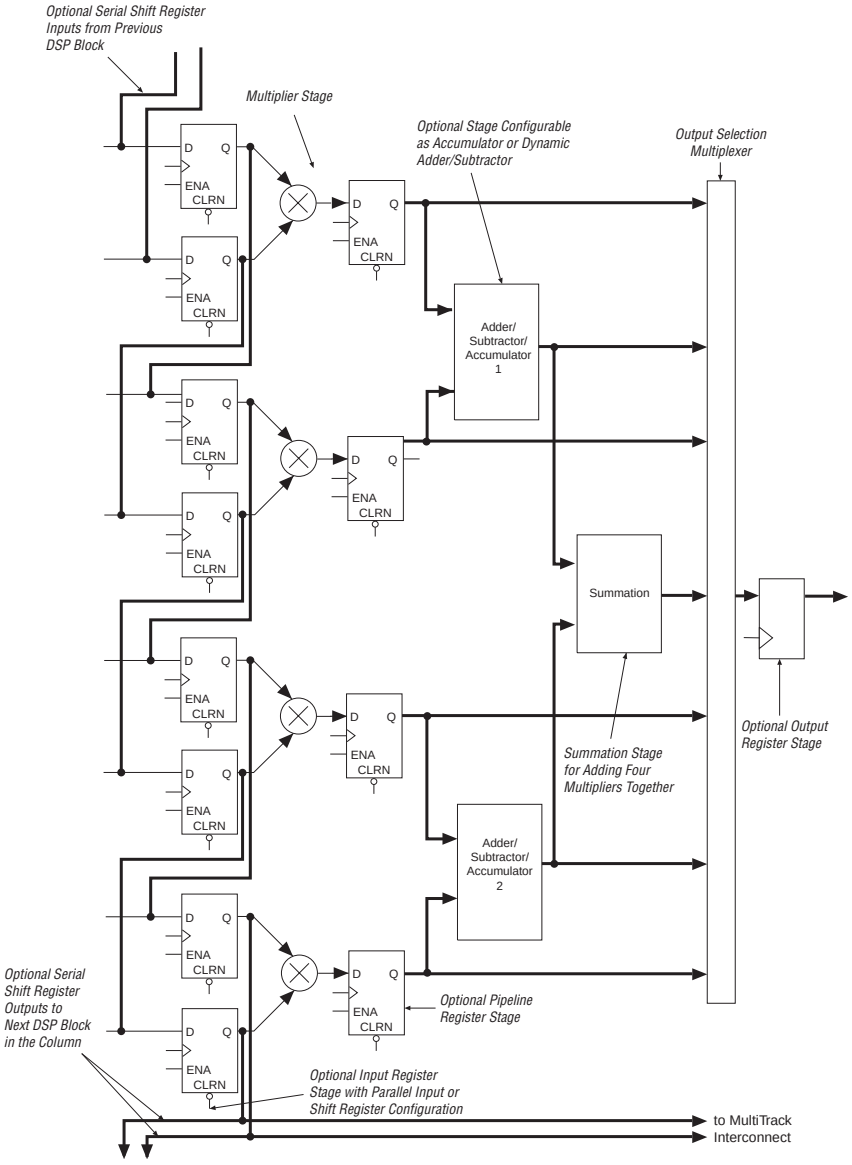
Table 4–8. M-RAM Block Configurations (True Dual-Port)				
Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the WREN signal, which sets the ports into either read or write modes. There is no separate read enable (RE) signal.

Writing into RAM is controlled by both the WREN and byte enable (byteena) signals for each port. The default value for the byteena signal is high, in which case writing is controlled only by the WREN signal. The byte enables are available for the ×18, ×36, and ×72 modes. In the ×144 simple dual-port mode, the two sets of byteena signals (byteena_a and byteena_b) are combined to form the necessary 16 byte enables. Tables 4–9 and 4–10 summarize the byte selection.

Table 4–9. Byte Enable for M-RAM Blocks Notes (1), (2)			
byteena[3..0]	datain ×18	datain ×36	datain ×72
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Figure 4–29. DSP Block Diagram for 18 × 18-Bit Configuration



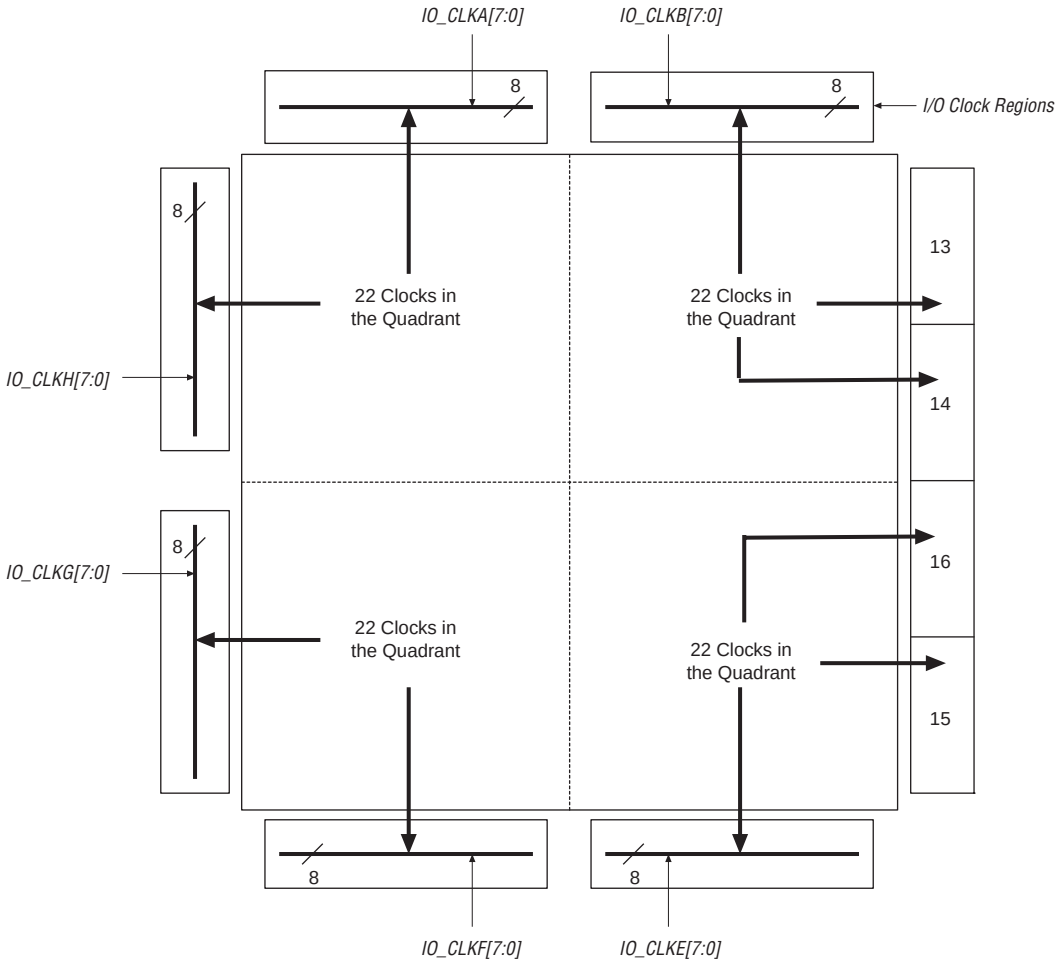
Pipeline/Post Multiply Register

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register pipelines the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. You can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 4–33 shows the adder and output stages.

Figure 4–46. EP1SGX25 & EP1SGX10 Device I/O Clock Groups



Phase Shifting

Stratix GX device fast PLLs have advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 150 to 400 ps. This resolution is a function of the VCO period.

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

For more information on high-speed differential I/O support, see the *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

The IOE in Stratix GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 4–58 shows the Stratix GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Table 4–22 shows the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1SGX10 through EP1SGX40 devices. The DDR SDRAM and QDR SRAM numbers in Table 4–22 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 4–22. External RAM Support in EP1SGX10 Through EP1SGX40 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)		
		-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
DDR SDRAM *(1)*, *(2)*	SSTL-2	200	167	133
DDR SDRAM - side banks *(2)*, *(3)*, *(4)*	SSTL-2	150	133	133
RLDRAM II *(4)*	1.8-V HSTL	200	*(5)*	*(5)*
QDR SRAM *(6)*	1.5-V HSTL	167	167	133
QDRII SRAM *(6)*	1.5-V HSTL	200	167	133
ZBT SRAM *(7)*	LVTTL	200	200	167

Notes to Table 4–22:

(1) These maximum clock rates apply if the Stratix GX device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).
(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*
(3) DDR SDRAM is supported on the Stratix GX device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.
(4) These performance specifications are preliminary.
(5) This device does not support RLDRAM II.
(6) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.
(7) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

In addition to six I/O registers and one input latch in the IOE for interfacing to these high-speed memory interfaces, Stratix GX devices also have dedicated circuitry for interfacing with DDR SDRAM. In every Stratix GX device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR SDRAM up to 200 MHz. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32.

Table 4–28 shows I/O standard support for each I/O bank.

Table 4–28. I/O Support by Bank (Part 1 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓		✓
3.3-V PCI-X 1.0	✓		✓
LVPECL		✓	✓
3.3-V PCML		✓	✓
LVDS		✓	✓
HyperTransport technology		✓	✓
Differential HSTL (clock inputs)	✓	✓	
Differential HSTL (clock outputs)			✓
Differential SSTL (clock outputs)			✓
3.3-V GTL	✓		✓
3.3-V GTL+	✓	✓	✓
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II	✓		✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II	✓		✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II	✓		✓
SSTL-2 class I	✓	✓	✓
SSTL-2 class II	✓	✓	✓
SSTL-3 class I	✓	✓	✓

You can implement the error detection CRC feature with existing circuitry in Stratix GX devices, eliminating the need for external logic. For Stratix GX devices, the CRC is computed by Quartus II and downloaded into the device as a part of the configuration bit stream. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix GX devices to perform error detection automatically. This error detection circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Temperature-Sensing Diode

Stratix GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix GX device and can be used for intelligent power management.

The diode requires two pins (tempdiodep and tempdioden) on the Stratix GX device to connect to the external temperature-sensing device, as shown in Figure 5–4. The temperature-sensing diode is a passive element and therefore can be used before the Stratix GX device is powered.

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 2 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade *(1)*			-6 Commercial & Industrial Speed Grade *(1)*			-7 Commercial & Industrial Speed Grade *(1)*			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Jitter tolerance (peak-to-peak)	Jitter components <20 MHz			20			20			20	ps
	Wideband			50			50			50	ps
Reference input clock frequency	Dedicated `refclkb` pins	25		650	25		650	25		312.5	MHz
	PLD clock resources	25		325	25		325	25		156.25	MHz
Receiver											
Serial data rate (general)	Commercial / industrial	614		3,187.5	614		3,187.5	614		2,500	Mbps
Serial data rate (8B/10B encoded)	Commercial / industrial	500		3,187.5	500		3,187.5	500		2,500	Mbps
Parallel transceiver/ logic array interface speed		20		398.4	20		375	20		312.5	MHz
Rate matching frequency tolerance	XAUI mode only			±100			±100			±100	ppm
8B/10B Custom Receiver Jitter Tolerance using Encoded CJPAT *Note (2)*											
Deterministic jitter	500 Mbps			0.45			0.45			0.45	UI
Total jitter	500 Mbps			0.71			0.71			0.71	UI
Fibre Channel Receiver Jitter Tolerance using 8B/10B Encoded CJTPAT *Note (2)*											
Deterministic jitter	1.0625 Gbps			0.37			0.37			0.37	UI
Total jitter	1.0625 Gbps			0.68			0.68			0.68	UI

Table 6–14. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300		600	mV
V_{ICM}	Input common mode voltage		1.5		3.465	V
V_{OD}	Output differential voltage (single-ended)		300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low				50	mV
V_{OCM}	Output common mode voltage		2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low				50	mV
V_T	Output termination voltage			V_{CCIO}		V
R_1	Output external pull-up resistors		45	50	55	Ω
R_2	Output external pull-up resistors		45	50	55	Ω

Table 6–15. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300		1,000	mV
V_{ICM}	Input common mode voltage		1		2	V
V_{OD}	Differential output voltage (single ended)	R_L = 100 Ω	525	700	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.5	1.7	1.9	V
R_L	Receiver differential input resistor, external		90	100	110	Ω

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 6–84. Stratix GX Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.8 V	250	250	250	MHz
1.5 V	225	200	200	MHz
LVCMOS	350	300	250	MHz
GTL	200	167	125	MHz
GTL+	200	167	125	MHz
SSTL-3 class I	167	150	133	MHz
SSTL-3 class II	167	150	133	MHz
SSTL-2 class I	200	200	167	MHz
SSTL-2 class II	200	200	167	MHz
SSTL-18 class I	150	133	133	MHz
SSTL-18 class II	150	133	133	MHz
1.5-V HSTL class I	250	225	200	MHz
1.5-V HSTL class II	225	200	200	MHz
1.8-V HSTL class I	250	225	200	MHz
1.8-V HSTL class II	225	200	200	MHz
3.3-V PCI	350	300	250	MHz
3.3-V PCI-X 1.0	350	300	250	MHz
Compact PCI	350	300	250	MHz
AGP 1×	350	300	250	MHz
AGP 2×	350	300	250	MHz
CTT	200	200	200	MHz
Differential HSTL	225	200	200	MHz
Differential SSTL-2	200	200	167	MHz
LVDS	500	500	500	MHz
LVPECL	500	500	500	MHz
PCML	350	350	350	MHz
HyperTransport technology	350	350	350	MHz

Table 6–85. Stratix GX Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2] Pins (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	400	350	300	MHz
2.5 V	400	350	300	MHz
1.8 V	400	350	300	MHz

Table 6–90. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		420	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		434	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* *(10)*	*(8)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration *(10)*	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		600 *(7)*	MHz