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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx25cf672i6

Transmitter Path

This section describes the data path through the Stratix GX transmitter (see [Figure 2–2](#)). Data travels through the Stratix GX transmitter via the following modules:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

Transmitter PLL

Each transceiver block has one transmitter PLL, which receives the reference clock and generates the following signals:

- High-speed serial clock used by the serializer
- Slow-speed reference clock used by the receiver
- Slow-speed clock used by the logic array (divisible by two for double-width mode)

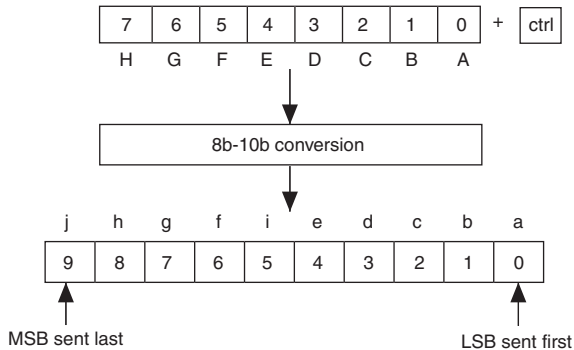
The INCLK clock is the input into the transmitter PLL. There is one INCLK clock per transceiver block. This clock can be fed by either the REFCLKB pin, PLD routing, or the inter-transceiver routing line. See the section [“Stratix GX Clocking”](#) on page 2–30 for more information about the inter-transceiver lines.

The transmitter PLL in each transceiver block clocks the circuits in the transmit path. The transmitter PLL is also used to train the receiver PLL. If no transmit channels are used in the transceiver block, the transmitter PLL can be turned off. [Figure 2–3](#) is a block diagram of the transmitter PLL.

8B/10B Encoder

The 8B/10B encoder translates 8-bit wide data + 1 control enable bit into a 10-bit encoded data. The encoded data has a maximum run length of 5. The 8B/10B encoder can be bypassed. Figure 2-4 diagrams the encoding process.

Figure 2-4. Encoding Process



Transmit State Machine

The transmit state machine operates in either XAUI mode or in GIGE mode, depending on the protocol used.

GIGE Mode

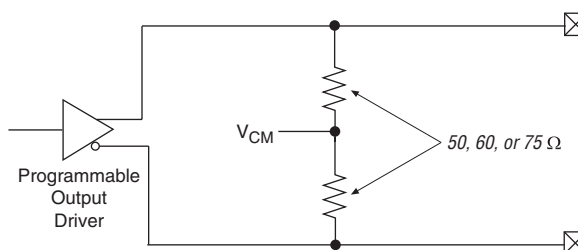
In GIGE mode, the transmit state machines convert all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by (/K28.5/, /D21.5/) and (/K28.5/, /D2.2/), respectively.) Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set. The GIGE transmit state machine can be statically disabled in the Quartus II software, even if using the GIGE protocol mode.

Pre-emphasis percentage is defined as $V_{PP}/V_S - 1$, where V_{PP} is the differential emphasized voltage (peak-to-peak) and V_S is the differential steady-state voltage (peak-to-peak).

Programmable Transmitter Termination

The programmable termination can be statically set in the Quartus II software. The values are 100 Ω , 120 Ω , 150 Ω and off. Figure 2–9 shows the setup for programmable termination.

Figure 2–9. Programmable Transmitter Termination



Receiver Path

This section describes the data path through the Stratix GX receiver (refer to Figure 2–2 on page 2–4). Data travels through the Stratix GX receiver via the following modules:

- Input buffer
- Clock Recovery Unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

Receiver Input Buffer

The Stratix GX receiver input buffer supports the 1.5-V PCML I/O standard at a rate up to 3.1875 Gbps. Additional I/O standards, LVDS, 3.3-V PCML, and LVPECL can be supported when AC coupled. The common mode of the input buffer is 1.1 V. The receiver can support Stratix GX-to-Stratix GX DC coupling.

Table 2–5. Receiver PLL & CRU Adjustable Parameters (Part 2 of 2)

Multiplication factor (W)	2, 4, 5, 8, 10, 16, or 20 (1)
PPM detector	125, 250, 500, 1,000
Bandwidth	Low, medium, high
Run length detector	10-bit or 20-bit mode: 5 to 160 in steps of 5
	8-bit or 16-bit mode: 4 to 128 in steps of 4

Note to Table 2–5:

- (1) Multiplication factors 2, 4, and 5 can only be achieved with the use of the pre-divider on the REFCLKB port or if the CRU is trained with the low speed clock from the transmitter PLL.

The CRU has a built-in switchover circuit to select whether the voltage-controlled oscillator of the PLL is trained by the reference clock or the data. The optional port `rx_freqlocked` monitors when the CRU is in locked to data mode.

In the automatic mode, the following conditions must be met for the CRU to switch from locked to reference to locked to data mode:

- The CRU PLL is within the prescribed PPM frequency threshold setting (125 PPM, 250 PPM, 500 PPM, 1,000 PPM) of the CRU reference clock.
- The reference clock and CRU PLL output are phase matched (phases are within .08 UI).

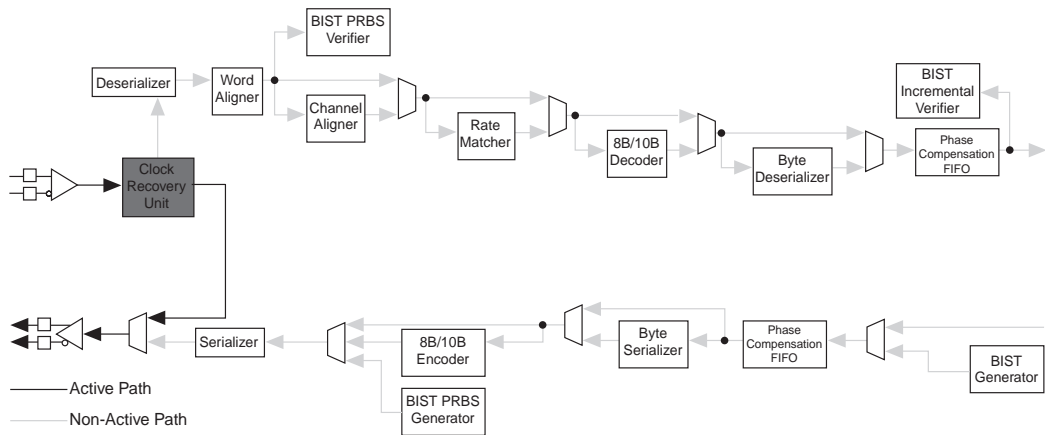
The automatic switchover circuit can be overridden by using the optional ports `rx_lockedtorefclk` and `rx_locktodata`. Table 2–6 shows the possible combinations of these two signals.

Table 2–6. Possible Combinations of `rx_lockedtorefclk` & `rx_locktodata`

<code>rx_locktodata</code>	<code>rx_lockedtorefclk</code>	VCO (lock to mode)
0	0	Auto
0	1	Reference CLK
1	x	DATA

If the `rx_lockedtorefclk` and `rx_locktodata` ports are not used, the default is auto mode.

Figure 2–23. Data Path in Reverse Serial Loopback Mode



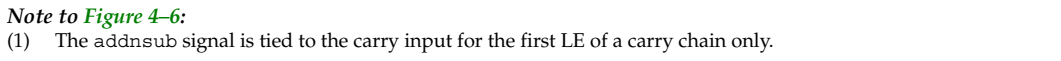
BIST (Built-In Self Test)

The Stratix GX transceiver has built-in self test modes to aid in debug and testing. The BIST modes are set in the Stratix GX MegaWizard Plug-In Manager in the Quartus II software. Only one BIST mode can be set for any single instance of the transceiver block. The BIST mode applies to all channels used in a transceiver.

The following is a list of the available BIST modes:

- PRBS generator and verifier
- Incremental mode generator and verifier
- High-frequency generator
- Low-frequency generator
- Mixed-frequency generator

Figures 2–24 and 2–25 are diagrams of the BIST PRBS data path and the BIST incremental data path, respectively.



The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

Figure 4-7 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used

Table 4–11 shows the input and output data signal connections for the column units (B1 to B6 and A1 to A6). It also shows the address and control signal input connections to the row units (R1 to R11).

Table 4–11. M-RAM Row & Column Interface Unit Signals		
Unit Interface Block	Input Signals	Output Signals
R1	addressa[7..0]	
R2	addressa[15..8]	
R3	byte_enable_a[7..0] renwe_a	
R4	-	
R5	-	
R6	clock_a clocken_a clock_b clocken_b	
R7	-	
R8	-	
R9	byte_enable_b[7..0] renwe_b	
R10	addressb[15..8]	
R11	addressb[7..0]	
B1	datain_b[71..60]	dataout_b[71..60]
B2	datain_b[59..48]	dataout_b[59..48]
B3	datain_b[47..36]	dataout_b[47..36]
B4	datain_b[35..24]	dataout_b[35..24]
B5	datain_b[23..12]	dataout_b[23..12]
B6	datain_b[11..0]	dataout_b[11..0]
A1	datain_a[71..60]	dataout_a[71..60]
A2	datain_a[59..48]	dataout_a[59..48]
A3	datain_a[47..36]	dataout_a[47..36]
A4	datain_a[35..24]	dataout_a[35..24]
A5	datain_a[23..12]	dataout_a[23..12]
A6	datain_a[11..0]	dataout_a[11..0]

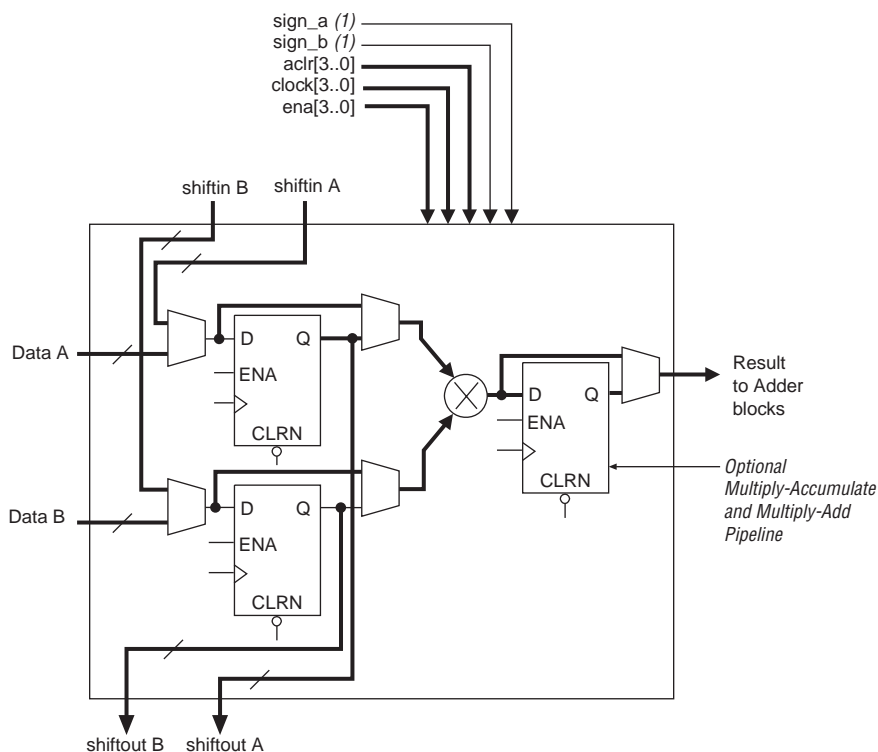
The DSP block consists of the following elements:

- Multiplier block
- Adder/output block

Multiplier Block

The DSP block multiplier block consists of the input registers, a multiplier, and pipeline register for pipelining multiply-accumulate and multiply-add/subtract functions as shown in Figure 4–31.

Figure 4–31. Multiplier Sub-Block Within Stratix GX DSP Block



Note to Figure 4–31:

- (1) These signals can be unregistered or registered once to match data path pipelines if required.

Input Registers

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. You can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. You select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

You can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in [Figure 4-32](#), to form a shift register chain. This chain can terminate in any block, that is, you can create any length of shift register chain up to 224 registers. You can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9×9 - and 18×18 -bit multipliers, you do not need to implement external shift registers in LAB LEs. You implement all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36×36 -bit multipliers.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock [3..0]`, `aclr [3..0]`, and `ena [3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

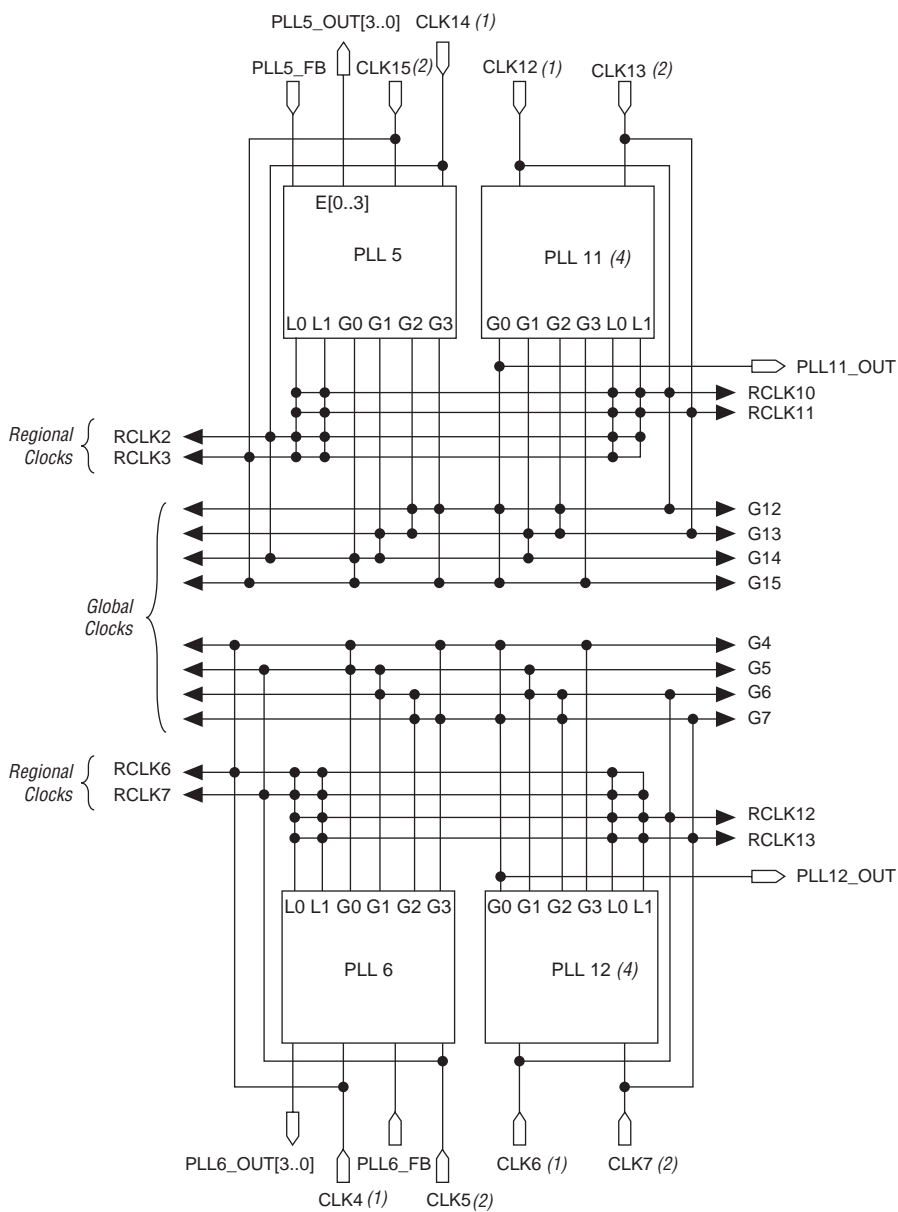
- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder



Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18×18 -bit multipliers or eight 9×9 -bit multipliers can drive their results directly out of one DSP block. See [Figure 4–34](#).

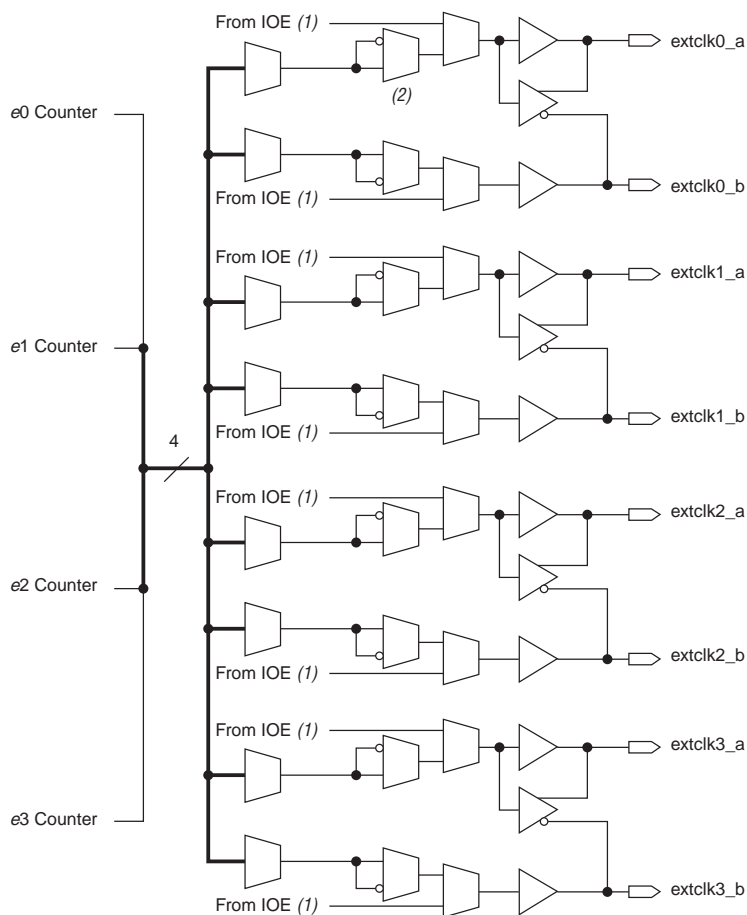
Figure 4–50. Global & Regional Clock Connections From Top Clock Pins & Enhanced PLL Outputs *Note (1)***Note to Figure 4–50:**

(1) PLLs 5, 6, 11, and 12 are enhanced PLLs.

External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See [Figure 4–54](#).

Figure 4–54. External Clock Outputs for PLLs 5 & 6



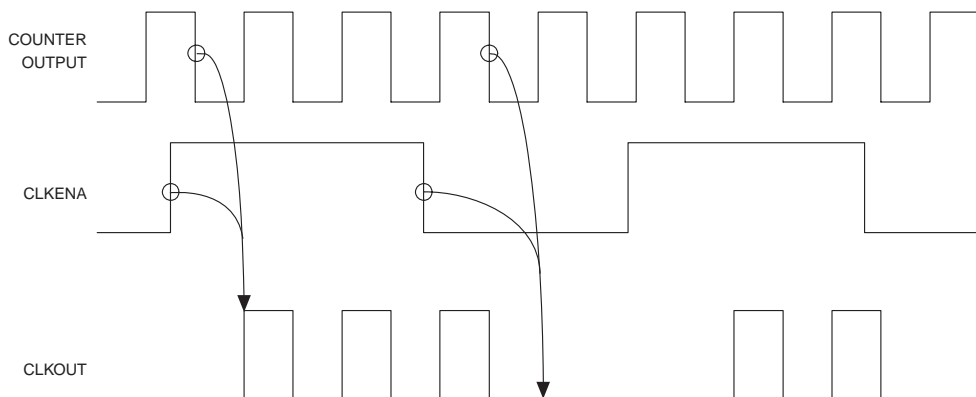
Notes to [Figure 4–54](#):

- (1) Each external clock output pin can be used as a general purpose output pin from the logic array. These pins are multiplexed with IOE outputs.
- (2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each

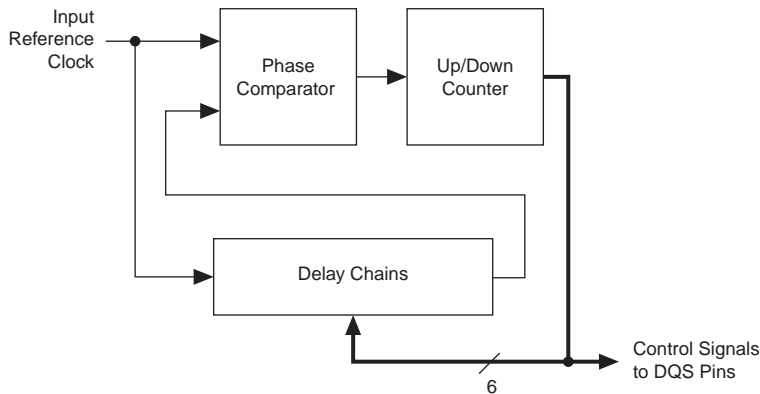
unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

Figure 4–56. extclkena Signals



Fast PLLs

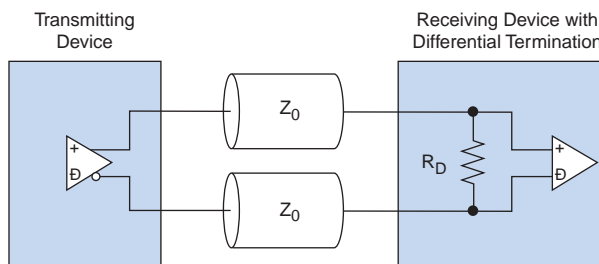
Stratix GX devices contain up to four fast PLLs with high-speed serial interfacing ability, along with general-purpose features. [Figure 4–57](#) shows a diagram of the fast PLL.

Figure 4–68. Simplified Diagram of the DQS Phase-Shift Circuitry

See the *External Memory Interfaces* chapter of the *Stratix GX Device Handbook, Volume 2* for more information on external memory interfaces.

Programmable Drive Strength

The output buffer for each Stratix GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Figure 4–70. LVDS Input Differential On-Chip Termination

I/O banks on the left and right side of the device support LVDS receiver (far-end) differential termination.

Table 4–29 shows the Stratix GX device differential termination support.

Table 4–29. Differential Termination Supported by I/O Banks

Differential Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)
Differential termination (1), (2)	LVDS		✓

Notes to Table 4–29:

- (1) Clock pin CLK0, CLK2, CLK9, CLK11, and pins FPLL [7..10] CLK do not support differential termination.
- (2) Differential termination is only supported for LVDS because of a 3.3-V V_{CCIO} .

Table 4–30 shows the termination support for different pin types.

Table 4–30. Differential Termination Support Across Pin Types

Pin Type	R_D
Top and bottom I/O banks (3, 4, 7, and 8)	
DIFFIO_RX []	✓
CLK [0, 2, 9, 11], CLK [4–7], CLK [12–15]	
CLK [1, 3, 8, 10]	✓
FCLK	
FPLL [7..10] CLK	

The differential on-chip resistance at the receiver input buffer is $118 \Omega \pm 20\%$.

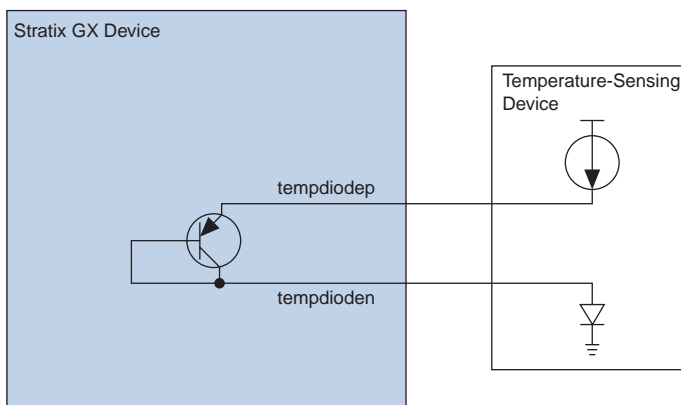
Figure 5–4. External Temperature-Sensing Diode

Table 5–2 shows the specifications for bias voltage and current of the Stratix GX temperature-sensing diode.

Table 5–2. Temperature-Sensing Diode Electrical Characteristics				
Parameter	Minimum	Typical	Maximum	Units
$I_{\text{BIAS high}}$	80	100	120	μA
$I_{\text{BIAS low}}$	8	10	12	μA
$V_{\text{BP}} - V_{\text{BN}}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	W

The temperature-sensing diode works for the entire operating range shown in Figure 5–5.

Table 6–23. SSTL-2 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	$I_{OH} = -8.1 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8.1 \text{ mA}$ (1)			$V_{TT} - 0.57$	V

Table 6–24. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -16.4 \text{ mA}$ (1)	$V_{TT} + 0.76$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16.4 \text{ mA}$ (1)			$V_{TT} - 0.76$	V

Table 6–25. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (1)	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (1)			$V_{TT} - 0.6$	V

Table 6–26. SSTL-3 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters <i>Notes (1), (2)</i>		
Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	$C_{\text{LOAD}} = 10 \text{ pF}$
t_{INSUPLL}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{OUTCOPLL}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	$C_{\text{LOAD}} = 10 \text{ pF}$

Notes to Table 6–52:

- (1) These timing parameters are sample-tested only.
- (2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) <i>Notes (1), (2)</i>		
Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	$C_{\text{LOAD}} = 10 \text{ pF}$
t_{INSUPLL}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Software

Stratix® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes hardware description language and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® logic analysis, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v6.2 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Stratix GX devices will be released on the Altera web site (www.altera.com).

Ordering Information

Figure 7-1 describes the ordering codes for Stratix GX devices.

Figure 7-1. Stratix GX Device Packaging Ordering Information

