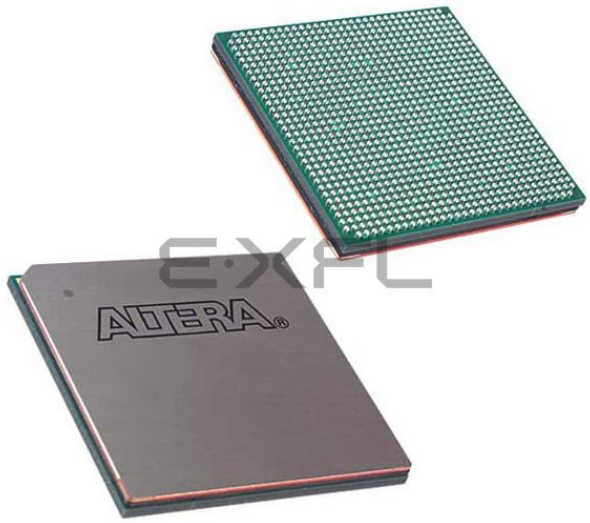

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

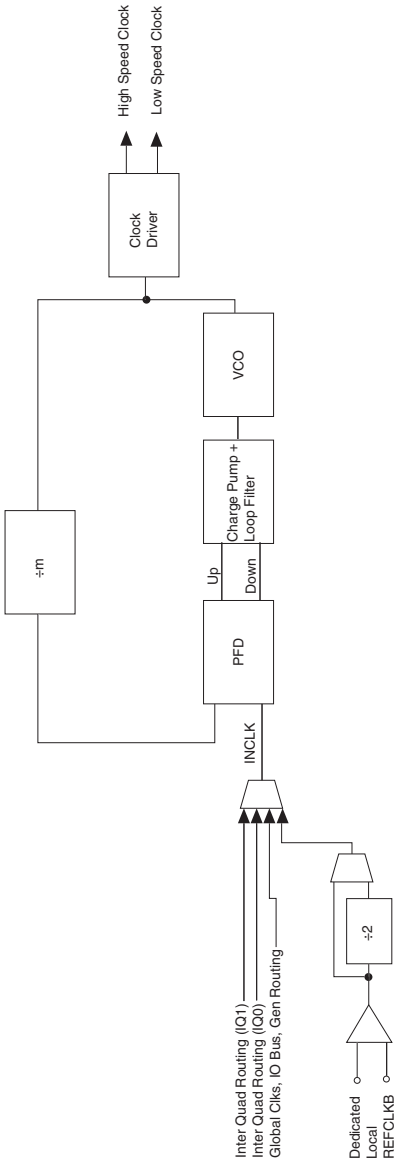
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	607
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx25df1020c5n

Figure 2–3. Transmitter PLL Block Diagram *Note (1)*



Note to Figure 2–3:
(1) The divider in the PLL divides by 4, 8, 10, 16, or 20.

Figure 2–24. BIST PRBS Data Path

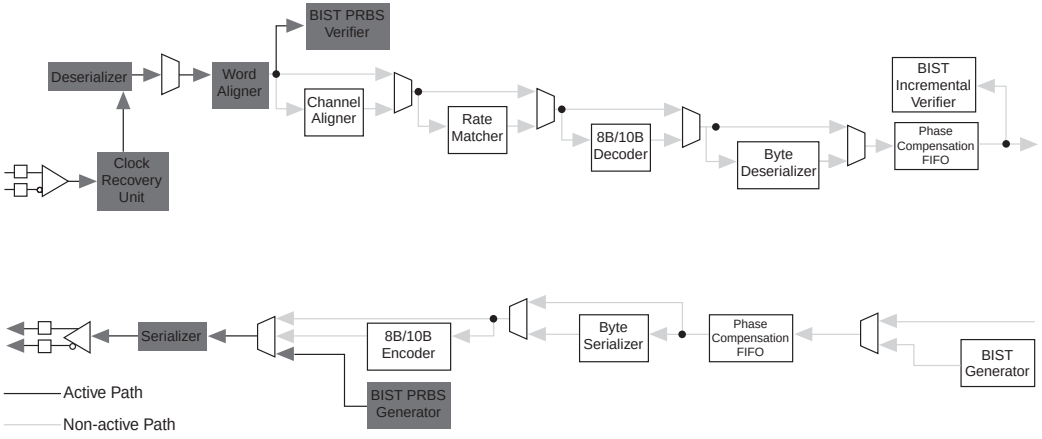


Figure 2–25. BIST Incremental Data Path

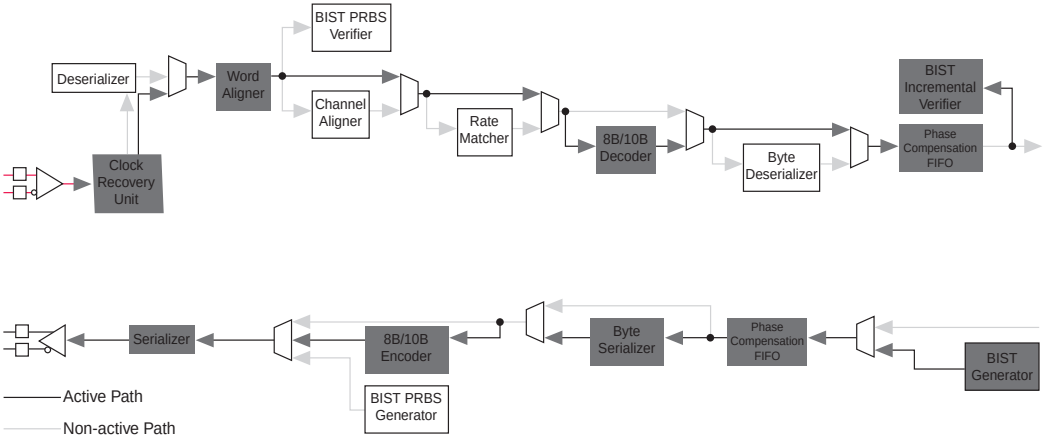


Table 2–9 shows the BIST data output and verifier alignment pattern.

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 1 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 8-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 10-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 2 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 16-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 20-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111
Incremental 10-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
Incremental 20-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
High frequency	1010101010		
Low frequency	0011111000		
Mixed frequency	0011111010 or 1100000101		

Note to Table 2–9:
(1) This output repeats.

Stratix GX Clocking

The Stratix GX global clock can be driven by certain REFCLKB pins, all transmitter PLL outputs, and all receiver PLL outputs. The REFCLKB pins (except for transceiver block 0 and transceiver block 4) can drive inter-transceiver and global clock lines as well as feed the transmitter and receiver PLLs. The output of the transmitter PLL can only feed global clock lines and the reference clock port of the receiver PLL.

Figures 2–26 and 2–27 are diagrams of the Inter-Transceiver line connections as well as the global clock connections for the EP1SGX25F and EP1SGX40G devices. For devices with fewer transceivers, ignore the information about the unavailable transceiver blocks.

multiplication value. The ×1 and ×2 operation is also possible by bypassing the SERDES. The SERDES DPA cannot support ×1, ×2, or ×4 natively.

On the receiver side, the high-frequency clock generated by the PLL shifts the serial data through a shift register (also called deserializer). The parallel data is clocked out to the logic array synchronized with the low-frequency clock. On the transmitter side, the parallel data from the logic array is first clocked into a parallel-in, serial-out shift register synchronized with the low-frequency clock and then transmitted out by the output buffers.

There are two dedicated fast PLLs each in EP1SGX10 to EP1SGX25 devices, and four in EP1SGX40 devices. These PLLs are used for the SERDES operations as well as general-purpose use.

Stratix GX Differential I/O Receiver Operation (Non-DPA Mode)

You can configure any of the Stratix GX source synchronous differential input channels as a receiver channel (see Figure 3–1). The differential receiver deserializes the incoming high-speed data. The input shift register continuously clocks the incoming data on the negative transition of the high-frequency clock generated by the PLL clock (×*W*).

The data in the serial shift register is shifted into a parallel register by the RXLOADEN signal generated by the fast PLL counter circuitry on the third falling edge of the high-frequency clock. However, you can select which falling edge of the high frequency clock loads the data into the parallel register, using the data-realignment circuit.

In normal mode, the enable signal RXLOADEN loads the parallel data into the next parallel register on the second rising edge of the low-frequency clock. You can also load data to the parallel register through the TXLOADEN signal when using the data-realignment circuit.

Figure 3–1 shows the block diagram of a single SERDES receiver channel. Figure 3–2 shows the timing relationship between the data and clocks in Stratix GX devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

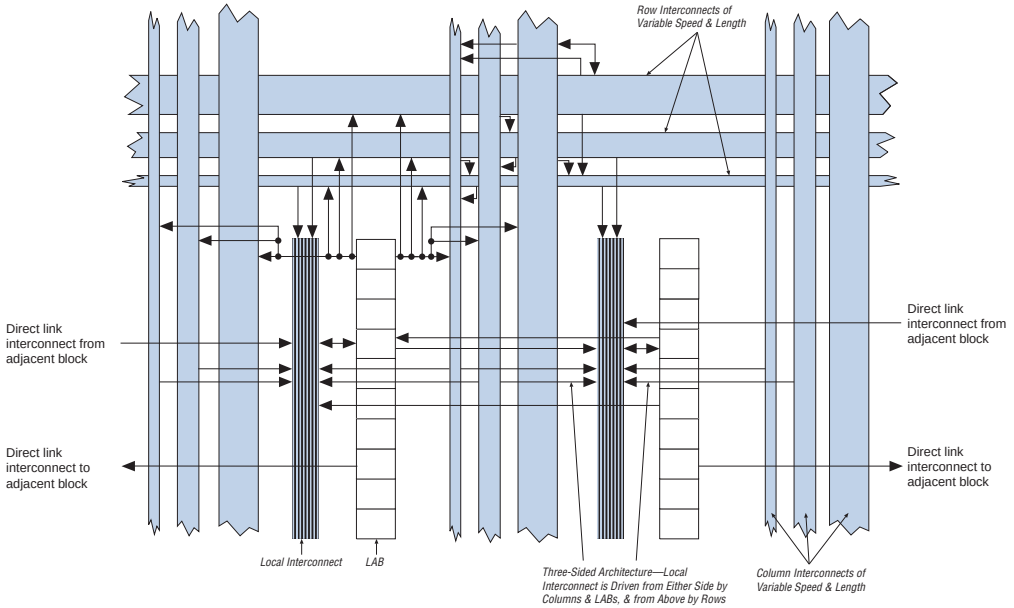
4. Stratix GX Architecture

SGX51004-1.0

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 4–1 shows the Stratix® GX LAB.

Figure 4–1. Stratix GX LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks,

Figure 4–21. M-RAM Row Unit Interface to Interconnect

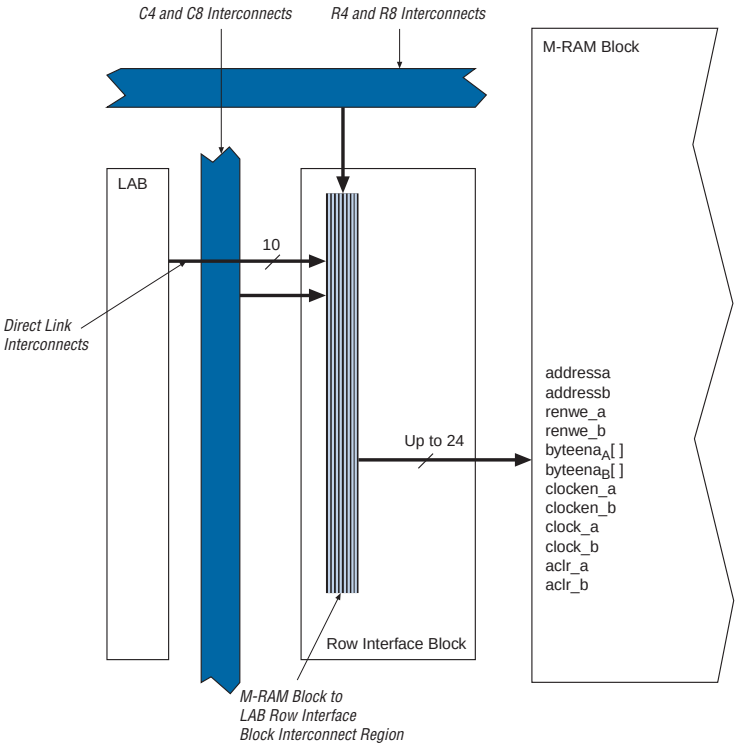
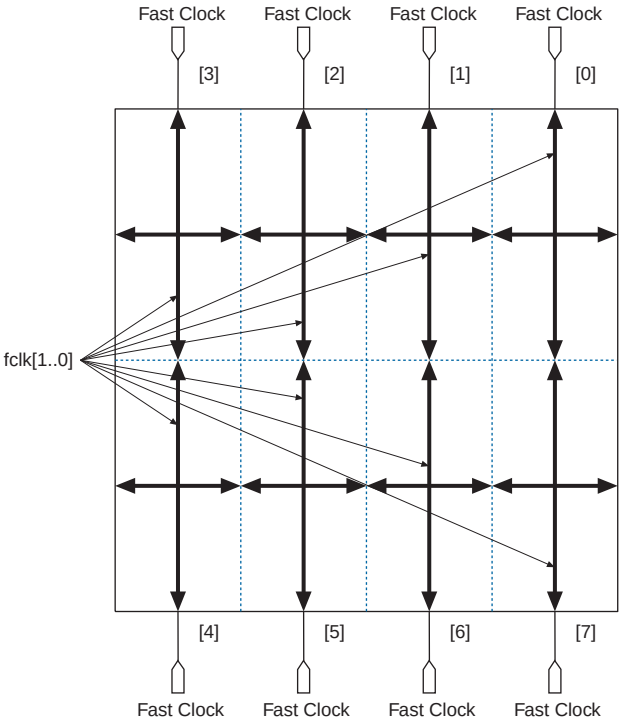


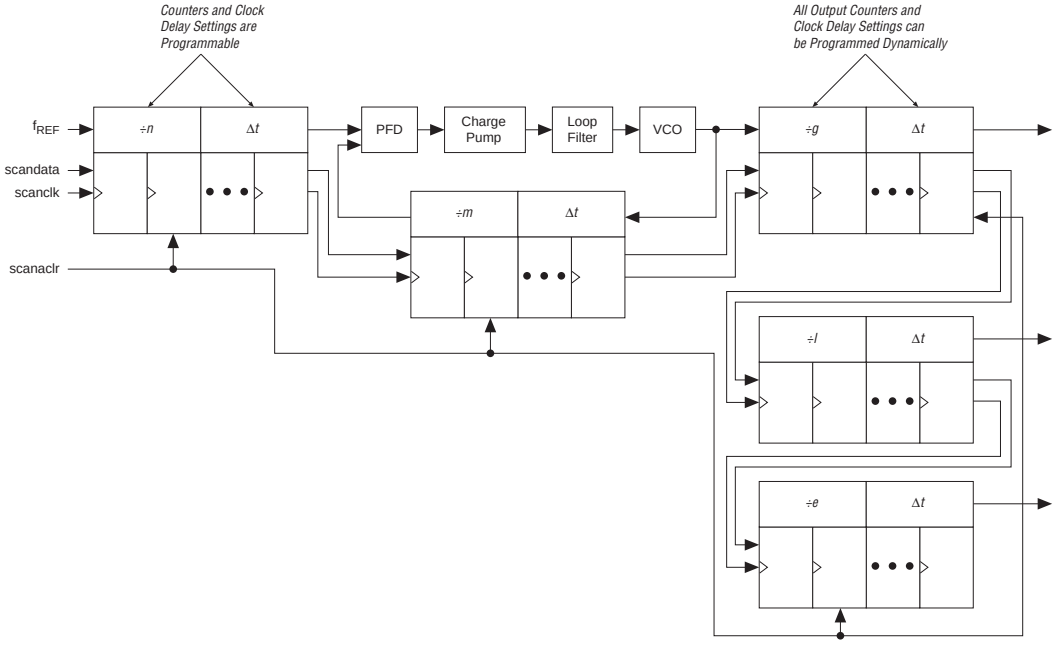
Figure 4–44. EP1SGX40 Device Fast Regional Clock Pin Connections to Fast Regional Clocks



Combined Resources

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, 4 regional clock lines, and 2 fast regional clock lines. Multiplexers are used with these clocks to form 8-bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer at the LAB level selects two of the eight row clocks to feed the LE registers within the LAB. See Figure 4–45.

Figure 4–53. Dynamically Programmable Counters & Delays in Stratix GX Device Enhanced PLLs



PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.

Programmable Bandwidth

You have advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also allows a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL takes longer to lock, but it attenuates all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and *m* counter value. You can manually adjust these values if desired. Bandwidth is programmable from 150 kHz to 2 MHz.

PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread spectrum for a PLL affects all of its outputs.

Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. You may need to gate the lock signal for use as a system control. The lock signal from the locked port can drive the logic array or an output pin.

Whenever the PLL loses lock for any reason (be it excessive inclk jitter, clock switchover, PLL reconfiguration, power supply noise etc.), the PLL must be reset with the `areset` signal for correct phase shift operation. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in the design, then the PLL need not be reset.

See the *Stratix GX FPGA Errata Sheet* for more information on implementing the gated lock signal in the design.

Programmable Duty Cycle

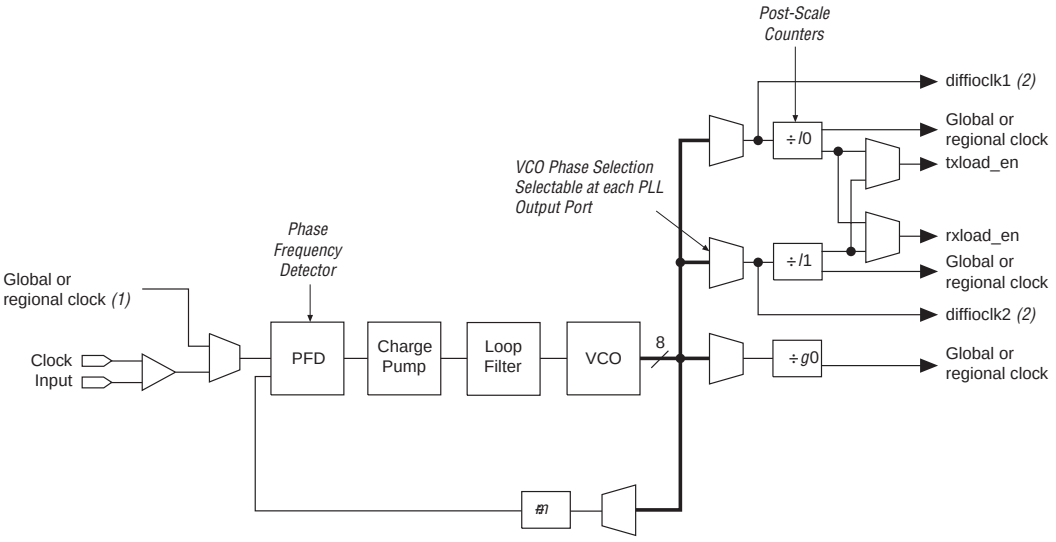
The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

Figure 4–57. Stratix GX Device Fast PLL



Notes to Figure 4–57:

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

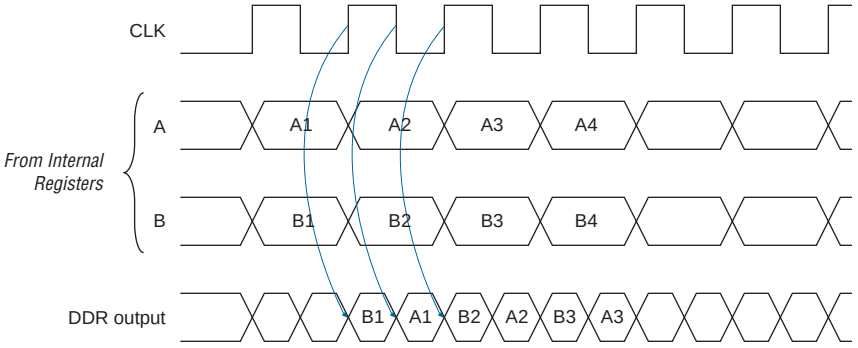
The Stratix GX device's fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output

Figure 4–67. Output Timing Diagram in DDR Mode



The Stratix GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix GX device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix GX devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix GX devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.

In addition to the required signals for external memory interfacing, Stratix GX devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See Figure 4–63.

To find out more about the DDR SDRAM specification, see the JEDEC web site (**www.jedec.org**). For information on memory controller megafunctions for Stratix GX devices, see the Altera web site (**www.altera.com**). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix GX. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

Table 4–24 shows the possible settings for the I/O standards with drive strength control.

Table 4–24. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL class I and II 1.8-V HSTL class I and II SSTL-3 class I and II SSTL-2 class I and II SSTL-18 class I and II	Support maximum and minimum strength

Notes to Table 4–24:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1 and 2 do not support this setting.

The Quartus II software, beginning with version 4.2, reports current strength as "PCI Compliant" for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix GX devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix GX devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

Table 4–33. Stratix GX JTAG Instructions (Part 2 of 2)

JTAG Instruction	Description
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring a Stratix GX device through the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a .jam file or .jbc file with an embedded processor.
PULSE_NCONFIG	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	Allows the IOE standards to be configured through the JTAG chain. Stops configuration if executed during configuration. Can be executed before or after configuration.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 4–33:
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Stratix GX device instruction register length is 10 bits, and the USERCODE register length is 32 bits. Tables 4–34 and 4–35 show the boundary-scan register length and IDCODE information for Stratix GX devices.

Table 4–34. Stratix GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1SGX10	1,029
EP1SGX25	1,665
EP1SGX40	1,941

Table 4–35. 32-Bit Stratix GX Device IDCODE (Part 1 of 2)

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1SGX10	0000	0010 0000 0100 0001	000 0110 1110	1
EP1SGX25	0000	0010 0000 0100 0011	000 0110 1110	1

You can implement the error detection CRC feature with existing circuitry in Stratix GX devices, eliminating the need for external logic. For Stratix GX devices, the CRC is computed by Quartus II and downloaded into the device as a part of the configuration bit stream. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix GX devices to perform error detection automatically. This error detection circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Temperature-Sensing Diode

Stratix GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix GX device and can be used for intelligent power management.

The diode requires two pins (tempdiodep and tempdioden) on the Stratix GX device to connect to the external temperature-sensing device, as shown in Figure 5–4. The temperature-sensing diode is a passive element and therefore can be used before the Stratix GX device is powered.

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 7 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade (1)			-6 Commercial & Industrial Speed Grade (1)			-7 Commercial & Industrial Speed Grade (1)			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output return loss	100 MHz to 2.5 GHz	–10			–10			–10			dB

Notes to Table 6–7:

(1) All numbers for the -6 and -7 speed grades are for both commercial and industrial unless specified otherwise in the Conditions column. Speed grade -5 is available only for commercial specifications.
(2) Not all V_{ID} and equalizer values will get the same results. The condition for the specification was that the V_{ID} before jitter was added is 1,000 mV and the equalizer was set to the maximum condition of 111 (equalizer control setting = 4 in the MegaWizard Plug-In Manager).
(3) Number of parallel clocks.
(4) Receive latency delay from serial receiver indata to parallel receiver data.
(5) Per IEEE Standard 802.3ae @ 3.125 for –5 and –6.
(6) The specification is for channel aligner tolerance.
(7) UI = Unit Interval.
(8) Run-length conditions are true for all data rates, but the average transition density must be enough to keep the receiver phase aligned and the overall data must be DC balanced.
(9) Not all combinations of V_{OD} and pre-emphasis will get the same results.
(10) The numbers are for 3.125-Gbps data rate for –5 and –6 devices and 2.5 Gbps for –7 devices.
(11) Transmitter latency delay from parallel transceiver data to serial transceiver out data.
(12) The receiver operates with a BER of better than 10^{-12} in the presence of an input signal as defined in the XAUI driver template for 3.125 Gbps and in the PCI Exp transmitter eye mask for 2.5 Gbps.

Table 6–8. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA (1)	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA (1)		0.45	V

Table 6–9. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V

Table 6–43. Stratix GX Reset & PLL Lock Time Parameter Descriptions (Part 2 of 2)	
Symbol	**Parameter**
$t_{RX\_FREQLOCK}$	The time until the clock recovery unit (CRU) switches to data mode from lock to reference mode.
$t_{RX\_FREQLOCK2PHASELOCK}$	The time until CRU phase locks to data after switching from lock to data mode.

Figure 6–4 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 6–39 through 6–41.

Figure 6–4. Dual-Port RAM Timing Microparameter Waveform

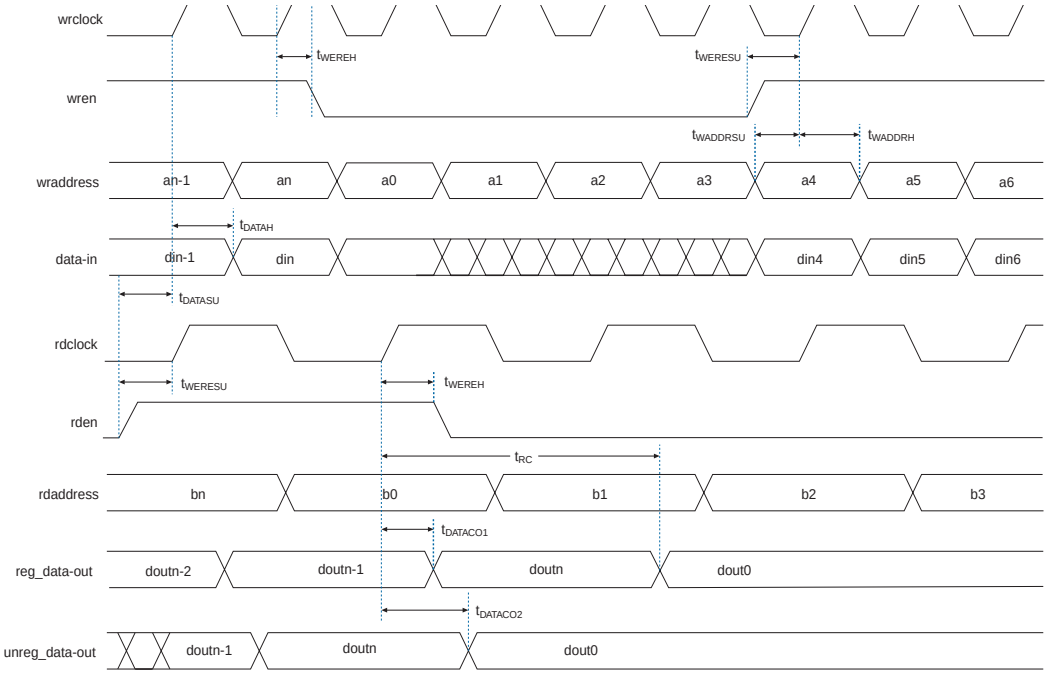


Table 6–50. Stratix GX Transceiver Reset & PLL Lock Time Parameters

Symbol	Min	Typ	Max	Units
$t_{ANALOGRESETPW}$ (5)	1			mS
$t_{DIGITALRESETPW}$ (5)	4			Parallel clock cycle
$t_{TX\_PLL\_LOCK}$ (3)			10	µS
$t_{RX\_FREQLOCK}$ (4)			5	mS
$t_{RX\_FREQLOCK2PHASELOCK}$ (2)			5	µS

Notes to Table 6–50:

(1) The minimum pulse width specified is associated with the power-down of circuits.

(2) The clock recovery unit (CRU) phase locked-to-data time is based on a data rate of 500 Mbps and 8B/10B encoded data.

(3) After `#pll_areset`, `pll_enable`, or PLL power-up, the time required for the transceiver PLL to lock to the reference clock.

(4) After `#rx_analogreset`, the time for the CRU to switch to lock-to-data mode.

(5) There is no maximum pulse width specification. The GXB can be held in reset indefinitely.

Routing delays vary depending on the load on a specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design. Contact Altera Applications Engineering for more details.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 6–6 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Table 6–62. EP1SGX25 Column Pin Global Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.790		1.883		2.120		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.194	2.000	5.569	2.000	6.381	ns
$t_{INSUPLL}$	1.046		1.141		1.220		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.676	0.500	2.813	0.500	3.208	ns

Table 6–63. EP1SGX25 Row Pin Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.394		2.594		2.936		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.456	2.000	4.761	2.000	5.454	ns

Table 6–64. EP1SGX25 Row Pin Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.970		2.109		2.377		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.880	2.000	5.246	2.000	6.013	ns
$t_{INSUPLL}$	1.326		1.386		1.552		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

Table 6–65. EP1SGX25 Row Pin Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.963		2.108		2.379		ns
t_{INH}	0.000		0.000		0.000		ns

Table 6–84. Stratix GX Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.8 V	250	250	250	MHz
1.5 V	225	200	200	MHz
LVCMOS	350	300	250	MHz
GTL	200	167	125	MHz
GTL+	200	167	125	MHz
SSTL-3 class I	167	150	133	MHz
SSTL-3 class II	167	150	133	MHz
SSTL-2 class I	200	200	167	MHz
SSTL-2 class II	200	200	167	MHz
SSTL-18 class I	150	133	133	MHz
SSTL-18 class II	150	133	133	MHz
1.5-V HSTL class I	250	225	200	MHz
1.5-V HSTL class II	225	200	200	MHz
1.8-V HSTL class I	250	225	200	MHz
1.8-V HSTL class II	225	200	200	MHz
3.3-V PCI	350	300	250	MHz
3.3-V PCI-X 1.0	350	300	250	MHz
Compact PCI	350	300	250	MHz
AGP 1×	350	300	250	MHz
AGP 2×	350	300	250	MHz
CTT	200	200	200	MHz
Differential HSTL	225	200	200	MHz
Differential SSTL-2	200	200	167	MHz
LVDS	500	500	500	MHz
LVPECL	500	500	500	MHz
PCML	350	350	350	MHz
HyperTransport technology	350	350	350	MHz

Table 6–85. Stratix GX Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2] Pins (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	400	350	300	MHz
2.5 V	400	350	300	MHz
1.8 V	400	350	300	MHz

Table 6–90. Enhanced PLL Specifications for -7 Speed Grade (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(9)*	0.5		0.6	%
t_{ARESET}	Minimum pulse width on `areset` signal	10			ns

Notes to Tables 6–88 through 6–90:

(1) The minimum input clock frequency to the PFD (f_{IN}/N) must be at least 3 MHz for Stratix device enhanced PLLs.
(2) See "Maximum Input & Output Clock Rates" on page 6–54.
(3) t_{FCOMP} can also equal 50% of the input clock period multiplied by the pre-scale divider *n* (whichever is less).
(4) This parameter is timing analyzed by the Quartus II software because the `scanclk` and `scandata` ports can be driven by the logic array.
(5) Actual jitter performance may vary based on the system configuration.
(6) Total required time to reconfigure and lock is equal to $t_{DLOCK} + t_{CONFIG}$. If only post-scale counters and delays are changed, then t_{DLOCK} is equal to 0.
(7) The VCO range is limited to 500 to 800 MHz when the spread spectrum feature is selected.
(8) Lock time is a function of PLL configuration and may be significantly faster depending on bandwidth settings or feedback counter change increment.
(9) Exact, user-controllable value depends on the PLL settings.
(10) The LOCK circuit on Stratix PLLs does not work for industrial devices below -20C unless the PFD frequency > 200 MHz. See the *Stratix FPGA Errata Sheet* for more information on the PLL.