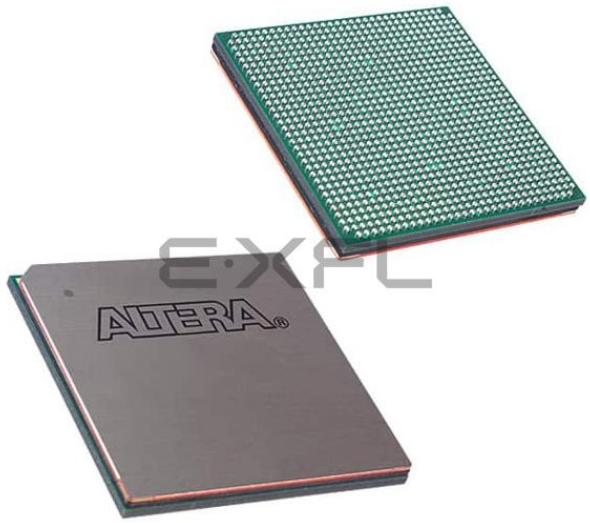

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

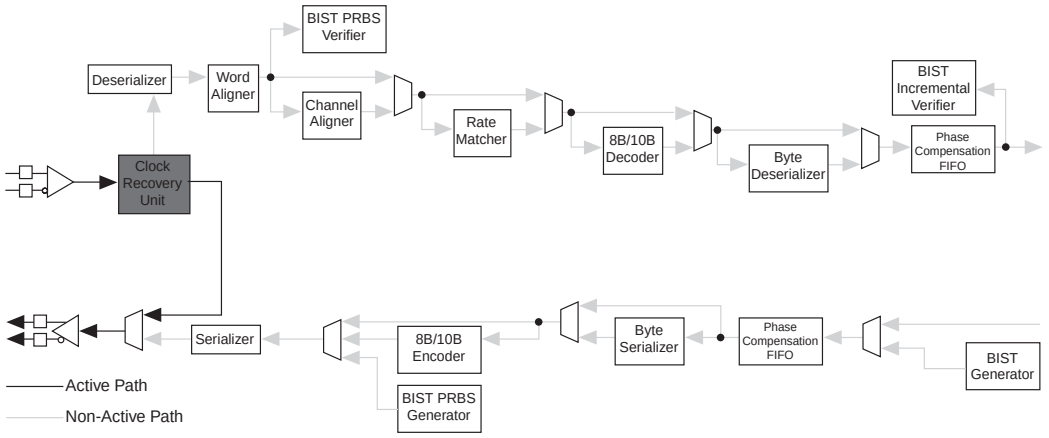
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	607
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx25df1020c6

Figure 2–23. Data Path in Reverse Serial Loopback Mode



BIST (Built-In Self Test)

The Stratix GX transceiver has built-in self test modes to aid in debug and testing. The BIST modes are set in the Stratix GX MegaWizard Plug-In Manager in the Quartus II software. Only one BIST mode can be set for any single instance of the transceiver block. The BIST mode applies to all channels used in a transceiver.

The following is a list of the available BIST modes:

- PRBS generator and verifier
- Incremental mode generator and verifier
- High-frequency generator
- Low-frequency generator
- Mixed-frequency generator

Figures 2–24 and 2–25 are diagrams of the BIST PRBS data path and the BIST incremental data path, respectively.

multiplication value. The ×1 and ×2 operation is also possible by bypassing the SERDES. The SERDES DPA cannot support ×1, ×2, or ×4 natively.

On the receiver side, the high-frequency clock generated by the PLL shifts the serial data through a shift register (also called deserializer). The parallel data is clocked out to the logic array synchronized with the low-frequency clock. On the transmitter side, the parallel data from the logic array is first clocked into a parallel-in, serial-out shift register synchronized with the low-frequency clock and then transmitted out by the output buffers.

There are two dedicated fast PLLs each in EP1SGX10 to EP1SGX25 devices, and four in EP1SGX40 devices. These PLLs are used for the SERDES operations as well as general-purpose use.

Stratix GX Differential I/O Receiver Operation (Non-DPA Mode)

You can configure any of the Stratix GX source synchronous differential input channels as a receiver channel (see Figure 3–1). The differential receiver deserializes the incoming high-speed data. The input shift register continuously clocks the incoming data on the negative transition of the high-frequency clock generated by the PLL clock (×*W*).

The data in the serial shift register is shifted into a parallel register by the RXLOADEN signal generated by the fast PLL counter circuitry on the third falling edge of the high-frequency clock. However, you can select which falling edge of the high frequency clock loads the data into the parallel register, using the data-realignment circuit.

In normal mode, the enable signal RXLOADEN loads the parallel data into the next parallel register on the second rising edge of the low-frequency clock. You can also load data to the parallel register through the TXLOADEN signal when using the data-realignment circuit.

Figure 3–1 shows the block diagram of a single SERDES receiver channel. Figure 3–2 shows the timing relationship between the data and clocks in Stratix GX devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

The logic array sends parallel data to the SERDES transmitter circuit when the TXLOADEN signal is asserted. This signal is generated by the high-speed counter circuitry of the logic array low-frequency clock's rising edge. The data is then transferred from the parallel register into the serial shift register by the TXLOADEN signal on the third rising edge of the high-frequency clock.

Figure 3–3 shows the block diagram of a single SERDES transmitter channel and Figure 3–4 shows the timing relationship between the data and clocks in Stratix GX devices in ×10 mode. *W* is the low-frequency multiplier and *J* is the data parallelization division factor.

Figure 3–3. Stratix GX High-Speed Interface Serialized in ×10 Mode

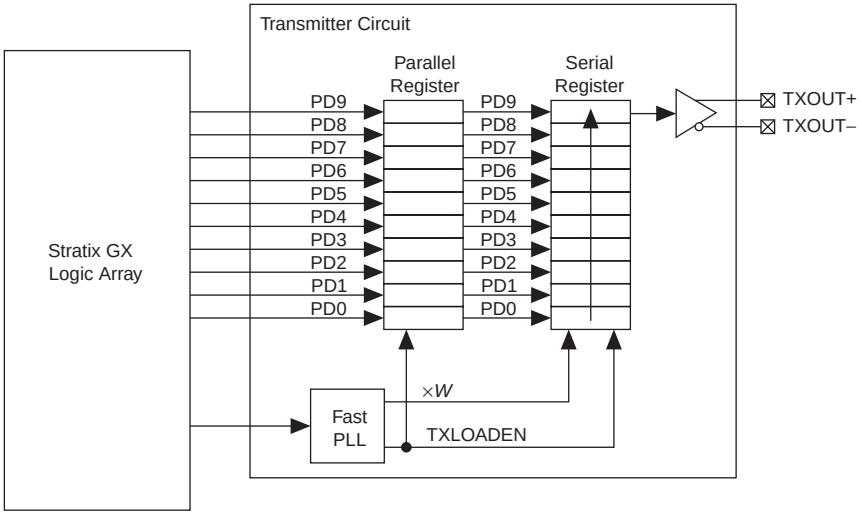
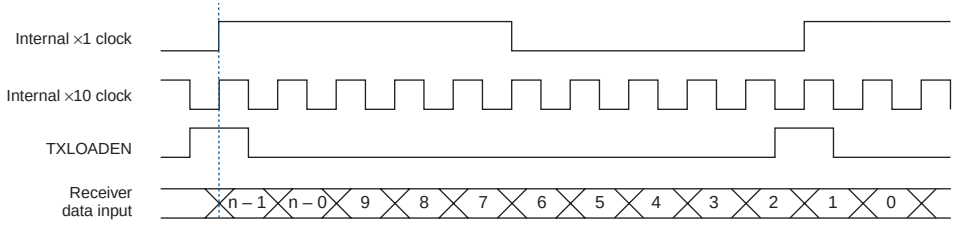


Figure 3–4. Transmitter Timing Diagram

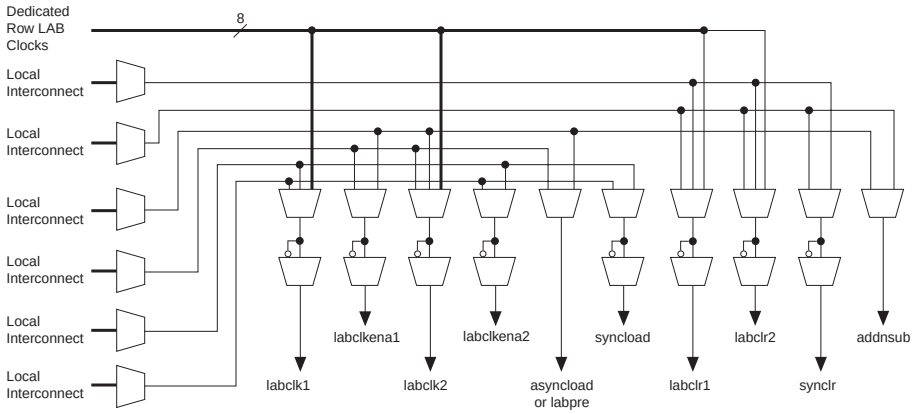


Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 4–3 shows the LAB control signal generation circuit.

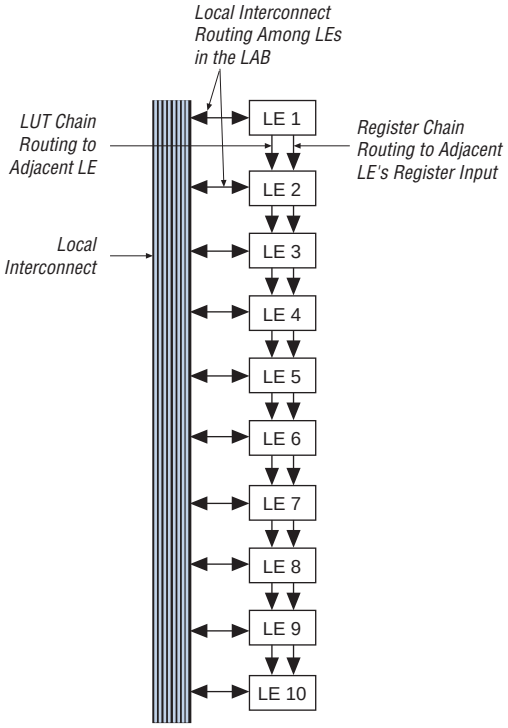
Figure 4–3. LAB-Wide Control Signals



Logic Elements

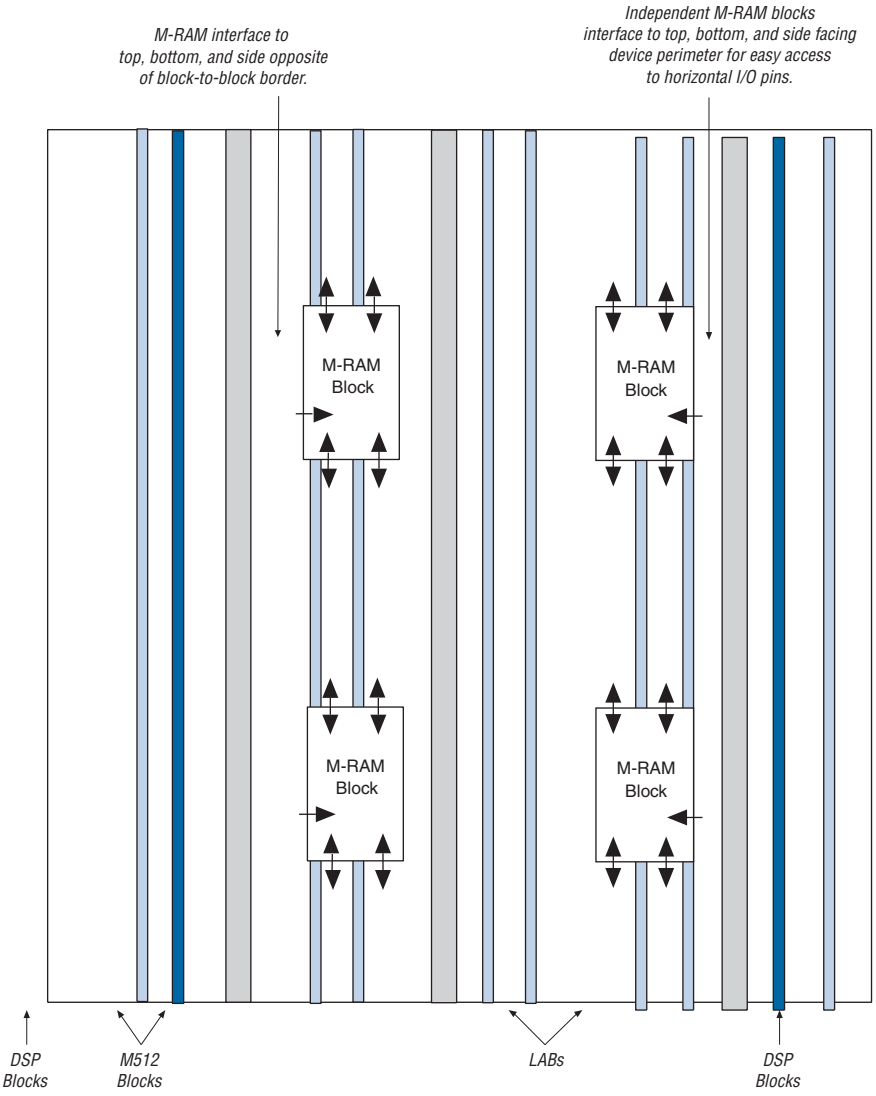
The smallest unit of logic in the Stratix GX architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 4–4.

Figure 4–9. LUT Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 4–10 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and vertical IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect.
C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 4–19. EP1SGX40 Device with M-RAM Interface Locations *Note (1)*



Note to Figure 4–19:
(1) Device shown is an EP1SGX40 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM block are possible from the left adjacent LABs for M-RAM

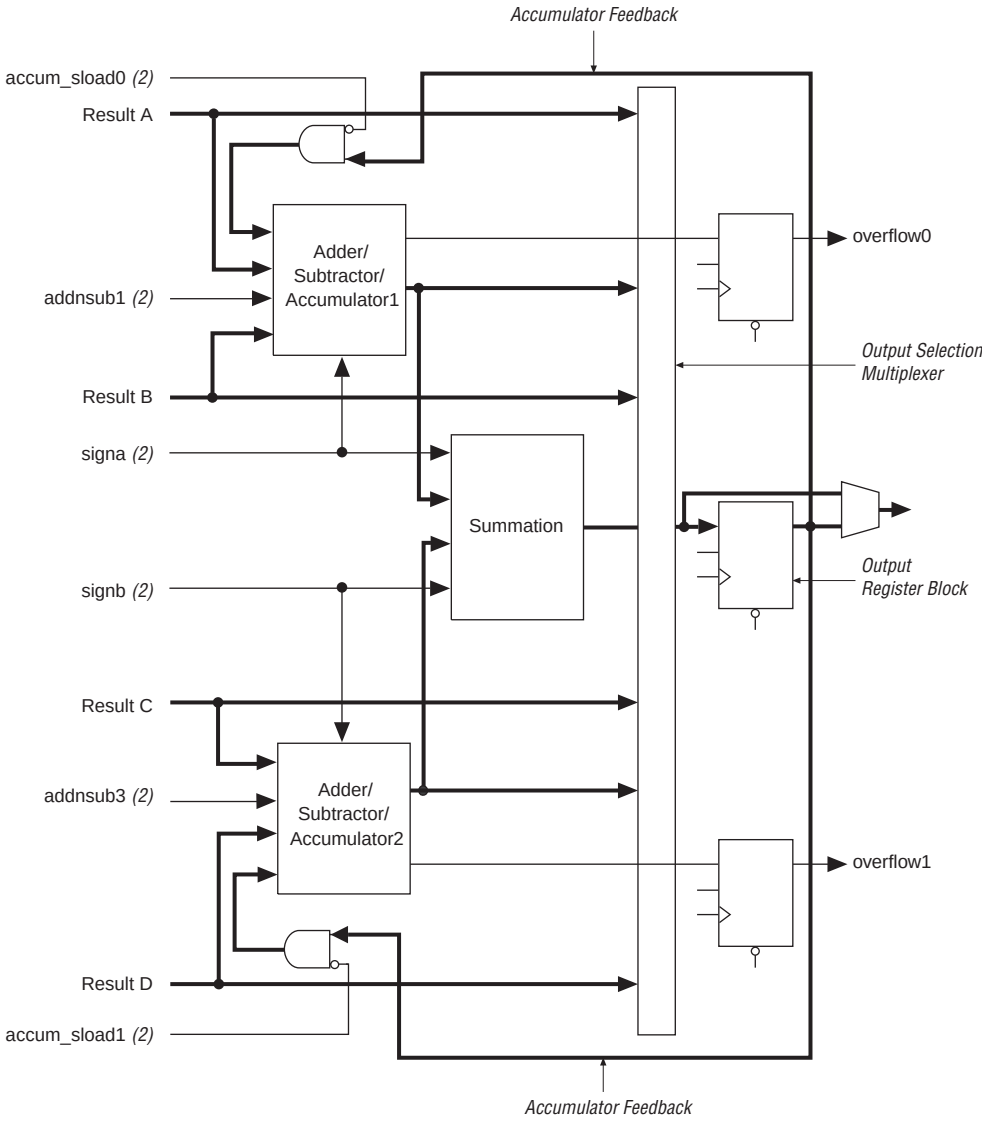
Pipeline/Post Multiply Register

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register pipelines the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. You can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 4–33 shows the adder and output stages.

Figure 4–33. Adder/Output Blocks *Note (1)*



Notes to Figure 4–33:

(1) Adder/output block shown in Figure 4–33 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 40 unique clock domains within EP1SGX10 and EP1SGX25 devices, and 48 unique clock domains within EP1SGX40 devices.

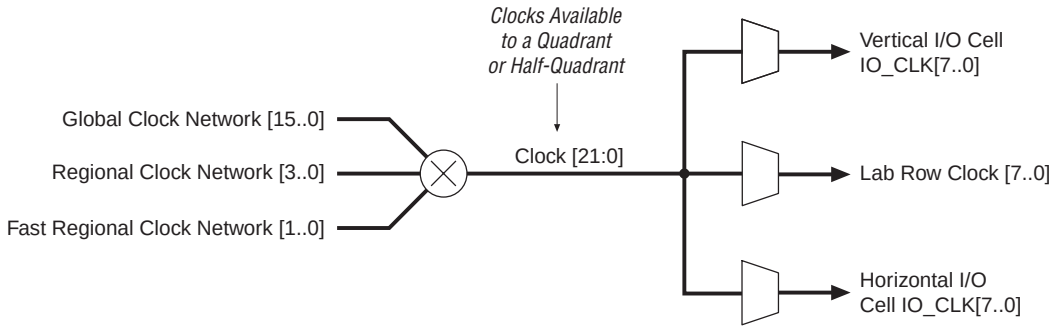
There are 12 dedicated clock pins (CLK[15..12], and CLK[7..0]) to drive either the global or regional clock networks. Three clock pins drive the top, bottom, and left side of the device. Enhanced and fast PLL outputs as well as an I/O interface can also drive these global and regional clock networks.

There are up to 20 recovered clocks (rxclkout[20..0]) and up to 5 transmitter clock outputs (coreclk_out) which can drive any of the global clock networks (CLK[15..0]), as shown in Figure 4–41.

Global Clock Network

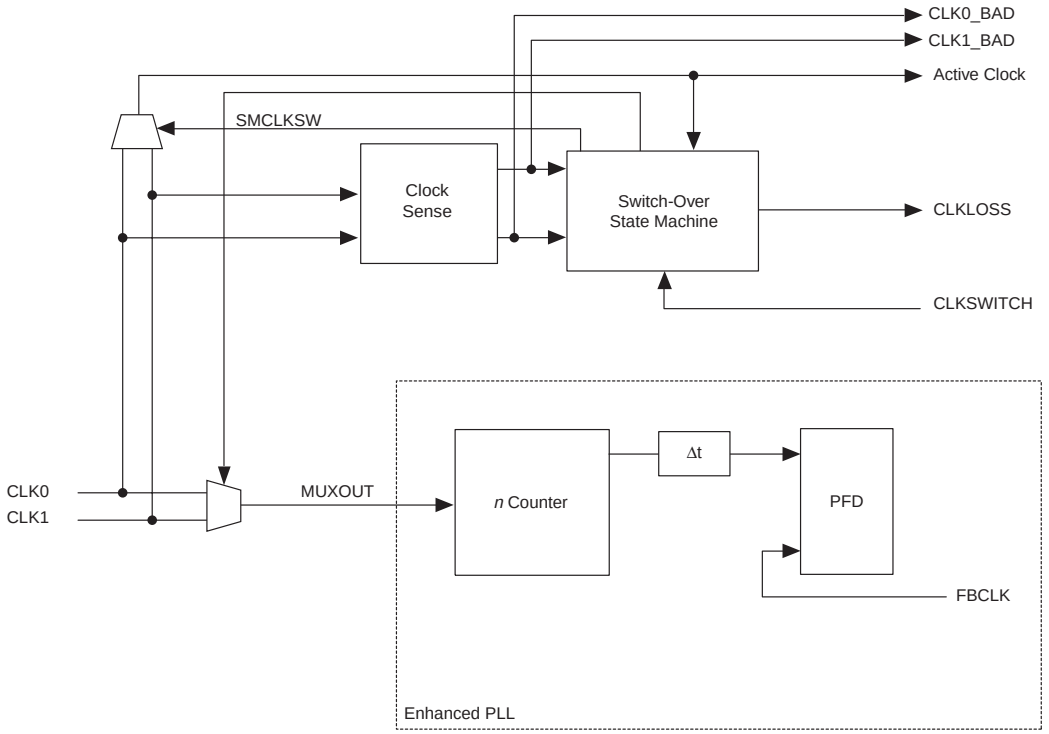
These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 4–41 shows the 12 dedicated CLK pins and the transceiver clocks driving global clock networks.

Figure 4–45. Regional Clock Bus



IOE clocks have horizontal and vertical block regions that are clocked by eight I/O clock signals chosen from the 22-quadrant or half-quadrant clock resources. Figures 4–46 and 4–47 show the quadrant and half-quadrant relationship to the I/O clock regions, respectively. The vertical regions (column pins) have less clock delay than the horizontal regions (row pins).

Figure 4–52. Clock Switchover Circuitry



Note to Figure 4–52:
(1) PFD: phase frequency detector.

There are two possible ways to use the clock switchover feature.

- You can use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 4–52. In this case, the secondary clock becomes the reference clock for the PLL.
- You can use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane,

requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

During switchover, the PLL VCO continues to run and either slows down or speeds up, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The preliminary specification for the maximum time to relock is 100 µs.

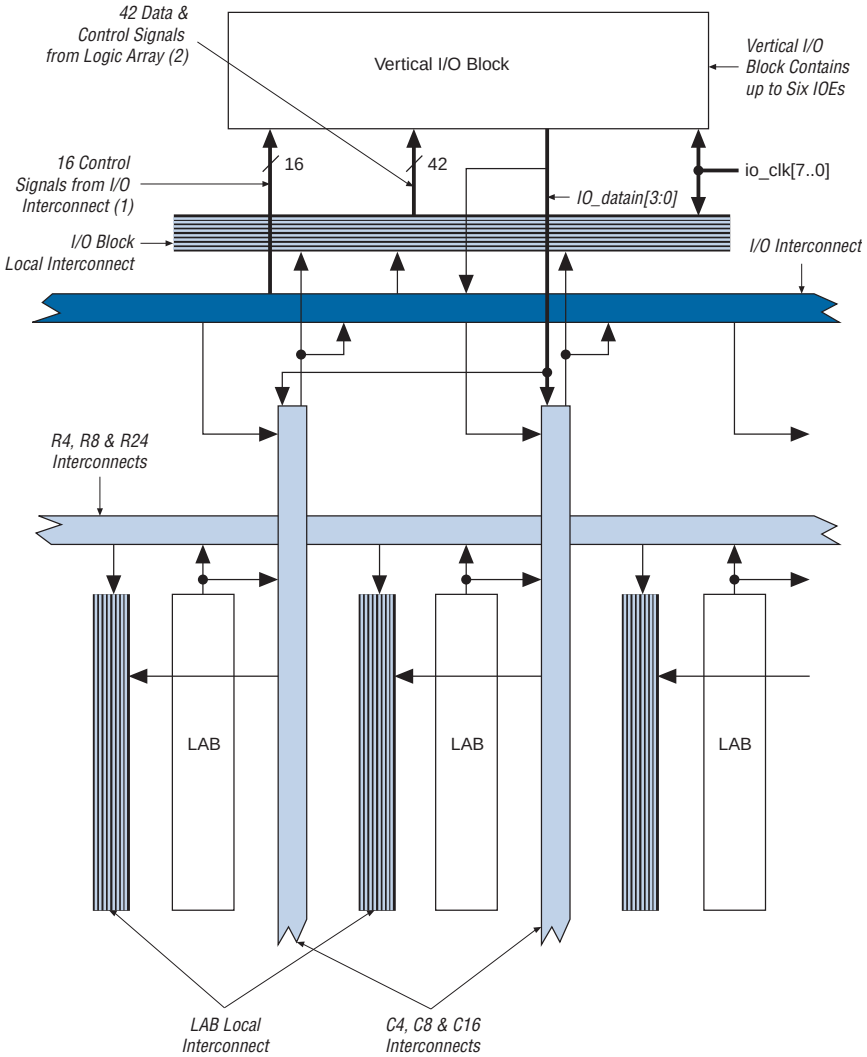
For more information on clock switchover, see *AN313: Implementing Clock Switchover in Stratix & Stratix GX Devices*.

PLL Reconfiguration

The PLL reconfiguration feature enables system logic to change Stratix GX device enhanced PLL counters and delay elements without reloading a Programmer Object File (**.pof**). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. You can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or t_{CO} delays in end systems.

Clock delay elements at each PLL output port implement variable delay. Figure 4–53 shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20 µs for the enhanced PLL using a input shift clock rate of 25 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

Figure 4–60. Column I/O Block Connection to the Interconnect



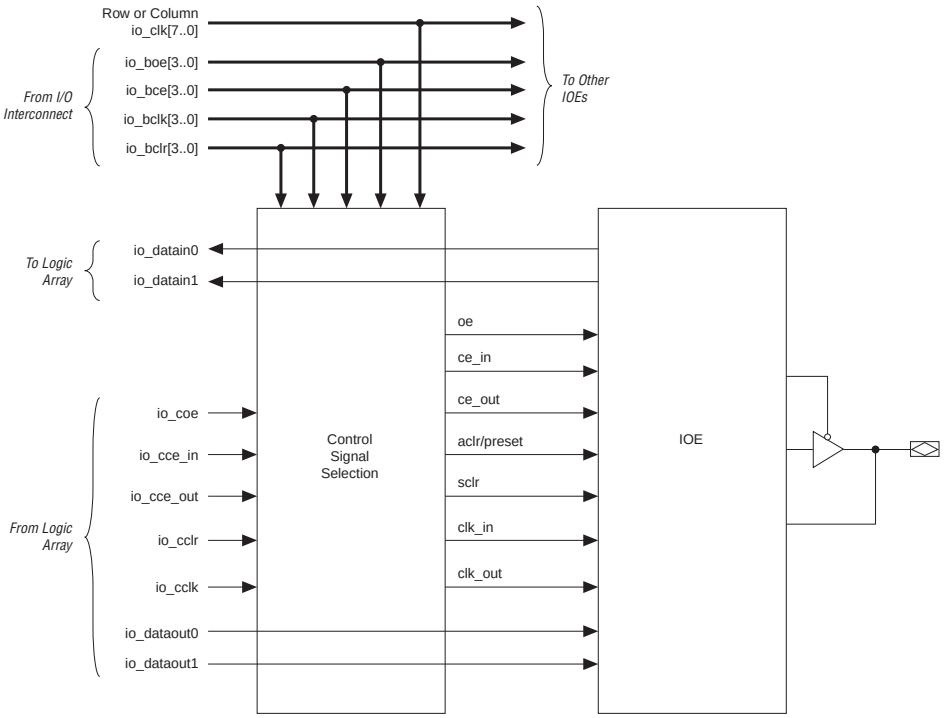
Notes to Figure 4–60:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

Stratix GX devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 4–68). Figure 4–61 illustrates the signal paths through the I/O block.

Figure 4–61. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 4–62 illustrates the control signal selection.

Table 4–28 shows I/O standard support for each I/O bank.

Table 4–28. I/O Support by Bank (Part 1 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓		✓
3.3-V PCI-X 1.0	✓		✓
LVPECL		✓	✓
3.3-V PCML		✓	✓
LVDS		✓	✓
HyperTransport technology		✓	✓
Differential HSTL (clock inputs)	✓	✓	
Differential HSTL (clock outputs)			✓
Differential SSTL (clock outputs)			✓
3.3-V GTL	✓		✓
3.3-V GTL+	✓	✓	✓
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II	✓		✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II	✓		✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II	✓		✓
SSTL-2 class I	✓	✓	✓
SSTL-2 class II	✓	✓	✓
SSTL-3 class I	✓	✓	✓

Table 6–56. EP1SGX10 Column Pin Global Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.785		1.814		2.087		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.057	2.000	5.438	2.000	6.214	ns
$t_{INSUPLL}$	0.988		0.936		1.066		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.634	0.500	2.774	0.500	3.162	ns

Table 6–57. EP1SGX10 Row Pin Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.194		2.384		2.727		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.956	2.000	4.971	2.000	5.463	ns

Table 6–58. EP1SGX10 Row Pin Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.244		2.413		2.574		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.906	2.000	4.942	2.000	5.616	ns
$t_{INSUPLL}$	1.126		1.186		1.352		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.804	0.500	2.627	0.500	2.765	ns

Table 6–59. EP1SGX10 Row Pin Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.919		2.062		2.368		ns
t_{INH}	0.000		0.000		0.000		ns

Table 6–83. Stratix GX Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins (Part 2 of 2)				
I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.8 V	422	422	390	MHz
1.5 V	422	422	390	MHz
LVCMOS	422	422	390	MHz
GTL	300	250	200	MHz
GTL+	300	250	200	MHz
SSTL-3 class I	400	350	300	MHz
SSTL-3 class II	400	350	300	MHz
SSTL-2 class I	400	350	300	MHz
SSTL-2 class II	400	350	300	MHz
SSTL-18 class I	400	350	300	MHz
SSTL-18 class II	400	350	300	MHz
1.5-V HSTL class I	400	350	300	MHz
1.5-V HSTL class II	400	350	300	MHz
1.8-V HSTL class I	400	350	300	MHz
1.8-V HSTL class II	400	350	300	MHz
3.3-V PCI	422	422	390	MHz
3.3-V PCI-X 1.0	422	422	390	MHz
Compact PCI	422	422	390	MHz
AGP 1×	422	422	390	MHz
AGP 2×	422	422	390	MHz
CTT	300	250	200	MHz
Differential HSTL	400	350	300	MHz
LVDS	645	645	640	MHz
LVPECL	645	645	640	MHz
PCML	300	275	275	MHz
HyperTransport technology	645	645	640	MHz

Tables 6–84 and 6–85 show the maximum output clock rate for column and row pins in Stratix GX devices.

Table 6–84. Stratix GX Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 1 of 2)				
I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	350	300	250	MHz
2.5 V	350	300	300	MHz

Table 6–85. Stratix GX Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2] Pins (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.5 V	350	300	300	MHz
LVCMOS	400	350	300	MHz
GTL	200	167	125	MHz
GTL+	200	167	125	MHz
SSTL-3 class I	167	150	133	MHz
SSTL-3 class II	167	150	133	MHz
SSTL-2 class I	150	133	133	MHz
SSTL-2 class II	150	133	133	MHz
SSTL-18 class I	150	133	133	MHz
SSTL-18 class II	150	133	133	MHz
HSTL class I	250	225	200	MHz
HSTL class II	225	225	200	MHz
3.3-V PCI	250	225	200	MHz
3.3-V PCI-X 1.0	225	225	200	MHz
Compact PCI	400	350	300	MHz
AGP 1×	400	350	300	MHz
AGP 2×	400	350	300	MHz
CTT	300	250	200	MHz
Differential HSTL	225	225	200	MHz
LVDS	717	717	500	MHz
LVPECL	717	717	500	MHz
PCML	420	420	420	MHz
HyperTransport technology	420	420	420	MHz

High-Speed I/O Specification

Table 6–86 provides high-speed timing specifications definitions.

Table 6–86. High-Speed Timing Specifications & Definitions (Part 1 of 2)

High-Speed Timing Specification	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
t_{RISE}	Low-to-high transmission time.

Table 6–86. High-Speed Timing Specifications & Definitions (Part 2 of 2)	
High-Speed Timing Specification	**Definitions**
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. SW = t_{SW} (max) – t_{SW} (min).
Input jitter (peak-to-peak)	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 6–87 shows the high-speed I/O timing specifications for Stratix GX devices.

Table 6–87. High-Speed I/O Specifications (Part 1 of 4) Notes (1), (2)											
Symbol	**Conditions**	**-5 Speed Grade**			**-6 Speed Grade**			**-7 Speed Grade**			**Unit**
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
f_{HSCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) f_{HSCLK} = f_{HSDR} / W	*W* = 1 to 30 for ≤717 Mbps W = 2 to 30 for > 717 Mbps	10		717	10		717	10		624	MHz
f_{HSCLK_DPA}		74		717	74		717	74		717	MHz

Table 6–92. Fast PLL Specifications for -7 & -8 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{DUTY}	Duty cycle for DFFIO 1× CLKOUT pin *(3)*	45	55	%
t_{JITTER}	Period jitter for DIFFIO clock out *(3)*		±80	ps
	Period jitter for internal global or regional clock		±100 ps for >200 MHz outclk ±20 mUI for <200 MHz outclk	ps or mUI
t_{LOCK}	Time required for PLL to acquire lock	10	100	µs
m	Multiplication factors for *m* counter *(4)*	1	32	Integer
*l*0, *l*1, *g*0	Multiplication factors for *l*0, *l*1, and *g*0 counter *(4)*, *(5)*	1	32	Integer
t_{ARESET}	Minimum pulse width on areset signal	10		ns

Notes to Tables 6–91 & 6–92:

(1) See "Maximum Input & Output Clock Rates" on page 6–54.
(2) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (that is, the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).
(3) This parameter is for high-speed differential I/O mode only.
(4) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.
(5) High-speed differential I/O mode supports $W = 1$ to 16 and $J = 4, 7, 8,$ or 10.

DLL Jitter

Table 6–93 reports the jitter for the DLL in the DQS phase-shift reference circuit.

Table 6–93. DLL Jitter for DQS Phase Shift Reference Circuit

Frequency (MHz)	DLL Jitter (ps)
197 to 200	± 100
160 to 196	± 300
100 to 159	± 500