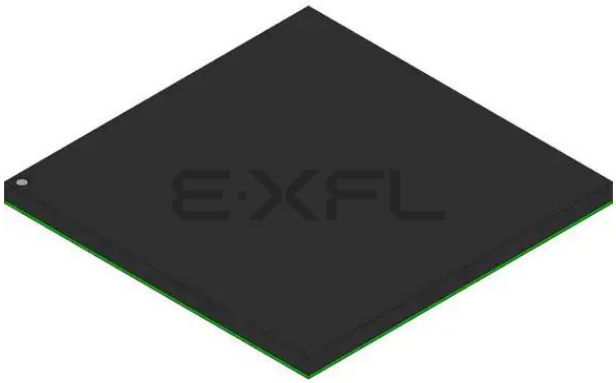

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx25df672c5

Each Stratix GX transceiver channel consists of a transmitter and receiver. The transmitter contains the following:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

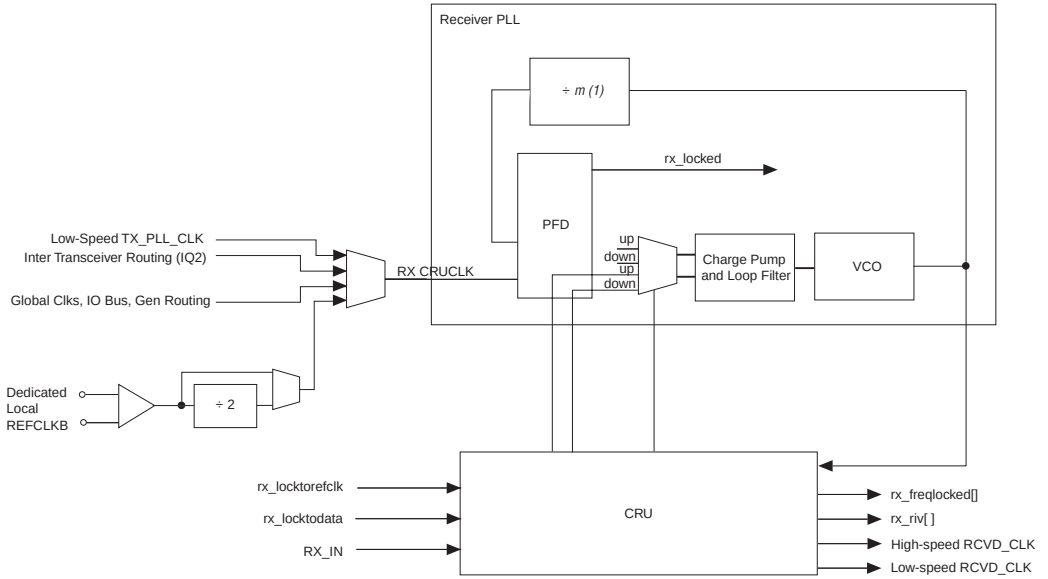
The receiver contains the following:

- Input buffer
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

You can set all the Stratix GX transceiver functions through the Quartus II software. You can set programmable pre-emphasis, programmable equalizer, and programmable V_{OD} dynamically as well. Each Stratix GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. Figure 2–2 shows the block diagram for the Stratix GX transceiver channel.

Stratix GX transceivers provide physical coding sublayer (PCS) and physical media attachment (PMA) implementation for protocols such as 10-gigabit XAUI and GIGE. The PCS portion of the transceiver consists of the logic array interface, 8B/10B encoder/decoder, pattern detector, word aligner, rate matcher, channel aligner, and the BIST and pseudo-random binary sequence pattern generator/verifier. The PMA portion of the transceiver consists of the serializer/deserializer, the CRU, and the I/O buffers.

Figure 2–13. Receiver PLL & CRU Circuit



Note to Figure 2–13:
(1) m = 8, 10 16, or 20.

The receiver PLLs and CRUs are capable of supporting up to 3.1875 Gbps. The input clock frequency for –5 and –6 speed grade devices is limited to 650 MHz if you use the REFCLKB pin or 325 MHz if you use the other clock routing resources. The maximum input clock frequency for –7 speed grade devices is 312.5 MHz if you use the REFCLKB pin or 156.25 MHz with the other clock routing resources. An optional RX_LOCKED port (active low signal) is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth, which can be set to low, medium, or high. The loop bandwidth parameter can be statically set by the Quartus II software.

Table 2–5 lists the adjustable parameters of the receiver PLL and CRU. All the parameters listed are statically programmable in the Quartus II software.

Table 2–5. Receiver PLL & CRU Adjustable Parameters (Part 1 of 2)

Parameter	Specifications
Input reference frequency range	25 MHz to 650 MHz
Data rate support	500 Mbps to 3.1875 Gbps

Figure 2–31. EP1SGX40 Receiver PLL Recovered Clock to Fast Regional Clock Connection

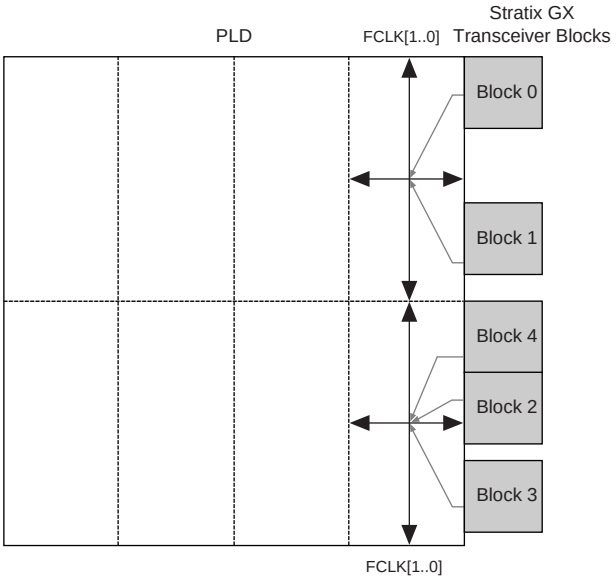


Table 2–10 summarizes the possible clocking connections for the transceivers.

Table 2–10. Possible Clocking Connections for Transceivers (Part 1 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
REFCLKB	✓	✓	✓ *(1)*	✓		✓ *(1)*
Transmitter PLL		✓	✓	✓	✓	
Receiver PLL			✓	✓	✓	
GCLK	✓	✓				
RCLK	✓	✓				
FCLK	✓	✓				

accurately tracked by the internal bias circuit. Moreover, the reference voltage and internal resistor bias current is generated and replicated to the analog circuitry in each channel.

Hot-Socketing Capabilities

Each Stratix GX device is capable of hot-socketing. Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Signals can be driven into Stratix GX devices before and during power-up without damaging the device. Once operating conditions are reached and the device is configured, Stratix GX devices operate according to your specifications. This feature provides the Stratix GX transceiver line card behavior, so you can insert it into the system without powering the system down, offering more flexibility.

Applications & Protocols Supported with Stratix GX Devices

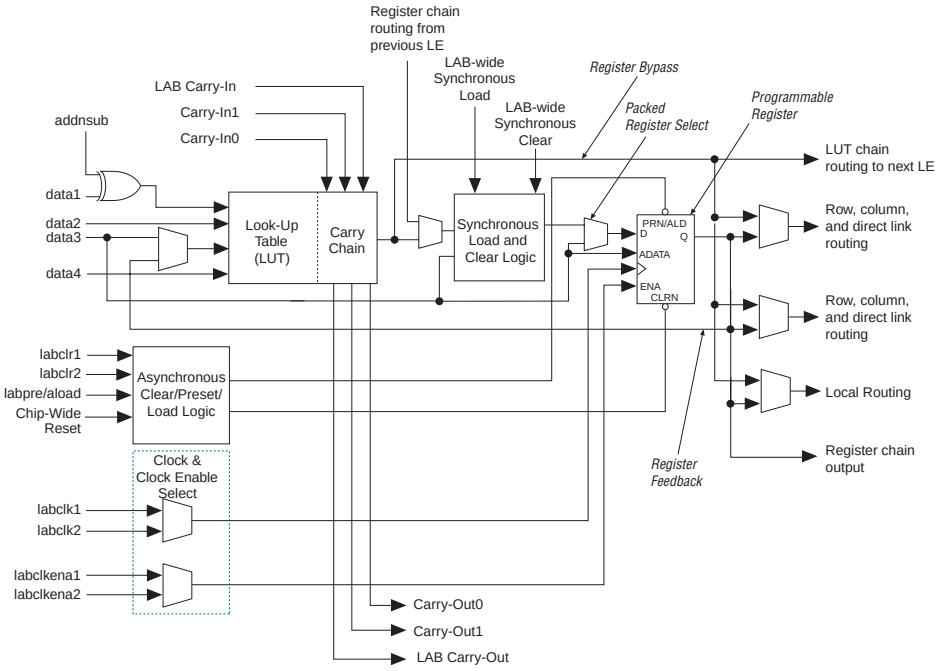
Each Stratix GX transceiver block is designed to operate at any serial bit rate from 500 Mbps to 3.1875 Gbps per channel. The wide, data rate range allows Stratix GX transceivers to support a wide variety of standard and future protocols such as 10-Gigabit Ethernet XAUI, InfiniBand, Fibre Channel, and Serial RapidIO. Stratix GX devices are ideal for many high-speed communication applications such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications standards support.

Stratix GX Example Application Support

Stratix GX devices can be used for many applications, including:

- Backplanes for traffic management and quality of service (QOS)
- Switch fabric applications for complete set for backplane and switch fabric transceivers
- Chip-to-chip applications such as: 10 Gigabit Ethernet XAUI to XGMII bridge, 10 Gigabit Ethernet XGMII to POS-PHY4 bridge, POS-PHY4 to NPSI bridge, or NPSI to backplane bridge

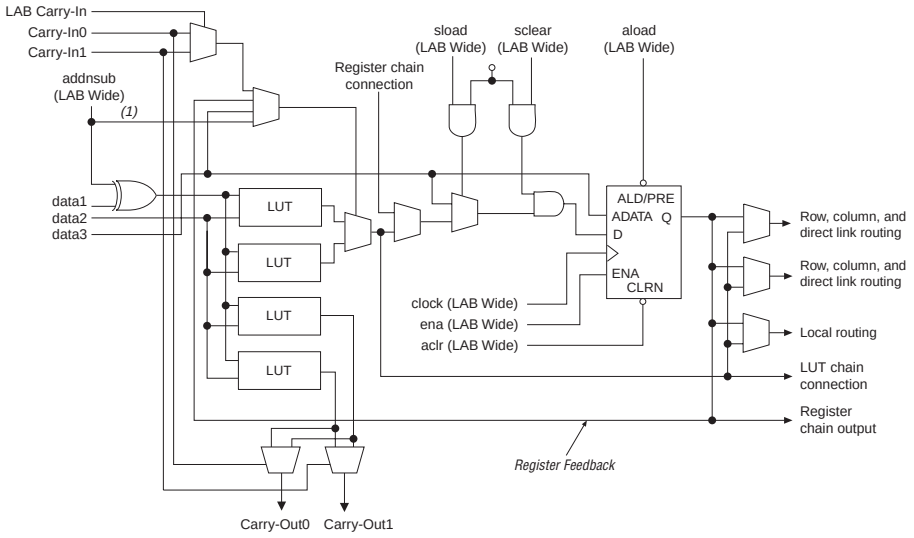
Figure 4–4. Stratix GX LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the register is bypassed and the output of the LUT drives directly to the outputs of the LE.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with

Figure 4–6. LE in Dynamic Arithmetic Mode



Note to Figure 4–6:
(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

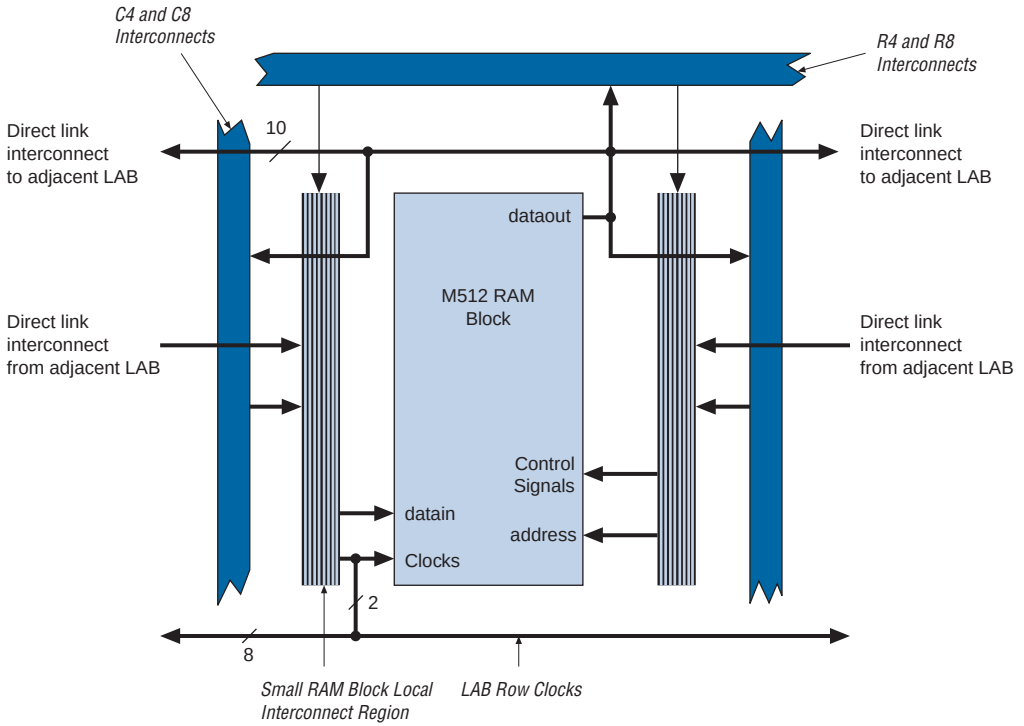
Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Because the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix GX architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 4–7 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used

Figure 4–15. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block implements buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Table 4–12 shows the number of DSP blocks in each Stratix GX device.

Table 4–12. DSP Blocks in Stratix GX Devices *Notes (1), (2)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1SGX10	6	48	24	6
EP1SGX25	10	80	40	10
EP1SGX40	14	112	56	14

Notes to Table 4–12:

(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

(2) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP block multipliers can optionally feed an adder/subtractor or accumulator within the block depending on the configuration. This makes routing to LEs easier, saves LE routing resources, and increases performance, because all connections and blocks are within the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications.

Figure 4–29 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode. Figure 4–30 shows the 9 × 9-bit multiplier configuration of the DSP block.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

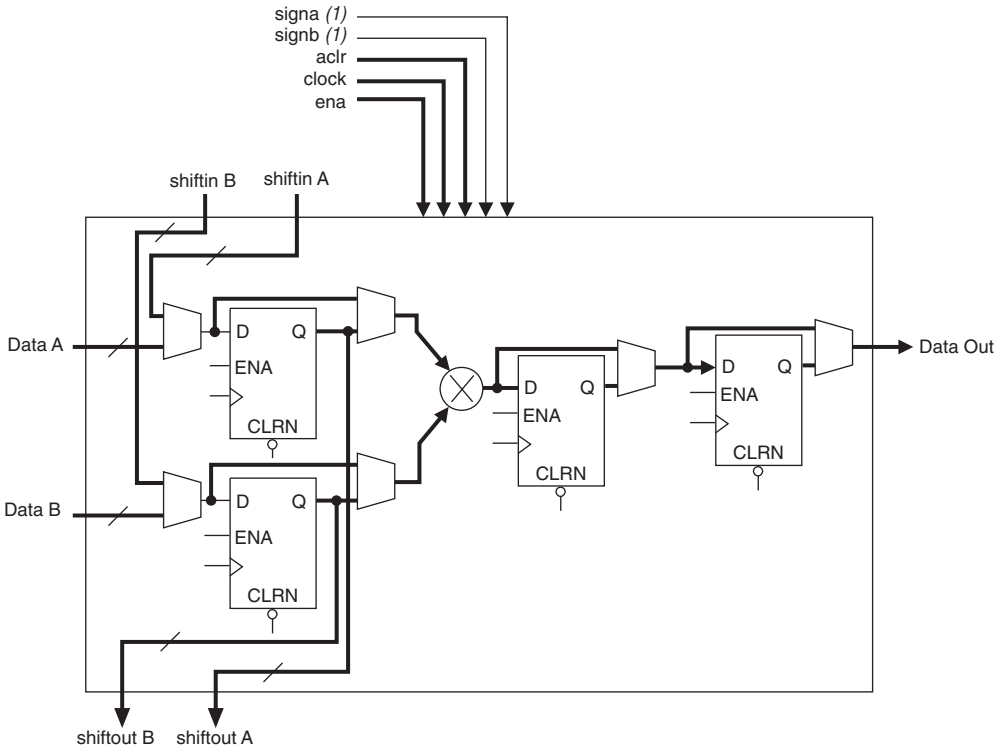
- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18 × 18-bit multipliers or eight 9 × 9-bit multipliers can drive their results directly out of one DSP block. See Figure 4–34.

Figure 4–34. Simple Multiplier Mode



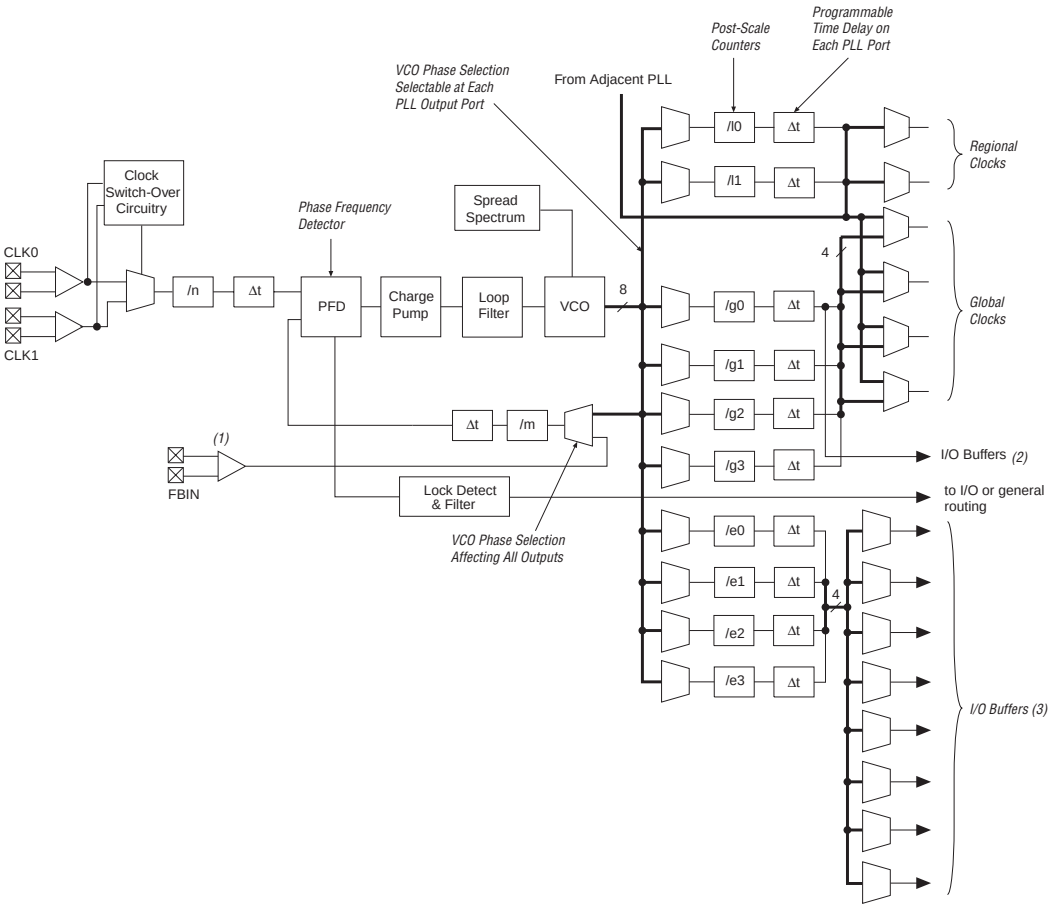
Note to Figure 4–34:
(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 4–35 shows the 36 × 36-bit multiply mode.

Enhanced PLLs

Stratix GX devices contain up to four enhanced PLLs with advanced clock management features. Figure 4–51 shows a diagram of the enhanced PLL.

Figure 4–51. Stratix GX Enhanced PLL



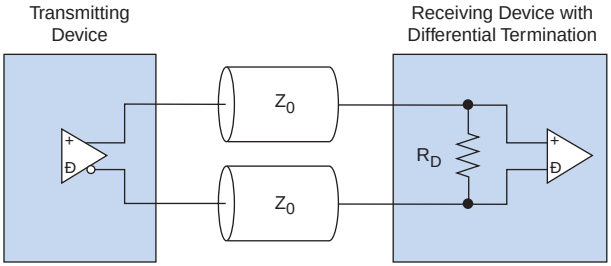
Notes to Figure 4–51:

(1) External feedback is available in PLLs 5 and 6.

(2) This external output is available from the *g*0 counter for PLLs 11 and 12.

(3) These counters and external outputs are available in PLLs 5 and 6.

Figure 4–70. LVDS Input Differential On-Chip Termination



I/O banks on the left and right side of the device support LVDS receiver (far-end) differential termination.

Table 4–29 shows the Stratix GX device differential termination support.

Table 4–29. Differential Termination Supported by I/O Banks

Differential Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)
Differential termination *(1)*, *(2)*	LVDS		✓

Notes to Table 4–29:
(1) Clock pin CLK0, CLK2, CLK9, CLK11, and pins FPLL[7..10]CLK do not support differential termination.
(2) Differential termination is only supported for LVDS because of a 3.3-V V_{CCIO}.

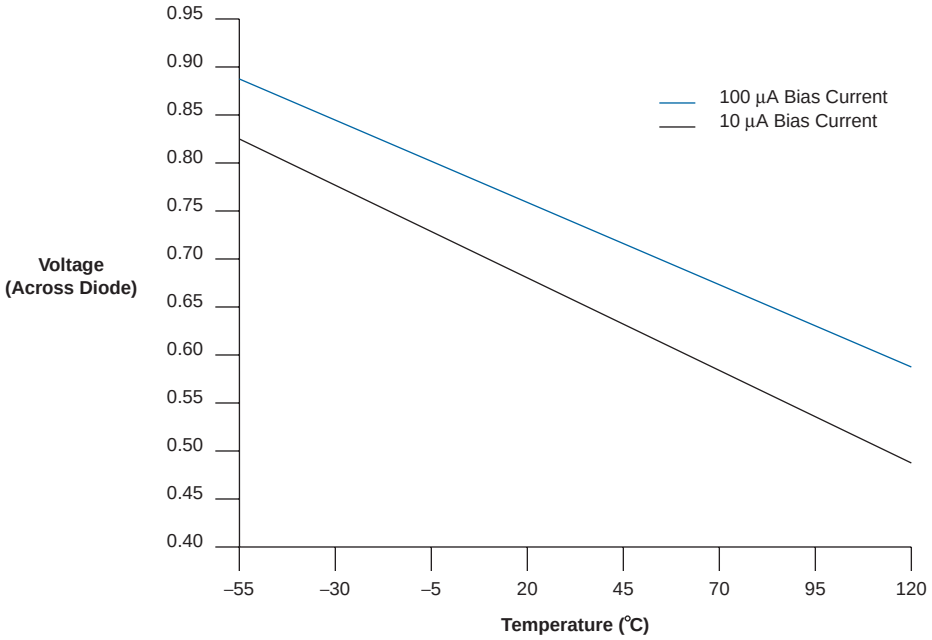
Table 4–30 shows the termination support for different pin types.

Table 4–30. Differential Termination Support Across Pin Types

Pin Type	R_D
Top and bottom I/O banks (3, 4, 7, and 8)	
DIFFIO_RX[]	✓
CLK[0,2,9,11],CLK[4-7],CLK[12-15]	
CLK[1,3,8,10]	✓
FCLK	
FPLL[7..10]CLK	

The differential on-chip resistance at the receiver input buffer is 118 Ω ±20 %.

Figure 5–5. Temperature Versus Temperature-Sensing Diode Voltage



Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 6–36 through 6–42 describe the Stratix GX device internal timing microparameters for LEs, IOEs, TriMatrix™ memory structures, DSP blocks, and MultiTrack interconnects.

Table 6–36. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinational LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 6–37. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	IOE input and output register setup time before clock
t_{H}	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.245		2.332		2.666		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.597	2.000	4.920	2.000	5.635	ns

Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.114		2.218		2.348		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.728	2.000	5.078	2.000	6.004	ns
$t_{INSUPLL}$	1.035		0.941		1.070		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.629	0.500	2.769	0.500	3.158	ns

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		180		189		217	ps
1.5-V HSTL class I		120		126		144	ps
1.5-V HSTL class II		120		126		144	ps
1.8-V HSTL class I		70		73		83	ps
1.8-V HSTL class II		70		73		83	ps

Table 6–73. Stratix GX I/O Standard Row Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		30		31		35	ps
1.8-V LVTTL		150		157		180	ps
1.5-V LVTTL		210		220		252	ps
GTL		0		0		0	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		80		84		96	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		0		0		0	ps
1.5-V HSTL class I		130		136		156	ps

Table 6–74. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)

Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
GTL+		–110		–115		–133	ps
3.3-V PCI		–230		–241		–277	ps
3.3-V PCI-X 1.0		–230		–241		–277	ps
Compact PCI		–230		–241		–277	ps
AGP 1×		–30		–31		–36	ps
AGP 2×		–30		–31		–36	ps
CTT		50		53		61	ps
SSTL-3 class I		90		95		109	ps
SSTL-3 class II		–50		–52		–60	ps
SSTL-2 class I		100		105		120	ps
SSTL-2 class II		20		21		24	ps
SSTL-18 class I		230		242		278	ps
SSTL-18 class II		0		0		0	ps
1.5-V HSTL class I		380		399		459	ps
1.5-V HSTL class II		190		200		230	ps
1.8-V HSTL class I		380		399		459	ps
1.8-V HSTL class II		390		410		471	ps

Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		570		599		689	ps
	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	24 mA		0		0		0	ps
3.3-V LVTTL	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	16 mA		70		74		85	ps
	24 mA		0		0		0	ps

Table 6–87. High-Speed I/O Specifications (Part 2 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSDR} Device operation (LVDS, LVPECL, HyperTransport technology)	*J* = 10	300		840	300		840	300		840	Mbps
	J = 8	300		840	300		840	300		840	Mbps
	J = 7	300		840	300		840	300		840	Mbps
	J = 4	300		840	300		840	300		840	Mbps
	J = 2	100		624	100		624	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		462	100		462	100		462	Mbps
$f_{HSDRDPA}$ (LVDS, LVPECL)	J=10	300		1000	300		840	300		840	Mbps
	J=8	300		1000	300		840	300		840	Mbps
f_{HSCLK} (Clock frequency) (PCML) f_{HSCLK} = f_{HSDR} / W	*W* = 1 to 30	10		400	10		400	10		311	MHz
f_{HSDR} Device operation (PCML)	*J* = 10	300		400	300		400	300		311	Mbps
	J = 8	300		400	300		400	300		311	Mbps
	J = 7	300		400	300		400	300		311	Mbps
	J = 4	300		400	300		400	300		311	Mbps
	J = 2	100		400	100		400	100		300	Mbps
	J = 1	100		250	100		250	100		200	Mbps
DPA Run Length				6400			6400			6400	UI
DPA Jitter Tolerance$_{(p-p)}$	all data rates			0.44			0.44			0.44	UI
DPA Minimum Eye opening (p-p)		0.56			0.56			0.56			UI
DPA Receiver Latency		5		9	5		9	5		9	*(3)*