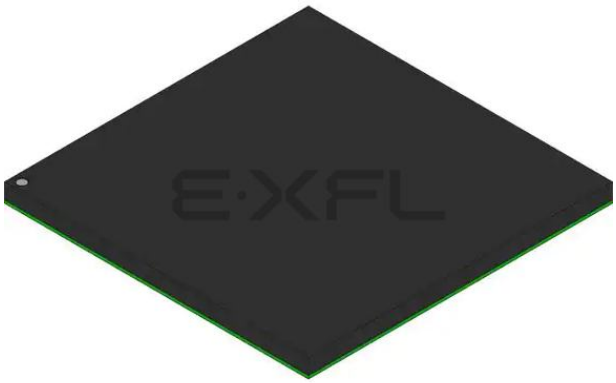


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

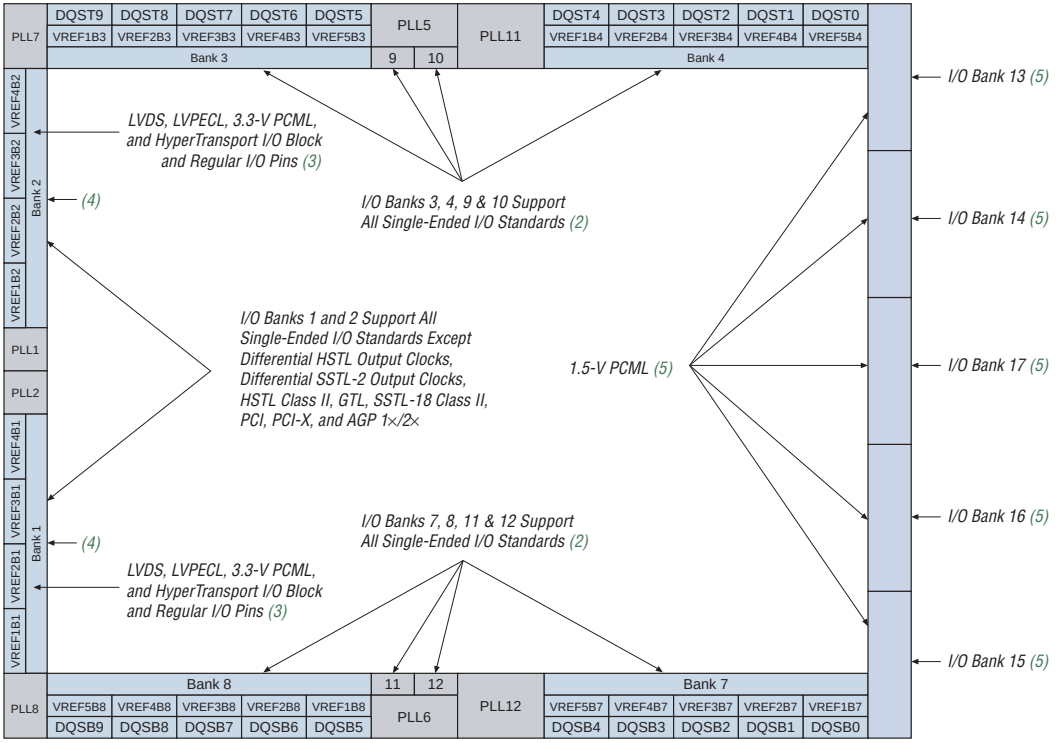
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	455
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx25df672c7

- Pattern detector and word aligner supports programmable patterns
- 8B/10B encoder/decoder performs 8- to 10-bit encoding and 10- to 8-bit decoding
- Rate matcher compliant with IEEE 802.3-2002 for GigE mode and with IEEE 802-3ae for XAUI mode
- Channel bonding compliant with IEEE 802.3ae (for XAUI mode only)
- Device can bypass some transceiver block features if necessary

- FPGA features are as follows:
  - 10,570 to 41,250 logic elements (LEs); see Table 1–1
  - Up to 3,423,744 RAM bits (427,968 bytes) available without reducing logic resources
  - TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in-out (FIFO) buffers
  - Up to 16 global clock networks with up to 22 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to eight general usage phase-locked loops (four enhanced PLLs and four fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 45 channels for 1-Gbps performance
  - Support for source-synchronous bus standards, including 10-Gigabit Ethernet XSBI, Parallel RapidIO, UTOPIA IV, Network Packet Streaming Interface (NPSI), HyperTransport™ technology, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
  - Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - Support for remote configuration updates
  - Dynamic phase alignment on LVDS receiver channels

Figure 1–1. Stratix GX I/O Blocks *Note (1)*



Notes to Figure 1–1:

(1) Figure 1–1 is a top view of the Stratix GX silicon die.
(2) Banks 9 through 12 are enhanced PLL external clock output banks.
(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.
(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.
(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled).

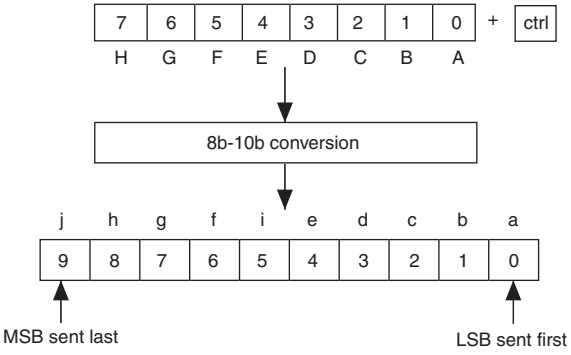
FPGA Functional Description

Stratix GX devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

8B/10B Encoder

The 8B/10B encoder translates 8-bit wide data + 1 control enable bit into a 10-bit encoded data. The encoded data has a maximum run length of 5. The 8B/10B encoder can be bypassed. Figure 2–4 diagrams the encoding process.

Figure 2–4. Encoding Process



Transmit State Machine

The transmit state machine operates in either XAUI mode or in GIGE mode, depending on the protocol used.

GIGE Mode

In GIGE mode, the transmit state machines convert all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by (/K28.5/, /D21.5/) and (/K28.5/, /D2.2/), respectively.) Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set. The GIGE transmit state machine can be statically disabled in the Quartus II software, even if using the GIGE protocol mode.

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 2 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 16-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 20-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111
Incremental 10-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
Incremental 20-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
High frequency	1010101010		
Low frequency	0011111000		
Mixed frequency	0011111010 or 1100000101		

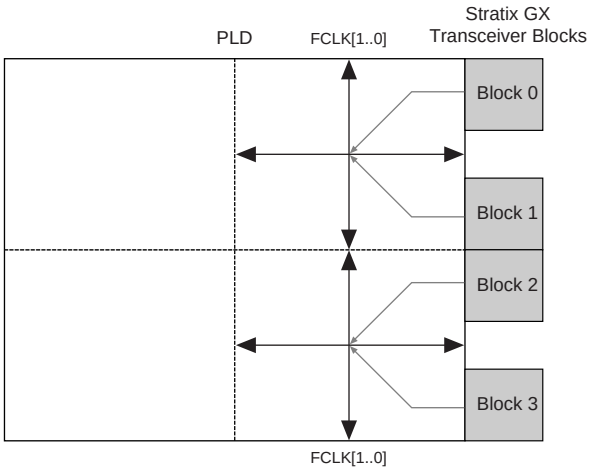
Note to Table 2–9:
(1) This output repeats.

Stratix GX Clocking

The Stratix GX global clock can be driven by certain REFCLKB pins, all transmitter PLL outputs, and all receiver PLL outputs. The REFCLKB pins (except for transceiver block 0 and transceiver block 4) can drive inter-transceiver and global clock lines as well as feed the transmitter and receiver PLLs. The output of the transmitter PLL can only feed global clock lines and the reference clock port of the receiver PLL.

Figures 2–26 and 2–27 are diagrams of the Inter-Transceiver line connections as well as the global clock connections for the EP1SGX25F and EP1SGX40G devices. For devices with fewer transceivers, ignore the information about the unavailable transceiver blocks.

Figure 2–29. EP1SGX25 Receiver PLL Recovered Clock to Fast Regional Clock Connection



In the EP1SGX40 device, the receiver PLL recovered clocks from transceivers 0 and 1 drive `RCLK[1..0]` while transceivers 2, 3, and 4 drive `RCLK[7..6]`. The regional clocks feed logic in their associated regions.

LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

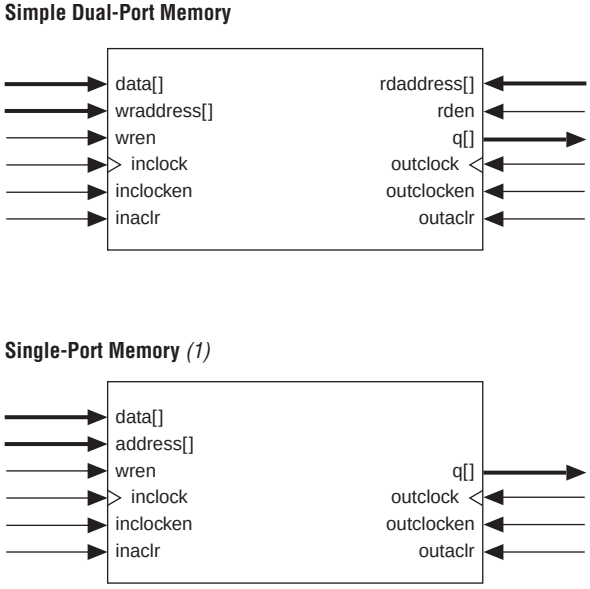
The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix GX devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 4–9 shows the LUT chain and register chain interconnects.

occurs or just read the don't care bits. Single-port memory supports non-simultaneous reads and writes, but the q[] port outputs the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see the *TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*. Figure 4–12 shows these different RAM memory port configurations for TriMatrix memory.

Figure 4–12. Simple Dual-Port & Single-Port Memory Configurations



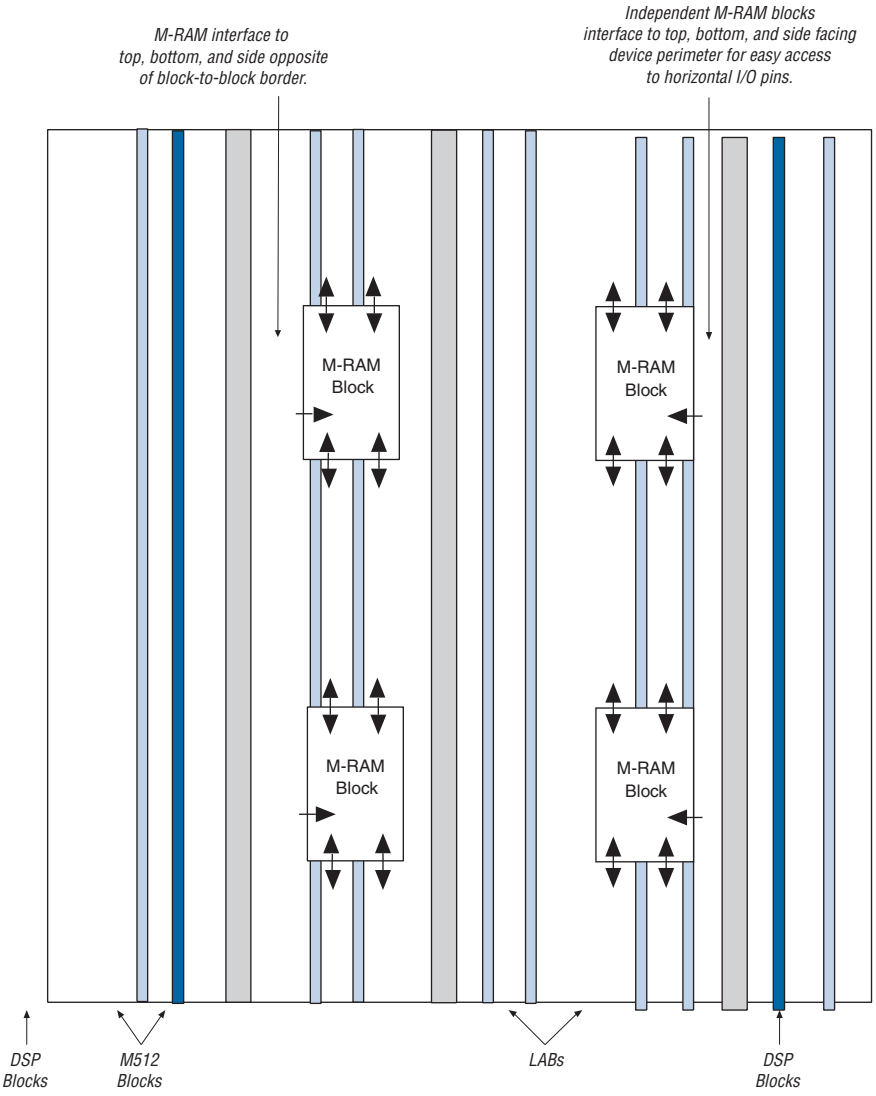
Note to Figure 4–12:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (WREN) signal derived from the global

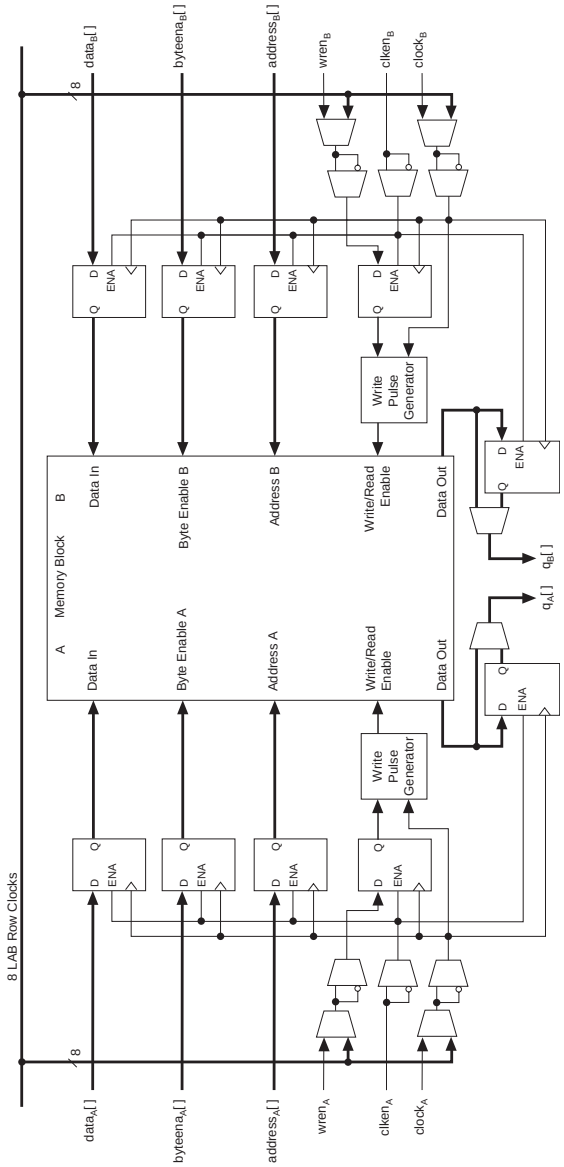
Figure 4–19. EP1SGX40 Device with M-RAM Interface Locations *Note (1)*



Note to Figure 4–19:
(1) Device shown is an EP1SGX40 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM block are possible from the left adjacent LABs for M-RAM

Figure 4–23. Independent Clock Mode *Note (1)*



Note to Figure 4–23:
(1) All registers shown have asynchronous clear ports.

Figure 4–48. PLL Floorplan

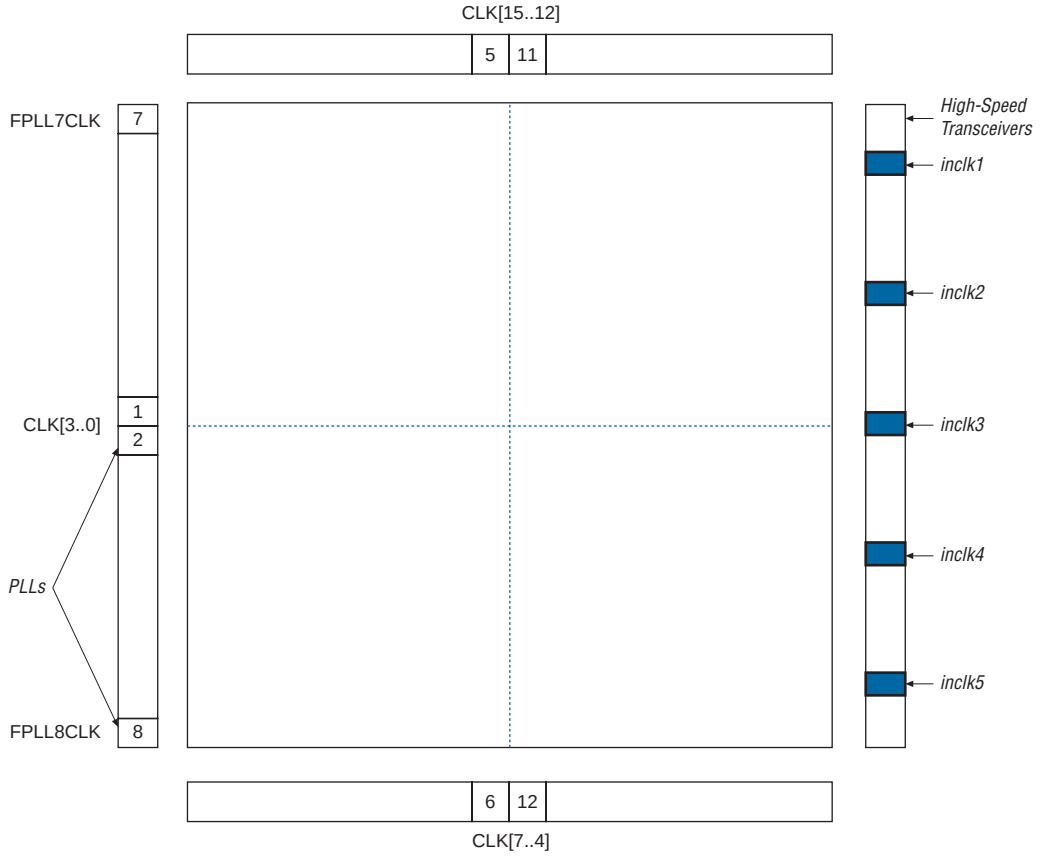


Figure 4–49 shows the global and regional clock connections from the PLL outputs and the CLK pins.

Slew-Rate Control

The output buffer for each Stratix GX device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Bus Hold

Each Stratix GX device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

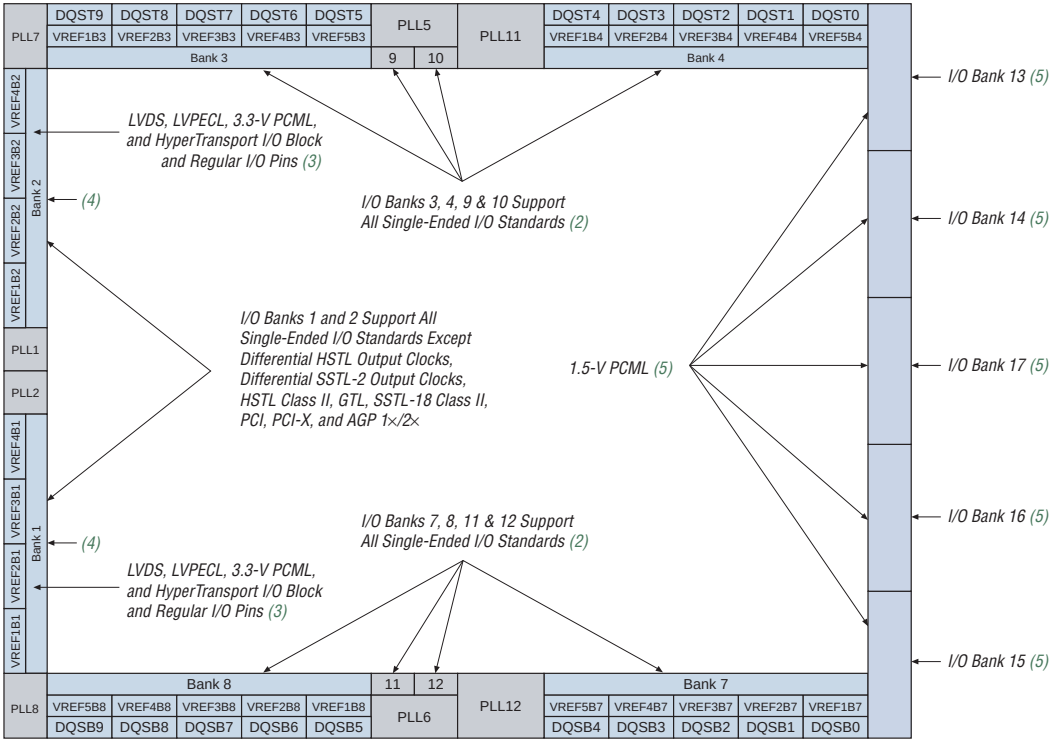
Table 4–25 shows bus hold support for different pin types.

Table 4–25. Bus Hold Support

Pin Type	Bus Hold
I/O pins	✓
CLK[15..0]	
CLK[0,1,2,3,8,9,10,11]	
FCLK	✓
FPLL[7..10]CLK	

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

Figure 4–69. Stratix GX I/O Banks *Notes (1), (2), (3)*



Notes to Figure 4–69:

(1) Figure 4–69 is a top view of the Stratix GX silicon die.

(2) Banks 9 through 12 are enhanced PLL external clock output banks.

(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix GX Device Handbook, Volume 2*.

(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled)

Table 4–35. 32-Bit Stratix GX Device IDCODE (Part 2 of 2)

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1SGX40	0000	0010 0000 0100 0101	000 0110 1110	1

Notes to Table 4–35:
(1) The most significant bit (MSB) is at the left end of the string.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 4–72 shows the timing requirements for the JTAG signals.

Figure 4–72. Stratix GX JTAG Waveforms

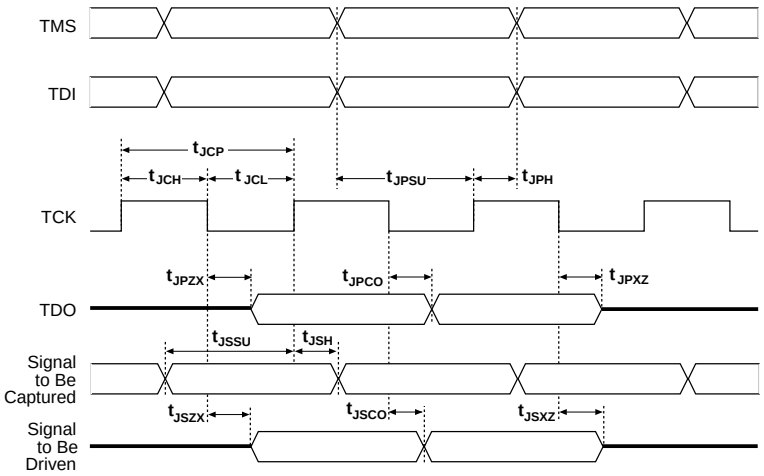
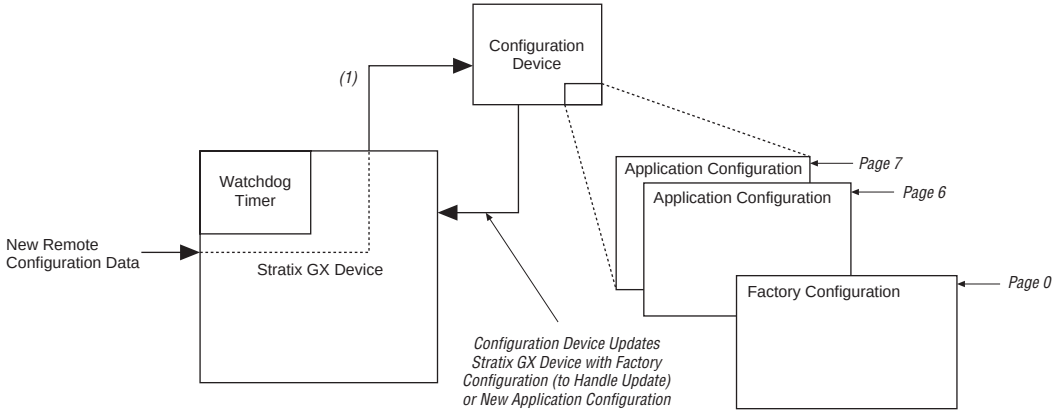


Table 4–36 shows the JTAG timing parameters and values for Stratix GX devices.

Table 4–36. Stratix GX JTAG Timing Parameters & Values (Part 1 of 2)

Symbol	Parameter	Min (ns)	Max (ns)
t_{JCP}	TCK clock period	100	
t_{JCH}	TCK clock high time	50	
t_{JCL}	TCK clock low time	50	
t_{JPSU}	JTAG port setup time	20	

Figure 5–1. Stratix GX Device Remote Update



Note to Figure 5–1:

(1) When the Stratix GX device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Figure 5–5. Temperature Versus Temperature-Sensing Diode Voltage

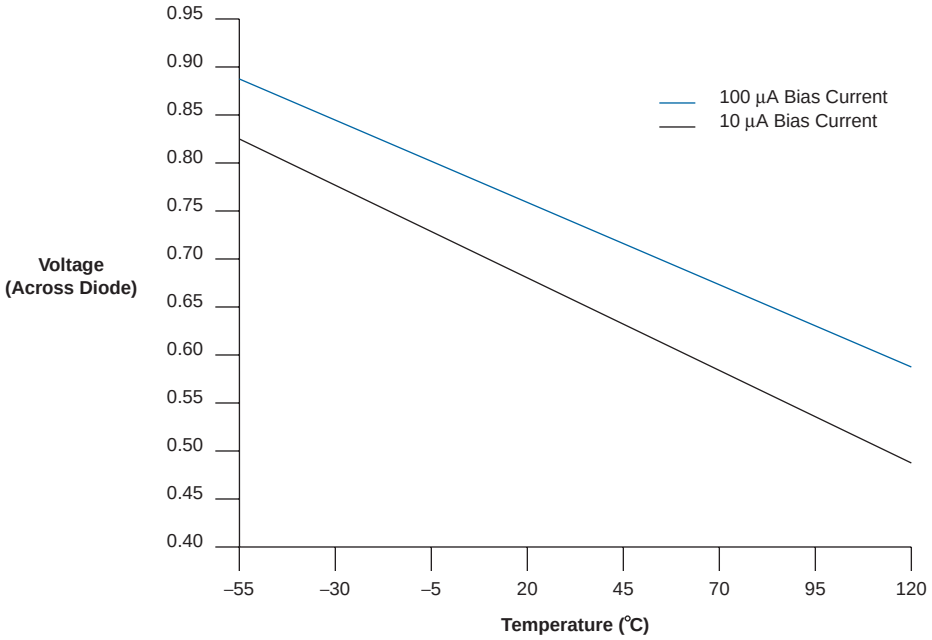


Table 6–21. SSTL-18 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Table 6–22. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			V_{TT} – 0.630	V

Table 6–23. SSTL-2 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V

Table 6–50. Stratix GX Transceiver Reset & PLL Lock Time Parameters

Symbol	Min	Typ	Max	Units
$t_{ANALOGRESETPW}$ (5)	1			mS
$t_{DIGITALRESETPW}$ (5)	4			Parallel clock cycle
$t_{TX\_PLL\_LOCK}$ (3)			10	µS
$t_{RX\_FREQLOCK}$ (4)			5	mS
$t_{RX\_FREQLOCK2PHASELOCK}$ (2)			5	µS

Notes to Table 6–50:

(1) The minimum pulse width specified is associated with the power-down of circuits.

(2) The clock recovery unit (CRU) phase locked-to-data time is based on a data rate of 500 Mbps and 8B/10B encoded data.

(3) After `#pll_areset`, `pll_enable`, or PLL power-up, the time required for the transceiver PLL to lock to the reference clock.

(4) After `#rx_analogreset`, the time for the CRU to switch to lock-to-data mode.

(5) There is no maximum pulse width specification. The GXB can be held in reset indefinitely.

Routing delays vary depending on the load on a specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design. Contact Altera Applications Engineering for more details.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 6–6 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.245		2.332		2.666		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.597	2.000	4.920	2.000	5.635	ns

Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.114		2.218		2.348		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.728	2.000	5.078	2.000	6.004	ns
$t_{INSUPLL}$	1.035		0.941		1.070		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.629	0.500	2.769	0.500	3.158	ns

Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OUTCO}	2.000	5.365	2.000	5.775	2.000	6.621	ns
$t_{INSUPLL}$	1.126		1.186		1.352		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

External I/O Delay Parameters

External I/O delay timing parameters, both for I/O standard input and output adders and programmable input and output delays, are specified by speed grade, independent of device density.

Tables 6–72 through 6–77 show the adder delays associated with column and row I/O pins. If an I/O standard is selected other than LVTTL 24 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters.

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		30		31		35	ps
1.8-V LVTTL		150		157		180	ps
1.5-V LVTTL		210		220		252	ps
GTL		220		231		265	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		120		126		144	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps

7. Reference & Ordering Information

SGX51007-1.0

Software

Stratix® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes hardware description language and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® logic analysis, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v6.2 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Stratix GX devices will be released on the Altera web site (**www.altera.com**).

Ordering Information

Figure 7–1 describes the ordering codes for Stratix GX devices.

Figure 7–1. Stratix GX Device Packaging Ordering Information