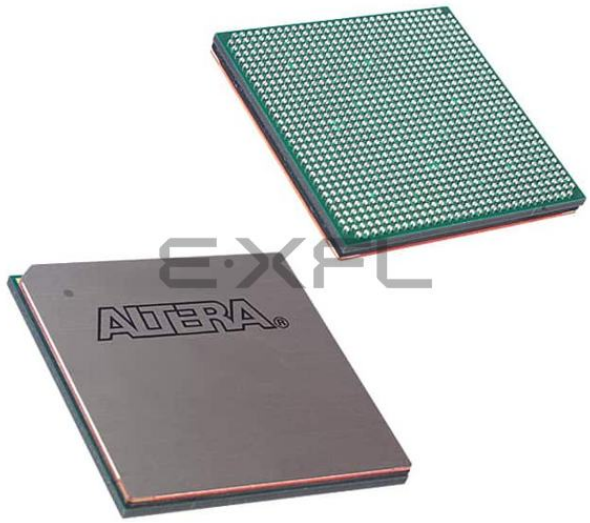


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

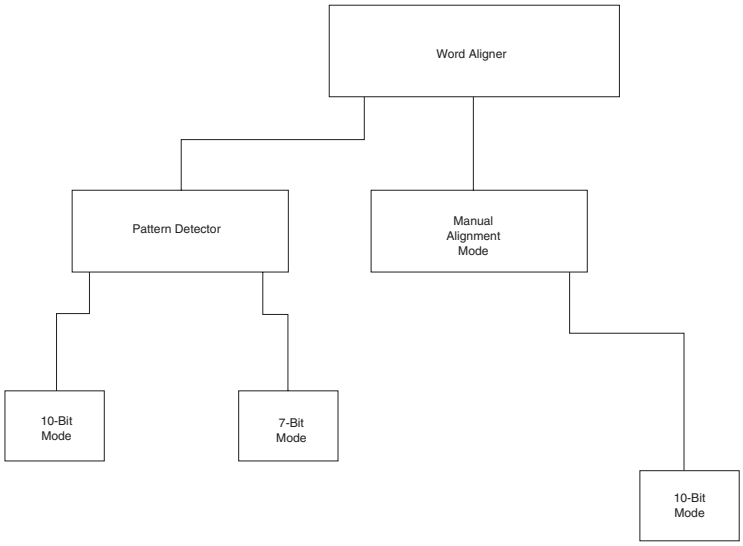
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2566 |
| Number of Logic Elements/Cells | 25660 |
| Total RAM Bits | 1944576 |
| Number of I/O | 607 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1020-BBGA |
| Supplier Device Package | 1020-FBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1sgx25ff1020c7n |

*Figure 2–17. Word Aligner in 10-Bit Mode*




In the 10-bit mode, the word aligner automatically aligns the user's predefined 10-bit alignment pattern. The pattern detector can detect the full 10-bit pattern or only the lower seven bits of the pattern. The word aligner and pattern detector detect both the positive and the negative disparity of the pattern. A user-controlled enable port is available for the word aligner.

The 10-bit mode is available only for the Custom mode.

Figure 2–18 shows the word aligner in XAUI mode.

accurately tracked by the internal bias circuit. Moreover, the reference voltage and internal resistor bias current is generated and replicated to the analog circuitry in each channel.

### Hot-Socketing Capabilities

Each Stratix GX device is capable of hot-socketing. Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Signals can be driven into Stratix GX devices before and during power-up without damaging the device. Once operating conditions are reached and the device is configured, Stratix GX devices operate according to your specifications. This feature provides the Stratix GX transceiver line card behavior, so you can insert it into the system without powering the system down, offering more flexibility.

## Applications & Protocols Supported with Stratix GX Devices

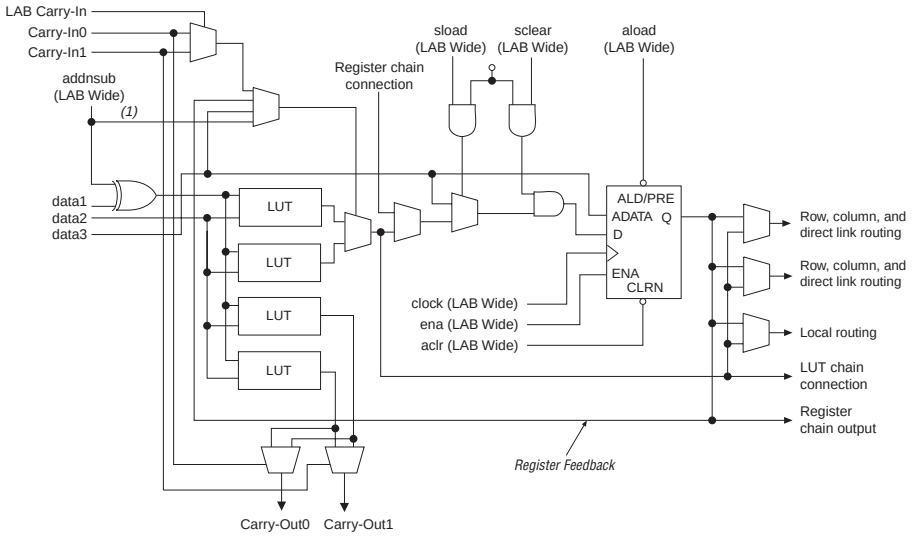
Each Stratix GX transceiver block is designed to operate at any serial bit rate from 500 Mbps to 3.1875 Gbps per channel. The wide, data rate range allows Stratix GX transceivers to support a wide variety of standard and future protocols such as 10-Gigabit Ethernet XAUI, InfiniBand, Fibre Channel, and Serial RapidIO. Stratix GX devices are ideal for many high-speed communication applications such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications standards support.

### Stratix GX Example Application Support

Stratix GX devices can be used for many applications, including:

- Backplanes for traffic management and quality of service (QOS)
- Switch fabric applications for complete set for backplane and switch fabric transceivers
- Chip-to-chip applications such as: 10 Gigabit Ethernet XAUI to XGMII bridge, 10 Gigabit Ethernet XGMII to POS-PHY4 bridge, POS-PHY4 to NPSI bridge, or NPSI to backplane bridge

*Figure 4–6. LE in Dynamic Arithmetic Mode*




*Note to Figure 4–6:*
(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

### *Carry-Select Chain*

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Because the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix GX architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 4–7 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used

*Figure 4–16. M4K RAM Block Control Signals*

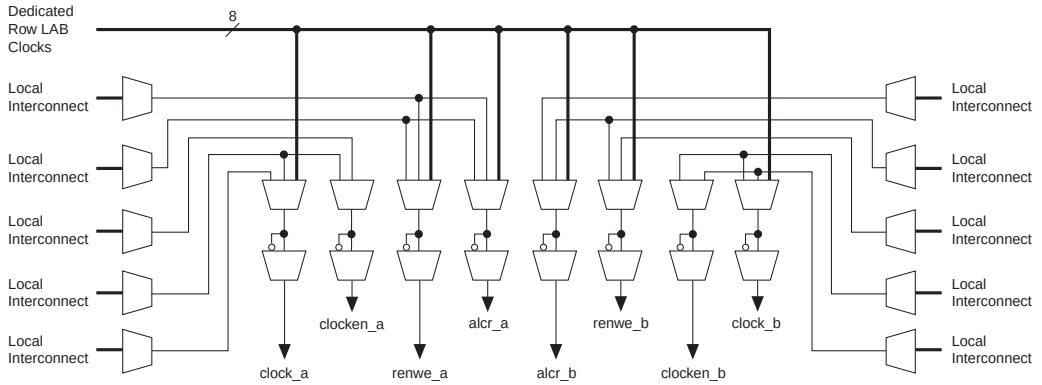



*Figure 4–17. M4K RAM Block LAB Row Interface*

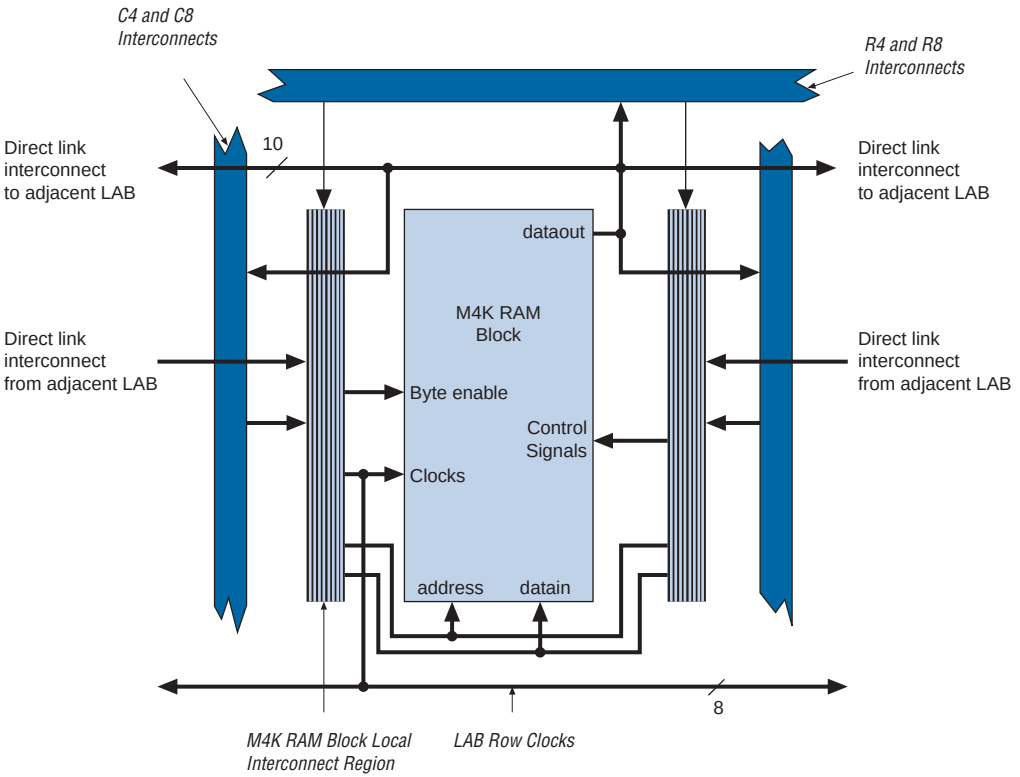
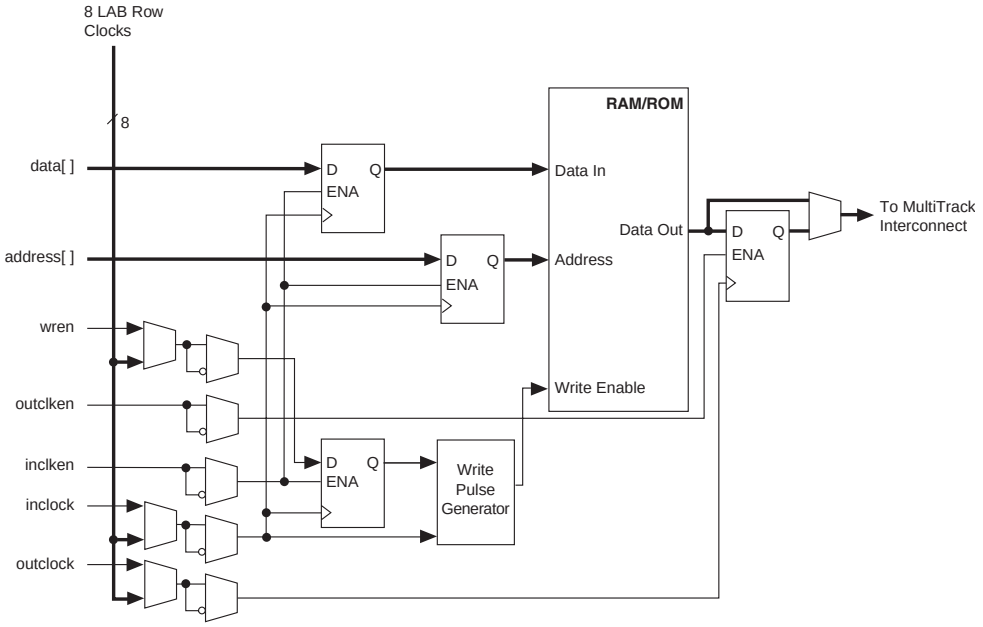


*Figure 4–27. Single-Port Mode*




# Digital Signal Processing Block

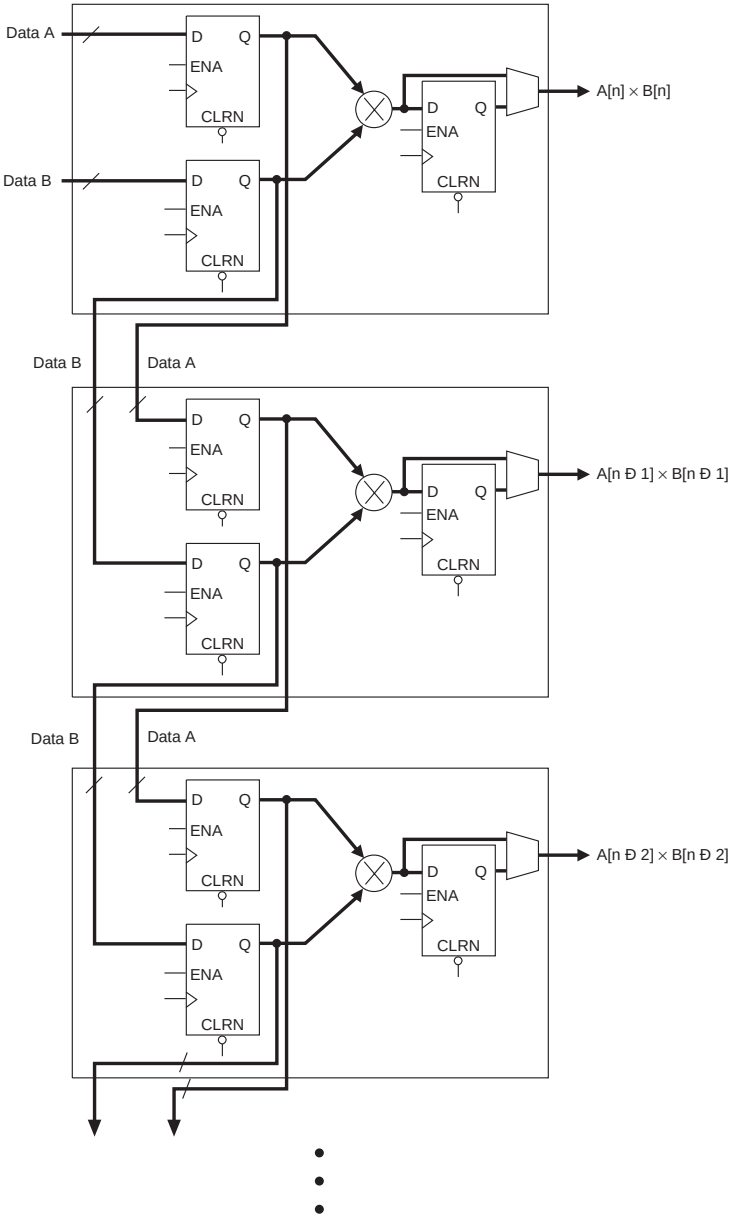
The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix GX device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix GX devices have more DSP blocks per column (see Table 4–12). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

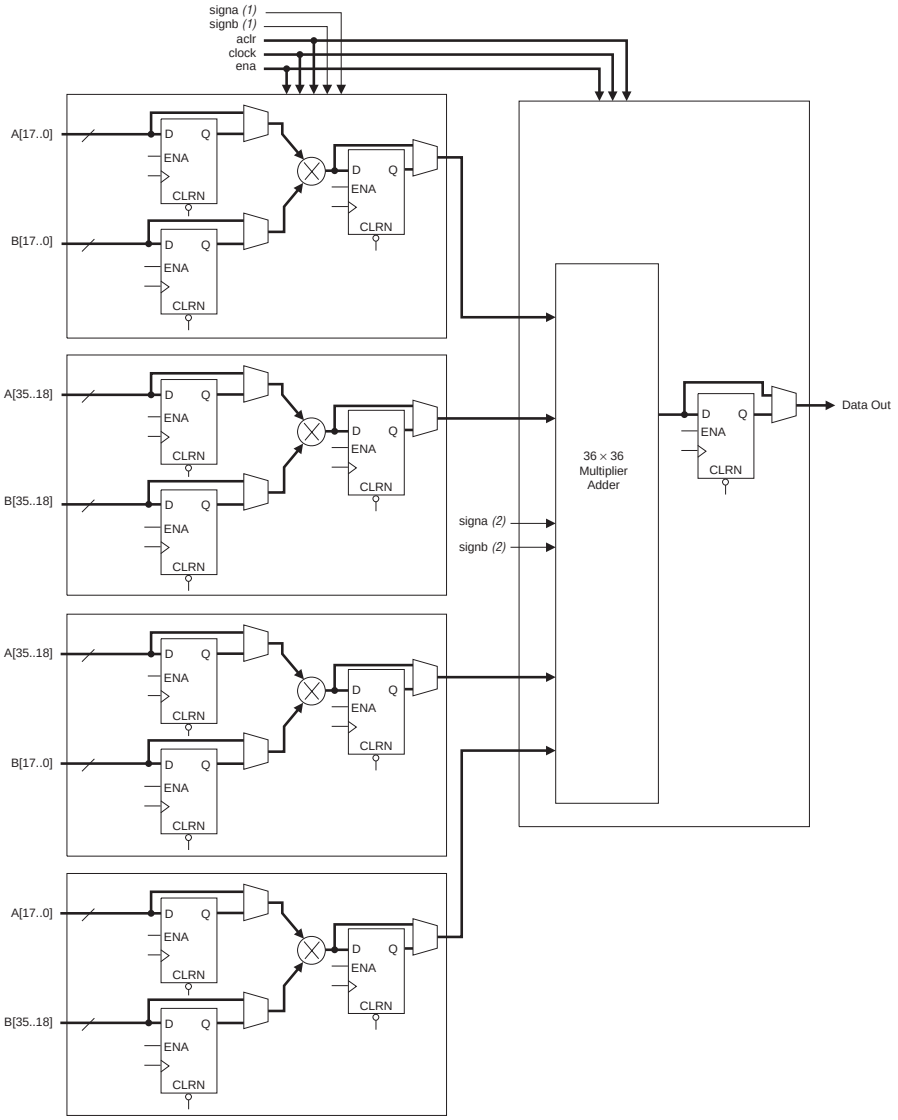
As indicated, the Stratix GX DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but

*Figure 4–32. Multiplier Sub-Blocks Using Input Shift Register Connections* *Note (1)*




*Note to Figure 4–32:*
(1) Either Data A or Data B input can be set to a parallel input for constant coefficient multiplication.

*Figure 4–35. 36 × 36 Multiply Mode*

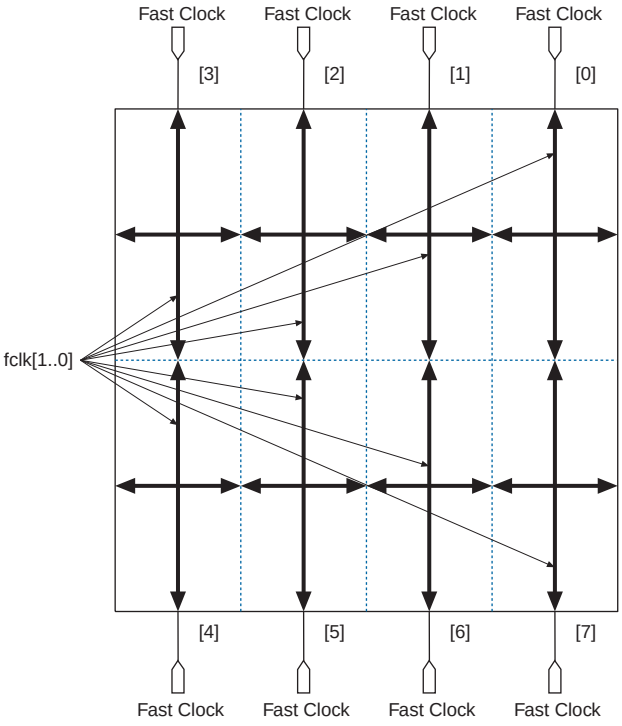



*Notes to Figure 4–35:*

(1) These signals are not registered or registered once to match the pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

*Figure 4–44. EP1SGX40 Device Fast Regional Clock Pin Connections to Fast Regional Clocks*

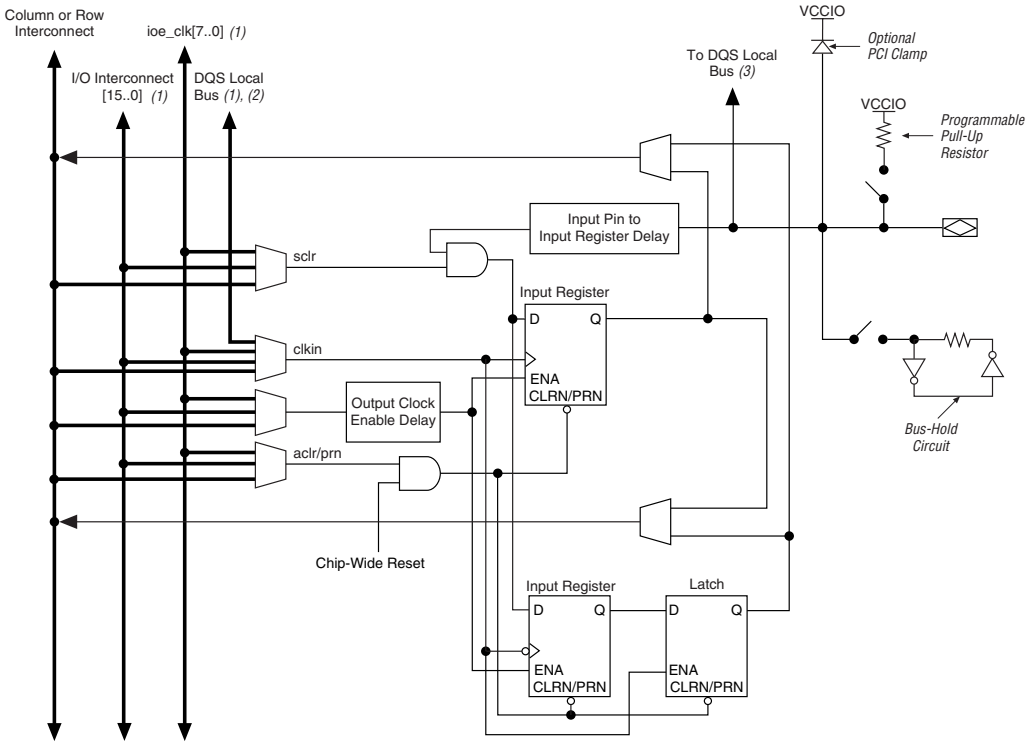



### *Combined Resources*

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, 4 regional clock lines, and 2 fast regional clock lines. Multiplexers are used with these clocks to form 8-bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer at the LAB level selects two of the eight row clocks to feed the LE registers within the LAB. See Figure 4–45.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 4–64 shows an IOE configured for DDR input. Figure 4–65 shows the DDR input timing diagram.

***Figure 4–64. Stratix GX IOE in DDR Input I/O Configuration*** *Note (1)*




*Notes to Figure 4–64:*

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.

## Slew-Rate Control

The output buffer for each Stratix GX device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

## Bus Hold

Each Stratix GX device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Table 4–25 shows bus hold support for different pin types.

*Table 4–25. Bus Hold Support*

| Pin Type | Bus Hold |
|---|---|
| I/O pins | ✓ |
| CLK[15..0] | |
| CLK[0,1,2,3,8,9,10,11] | |
| FCLK | ✓ |
| FPLL[7..10]CLK | |

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than $V_{CCIO}$ to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

*Table 4–33. Stratix GX JTAG Instructions (Part 2 of 2)*

| JTAG Instruction | Description |
|---|---|
| CLAMP *(1)* | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | Used when configuring a Stratix GX device through the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a .jam file or .jbc file with an embedded processor. |
| PULSE_NCONFIG | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO | Allows the IOE standards to be configured through the JTAG chain. Stops configuration if executed during configuration. Can be executed before or after configuration. |
| SignalTap instructions | Monitors internal device operation with the SignalTap embedded logic analyzer. |

*Note to Table 4–33:*
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Stratix GX device instruction register length is 10 bits, and the USERCODE register length is 32 bits. Tables 4–34 and 4–35 show the boundary-scan register length and IDCODE information for Stratix GX devices.

*Table 4–34. Stratix GX Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP1SGX10 | 1,029 |
| EP1SGX25 | 1,665 |
| EP1SGX40 | 1,941 |

*Table 4–35. 32-Bit Stratix GX Device IDCODE (Part 1 of 2)*

| Device | IDCODE (32 Bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) *(2)* |
| EP1SGX10 | 0000 | 0010 0000 0100 0001 | 000 0110 1110 | 1 |
| EP1SGX25 | 0000 | 0010 0000 0100 0011 | 000 0110 1110 | 1 |

# 6. DC & Switching Characteristics

SGX51006-1.2

## Operating Conditions

Stratix® GX devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 6–1 through 6–12 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and transceiver block absolute maximum ratings. Notes for Tables 6–1 through 6–6 immediately follow Table 6–6, notes for Table 6–7 immediately follow that table, and notes for Tables 6–8 through 6–12 immediately follow Table 6–12.

*Table 6–1. Stratix GX Device Absolute Maximum Ratings* *Notes (1), (2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 2.4 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | BGA packages under bias | | 135 | ° C |

*Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 1 of 2)* *Note (7), (12), (13)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)* | 1.425 | 1.575 | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4), (5)* | 3.00 (3.135) | 3.60 (3.465) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)* | 2.375 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | *(4)* | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | *(4)* | 1.4 | 1.6 | V |
| $V_I$ | Input voltage | *(3), (6)* | –0.5 | 4.1 | V |

*Table 6–7. Stratix GX Transceiver Block AC Specification (Part 4 of 7)*

| Symbol / Description | Conditions | -5 Commercial Speed Grade *(1)* | | | -6 Commercial & Industrial Speed Grade *(1)* | | | -7 Commercial & Industrial Speed Grade *(1)* | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter | f = 22.1 kHz at 3.125 Gbps | | | 8.5 | | | 8.5 | | | N/A | |
| | f = 1.875 MHz at 3.125 Gbps | | | 0.1 | | | 0.1 | | | N/A | |
| | f = 20 MHz at 3.125 Gbps | | | 0.1 | | | 0.1 | | | N/A | |
| BER *(12)* | | | | $10^{-12}$ | | | $10^{-12}$ | | | $10^{-12}$ | |
| Receive latency *(4)* | Single width | 7 | | 32 | 7 | | 32 | 7 | | 32 | *(3)* |
| | Double width | 5 | | 19 | 5 | | 19 | 5 | | 19 | *(3)* |
| Channel to channel bit skew tolerance *(5)*, *(6)* | XAUI mode / inter-quadrant only | | | 40 | | | 40 | | | N/A | UI *(7)* |
| Run-length | *(8)* | | | 80 | | | 80 | | | 80 | UI |
| Receive return loss (differential) | 100 MHz to 2.5 Ghz | | | –10 | | | –10 | | | –10 | dB |
| Receive return loss (common mode) | 100 MHz to 2.5 Ghz | | | –6 | | | –6 | | | –6 | dB |
| **Transmitter** | | | | | | | | | | | |
| Serial data rate | Commercial / industrial | 500 | | 3,187.5 | 500 | | 3,187.5 | 500 | | 2,500 | Mbps |
| Parallel transceiver/ core interface speed | | 20 | | 398.4 | 20 | | 375 | 20 | | 312.5 | MHz |
| **8B/10B Custom Transmitter Jitter using Encoded CRPAT** *Note (9)* | | | | | | | | | | | |
| Deterministic jitter | 500 Mbps Pre-emphasis = 1 $V_{OD}$ = 1,400 mV | | | 0.11 | | | 0.11 | | | 0.11 | UI |
| Total jitter | | | | 0.18 | | | 0.18 | | | 0.18 | UI |

*Table 6–35. Stratix GX Device Performance (Part 2 of 3)* *Notes (1), (2)*

| Applications | | Resources Used | | | Performance | | | |
|---|---|---|---|---|---|---|---|---|
| | | LEs | TriMatrix Memory Blocks | DSP Blocks | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | Units |
| TriMatrix memory M512 block | Simple dual-port RAM 32 × 18 bit | 0 | 1 | 0 | 317.76 | 277.62 | 241.48 | MHz |
| | FIFO 32 × 18 bit | 30 | 1 | 0 | 319.18 | 278.86 | 242.54 | MHz |
| TriMatrix memory M4K block | Simple dual-port RAM 128 × 36 bit | 0 | 1 | 0 | 290.86 | 255.55 | 222.27 | MHz |
| | True dual-port RAM 128 × 18 bit | 0 | 1 | 0 | 290.86 | 255.55 | 222.27 | MHz |
| | FIFO 128 × 36 bit | 34 | 1 | 0 | 290.86 | 255.55 | 222.27 | MHz |
| TriMatrix memory M-RAM block | Single port RAM 4K × 144 bit | 1 | 1 | 0 | 255.95 | 223.06 | 194.06 | MHz |
| | Simple dual-port RAM 4K × 144 bit | 0 | 1 | 0 | 255.95 | 233.06 | 194.06 | MHz |
| | True dual-port RAM 4K × 144 bit | 0 | 1 | 0 | 255.95 | 233.06 | 194.06 | MHz |
| | Single port RAM 8K × 72 bit | 0 | 1 | 0 | 278.94 | 243.19 | 211.59 | MHz |
| | Simple dual-port RAM 8K × 72 bit | 0 | 1 | 0 | 255.95 | 223.06 | 194.06 | MHz |
| | True dual-port RAM 8K × 72 bit | 0 | 1 | 0 | 255.95 | 223.06 | 194.06 | MHz |
| | Single port RAM 16K × 36 bit | 0 | 1 | 0 | 280.66 | 254.32 | 221.28 | MHz |
| | Simple dual-port RAM 16K × 36 bit | 0 | 1 | 0 | 269.83 | 237.69 | 206.82 | MHz |

## Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 6–36 through 6–42 describe the Stratix GX device internal timing microparameters for LEs, IOEs, TriMatrix™ memory structures, DSP blocks, and MultiTrack interconnects.

*Table 6–36. LE Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LE combinational LUT delay for data-in to data-out |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{PRE}$ | Minimum preset pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

*Table 6–37. IOE Internal Timing Microparameter Descriptions*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | IOE input and output register setup time before clock |
| $t_{H}$ | IOE input and output register hold time after clock |
| $t_{CO}$ | IOE input and output register clock-to-output delay |
| $t_{PIN2COMBOUT\_R}$ | Row input pin to IOE combinational output |
| $t_{PIN2COMBOUT\_C}$ | Column input pin to IOE combinational output |
| $t_{COMBIN2PIN\_R}$ | Row IOE data input to combinational output pin |
| $t_{COMBIN2PIN\_C}$ | Column IOE data input to combinational output pin |
| $t_{CLR}$ | Minimum clear pulse width |
| $t_{PRE}$ | Minimum preset pulse width |
| $t_{CLKHL}$ | Minimum clock high or low time |

*Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)*

| Symbol | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{OUTCO}$ | 2.000 | 5.365 | 2.000 | 5.775 | 2.000 | 6.621 | ns |
| $t_{INSUPLL}$ | 1.126 | | 1.186 | | 1.352 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 0.500 | 2.304 | 0.500 | 2.427 | 0.500 | 2.765 | ns |

## External I/O Delay Parameters

External I/O delay timing parameters, both for I/O standard input and output adders and programmable input and output delays, are specified by speed grade, independent of device density.

Tables 6–72 through 6–77 show the adder delays associated with column and row I/O pins. If an I/O standard is selected other than LVTTL 24 mA with a fast slew rate, add the selected delay to the external $t_{CO}$ and $t_{SU}$ I/O parameters.

*Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 1 of 2)*

| I/O Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | | 30 | | 31 | | 35 | ps |
| 1.8-V LVTTL | | 150 | | 157 | | 180 | ps |
| 1.5-V LVTTL | | 210 | | 220 | | 252 | ps |
| GTL | | 220 | | 231 | | 265 | ps |
| GTL+ | | 220 | | 231 | | 265 | ps |
| 3.3-V PCI | | 0 | | 0 | | 0 | ps |
| 3.3-V PCI-X 1.0 | | 0 | | 0 | | 0 | ps |
| Compact PCI | | 0 | | 0 | | 0 | ps |
| AGP 1× | | 0 | | 0 | | 0 | ps |
| AGP 2× | | 0 | | 0 | | 0 | ps |
| CTT | | 120 | | 126 | | 144 | ps |
| SSTL-3 class I | | –30 | | –32 | | –37 | ps |
| SSTL-3 class II | | –30 | | –32 | | –37 | ps |

*Table 6–74. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)*

| Standard | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| GTL+ | | –110 | | –115 | | –133 | ps |
| 3.3-V PCI | | –230 | | –241 | | –277 | ps |
| 3.3-V PCI-X 1.0 | | –230 | | –241 | | –277 | ps |
| Compact PCI | | –230 | | –241 | | –277 | ps |
| AGP 1× | | –30 | | –31 | | –36 | ps |
| AGP 2× | | –30 | | –31 | | –36 | ps |
| CTT | | 50 | | 53 | | 61 | ps |
| SSTL-3 class I | | 90 | | 95 | | 109 | ps |
| SSTL-3 class II | | –50 | | –52 | | –60 | ps |
| SSTL-2 class I | | 100 | | 105 | | 120 | ps |
| SSTL-2 class II | | 20 | | 21 | | 24 | ps |
| SSTL-18 class I | | 230 | | 242 | | 278 | ps |
| SSTL-18 class II | | 0 | | 0 | | 0 | ps |
| 1.5-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.5-V HSTL class II | | 190 | | 200 | | 230 | ps |
| 1.8-V HSTL class I | | 380 | | 399 | | 459 | ps |
| 1.8-V HSTL class II | | 390 | | 410 | | 471 | ps |

*Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)*

| Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 570 | | 599 | | 689 | ps |
| | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | 4 mA | | 570 | | 599 | | 689 | ps |
| | 8 mA | | 350 | | 368 | | 423 | ps |
| | 12 mA | | 130 | | 137 | | 157 | ps |
| | 16 mA | | 70 | | 74 | | 85 | ps |
| | 24 mA | | 0 | | 0 | | 0 | ps |

*Table 6–77. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins*

| I/O Standard | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 1,930 | | 2,031 | | 2,335 | ps |
| | 4 mA | | 1,930 | | 2,031 | | 2,335 | ps |
| | 8 mA | | 1,710 | | 1,800 | | 2,069 | ps |
| | 12 mA | | 1,490 | | 1,569 | | 1,803 | ps |
| 3.3-V LVTTL | 4 mA | | 1,953 | | 2,055 | | 2,363 | ps |
| | 8 mA | | 1,733 | | 1,824 | | 2,097 | ps |
| | 12 mA | | 1,513 | | 1,593 | | 1,831 | ps |
| | 16 mA | | 1,453 | | 1,530 | | 1,759 | ps |
| 2.5-V LVTTL | 2 mA | | 2,632 | | 2,769 | | 3,183 | ps |
| | 8 mA | | 2,052 | | 2,160 | | 2,483 | ps |
| | 12 mA | | 1,942 | | 2,044 | | 2,350 | ps |
| | 16 mA | | 1,902 | | 2,002 | | 2,301 | ps |
| 1.8-V LVTTL | 2 mA | | 4,537 | | 4,773 | | 5,489 | ps |
| | 8 mA | | 3,447 | | 3,628 | | 4,172 | ps |
| | 12 mA | | 3,377 | | 3,555 | | 4,088 | ps |
| 1.5-V LVTTL | 2 mA | | 6,575 | | 6,917 | | 7,954 | ps |
| | 4 mA | | 5,995 | | 6,308 | | 7,253 | ps |
| | 8 mA | | 5,525 | | 5,815 | | 6,686 | ps |
| CTT | | | 1,410 | | 1,485 | | 1,707 | ps |
| SSTL-3 class I | | | 1,450 | | 1,527 | | 1,755 | ps |
| SSTL-3 class II | | | 1,310 | | 1,380 | | 1,586 | ps |
| SSTL-2 class I | | | 1,797 | | 1,892 | | 2,175 | ps |
| SSTL-2 class II | | | 1,717 | | 1,808 | | 2,079 | ps |
| LVDS *(1)* | | | 1,340 | | 1,411 | | 1,622 | ps |
| LVPECL *(1)* | | | 1,400 | | 1,474 | | 1,694 | ps |
| 3.3-V PCML *(1)* | | | 1,300 | | 1,369 | | 1,573 | ps |
| HyperTransport technology *(1)* | | | 1,430 | | 1,506 | | 1,731 | ps |

*Note to Tables 6–72 through 6–77:*
(1) These parameters are only available on the left side row I/O pins.

*Table 6–87. High-Speed I/O Specifications (Part 3 of 4)* *Notes (1), (2)*

| Symbol | Conditions | | | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| DPA Lock Time | Standard | Training Pattern | Transition Density | | | | | | | | | | |
| | SPI-4, CSIX | 0000 0000 0011 1111 1111 | 10% | 256 | | | 256 | | | 256 | | | *(4)* |
| | Rapid IO | 0000 1111 | 25% | 256 | | | 256 | | | 256 | | | *(4)* |
| | | 1001 0000 | 50% | 256 | | | 256 | | | 256 | | | *(4)* |
| | Misc | 1010 1010 | 100 % | 256 | | | 256 | | | 256 | | | *(4)* |
| | | 0101 0101 | | 256 | | | 256 | | | 256 | | | *(4)* |
| TCCS | All | | | | | 200 | | | 200 | | | 300 | ps |
| SW | PCML ($J$ = 4, 7, 8, 10) | | | 750 | | | 750 | | | 800 | | | ps |
| | PCML ($J$ = 2) | | | 900 | | | 900 | | | 1,200 | | | ps |
| | PCML ($J$ = 1) | | | 1,500 | | | 1,500 | | | 1,700 | | | ps |
| | LVDS and LVPECL ($J$ = 1) | | | 500 | | | 500 | | | 550 | | | ps |
| | LVDS, LVPECL, HyperTransport technology ($J$ = 2 through 10) | | | 440 | | | 440 | | | 500 | | | ps |
| Input jitter tolerance (peak-to-peak) | All | | | | | 250 | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | | | 160 | | | 160 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | | | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | | | 110 | 170 | 200 | 110 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | | | 90 | 130 | 150 | 90 | 130 | 150 | 100 | 135 | 150 | ps |
| | PCML | | | 80 | 110 | 135 | 80 | 110 | 135 | 80 | 110 | 135 | ps |

*Table 6–92. Fast PLL Specifications for -7 & -8 Speed Grades (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DUTY}$ | Duty cycle for DFFIO 1× CLKOUT pin *(3)* | 45 | 55 | % |
| $t_{JITTER}$ | Period jitter for DIFFIO clock out *(3)* | | ±80 | ps |
| | Period jitter for internal global or regional clock | | ±100 ps for >200 MHz outclk<br>±20 mUI for <200 MHz outclk | ps or mUI |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(4)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(4)*, *(5)* | 1 | 32 | Integer |
| $t_{ARESET}$ | Minimum pulse width on areset signal | 10 | | ns |

***Notes to Tables 6–91 & 6–92:***

(1) See "Maximum Input & Output Clock Rates" on page 6–54.
(2) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (that is, the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).
(3) This parameter is for high-speed differential I/O mode only.
(4) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.
(5) High-speed differential I/O mode supports $W = 1$ to 16 and $J = 4, 7, 8,$ or 10.

## DLL Jitter

Table 6–93 reports the jitter for the DLL in the DQS phase-shift reference circuit.

*Table 6–93. DLL Jitter for DQS Phase Shift Reference Circuit*

| Frequency (MHz) | DLL Jitter (ps) |
|---|---|
| 197 to 200 | ± 100 |
| 160 to 196 | ± 300 |
| 100 to 159 | ± 500 |