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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx40df1020c5n

Transceiver Blocks

Stratix® GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

There are up to 20 transceiver channels available on a single Stratix GX device. [Table 2–1](#) shows the number of transceiver channels available on each Stratix GX device.

<i>Table 2–1. Stratix GX Transceiver Channels</i>	
Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

[Figure 2–1](#) shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GIGE applications, in addition to channel bonding for XAUI applications.

Receiver State Machine

The receiver state machine operates in GIGE and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with 9'h1FE. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group. [Table 2–8](#) shows the code conversion. The conversion adheres to the IEEE 802.3ae specification.

Table 2–8. Code Conversion

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal Data
1	07	K28.0 or K28.3 or K28.5	Idle in I
1	07	K28.5	Idle in T
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code group	Invalid XGMII character
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups

Byte Deserializer

The byte deserializer takes a single width word (8 or 10 bits) from the transceiver logic and converts it into double-width words (16 or 20 bits) to the phase compensation FIFO buffer. The byte deserializer is bypassed when single width mode (8 or 10 bits) is used at the PLD interface.

Phase Compensation FIFO Buffer

The receiver phase compensation FIFO buffer resides in the transceiver block at the programmable logic device (PLD) boundary. This buffer compensates for the phase difference between the recovered clock within the transceiver and the recovered clock after it has transferred to the PLD core. The phase compensation FIFO buffer is four words deep and cannot be bypassed.

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not use in the loopback path. The received data is not retimed. [Figure 2–22](#) shows the data path in parallel loopback mode. This option is not dynamically switchable. Reception of an external signal is not possible in this mode.

The reverse serial loopback exercises the analog portion of the transceiver. This loopback mode is dynamically switchable through the `tx_srlpbk` port on a channel by channel basis. Asserting `rxanalogreset` in reverse serial loopback mode powers down the receiver buffer and CRU, preventing data loopback. [Figure 2-23](#) shows the data path in reverse serial loopback mode.

Introduction

Expansion in the telecommunications market and growth in Internet use requires systems to move more data faster than ever. To meet this demand, rely on solutions such as differential signaling and emerging high-speed interface standards including RapidIO, POS-PHY 4, SFI-4, or XSBI.

These new protocols support differential data rates up to 1 Gbps and higher. At these high data rates, it becomes more challenging to manage the skew between the clock and data signals. One solution to this challenge is to use CDR to eliminate skew between data channels and clock signals. Another potential solution, DPA, is beginning to be incorporated into some of these protocols.

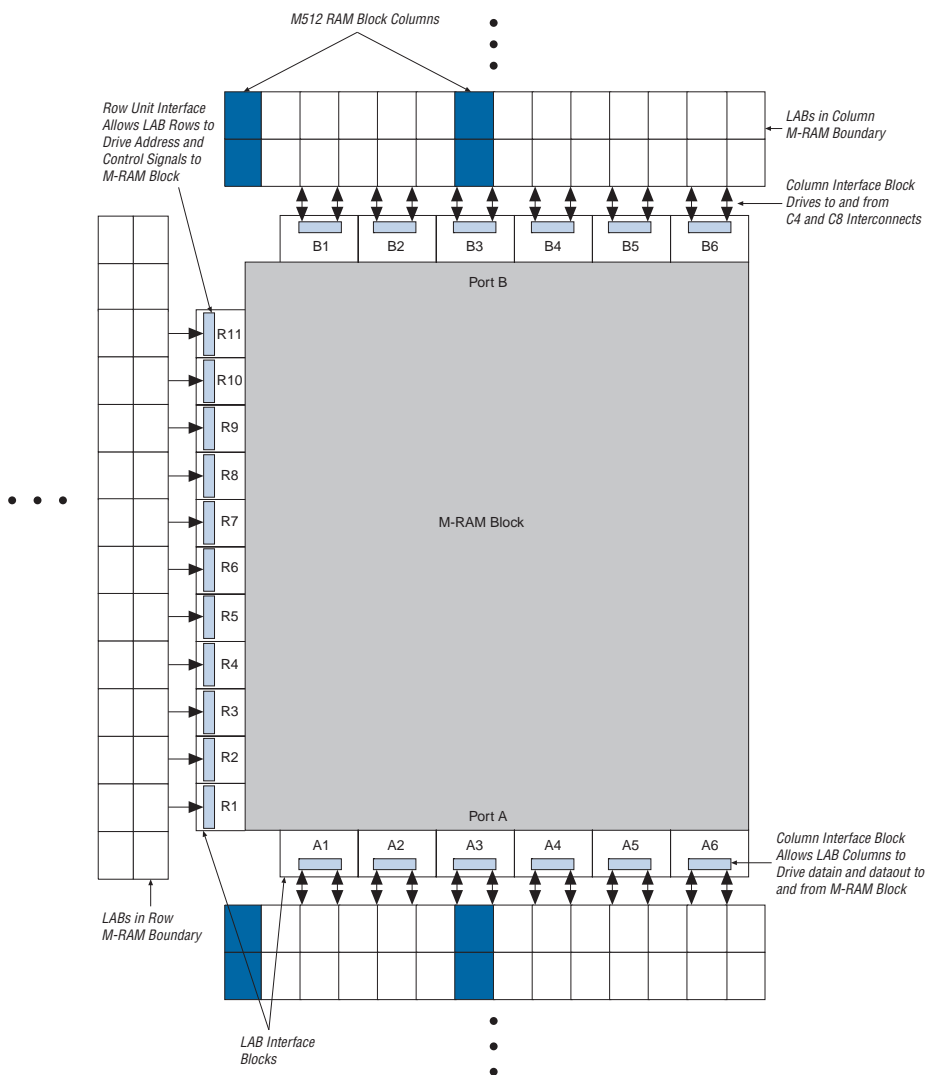
The source-synchronous high-speed interface in Stratix GX devices is a dedicated circuit embedded into the PLD allowing for high-speed communications. The *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2* provides information on the high-speed I/O standard features and functions of the Stratix GX device.

Stratix GX I/O Banks

Stratix GX devices contain 17 I/O banks. I/O banks one and two support high-speed LVDS, LVPECL, and 3.3-V PCML inputs and outputs. These two banks also incorporate an embedded dynamic phase aligner within the source-synchronous interface (see [Figure 3-8 on page 3-10](#)). The dynamic phase aligner corrects for the phase difference between the clock and data lines caused by skew. The dynamic phase aligner operates automatically and continuously without requiring a fixed training pattern, and allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-clock skew.

Principles of SERDES Operation

Stratix GX devices support source-synchronous differential signaling up to 1 Gbps in DPA mode, and up to 840 Mbps in non-DPA mode. Serial data is transmitted and received along with a low-frequency clock. The PLL can multiply the incoming low-frequency clock by a factor of 1 to 10. The SERDES factor J can be 8 or 10 for the DPA mode, or 4, 7, 8, or 10 for all other modes. The SERDES factor does not have to equal the clock

Figure 4–20. Left-Facing M-RAM to Interconnect Interface *Notes (1), (2)***Notes to Figure 4–20:**

- (1) Only R24 and C16 interconnects cross the M-RAM block boundaries.
- (2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. [Figures 4–24](#) and [4–25](#) show the memory block in input/output clock mode.

clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in [Table 4–16](#).

Table 4–16. DSP Block Signal Sources & Destinations			
LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
1	signa	A1 [17..0]	OA [17..0]
2	aclr0 accum_sload0	B1 [17..0]	OB [17..0]
3	addnsb1 clock0 ena0	A2 [17..0]	OC [17..0]
4	aclr1 clock1 ena1	B2 [17..0]	OD [17..0]
5	aclr2 clock2 ena2	A3 [17..0]	OE [17..0]
6	sign_b clock3 ena3	B3 [17..0]	OF [17..0]
7	clear3 accum_sload1	A4 [17..0]	OG [17..0]
8	addnsb3	B4 [17..0]	OH [17..0]

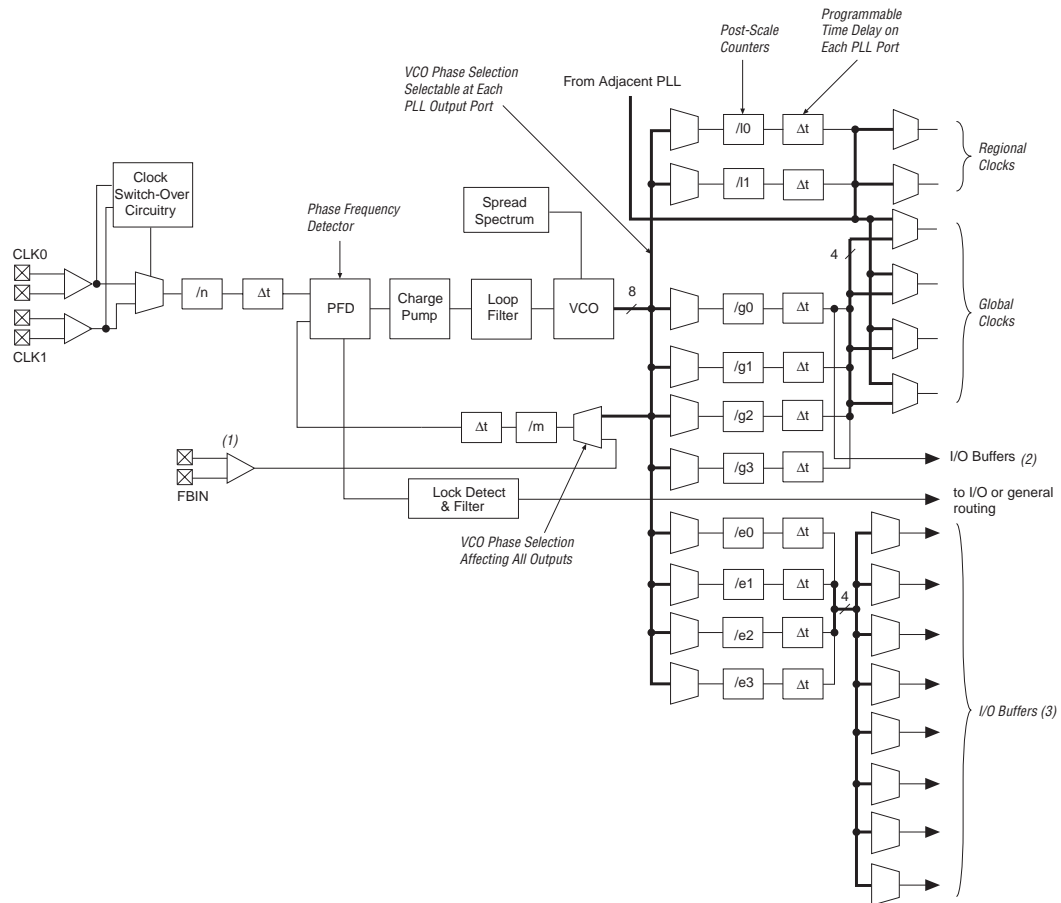
PLLs & Clock Networks

Stratix GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution. Stratix GX devices contain up to four enhanced PLLs and up to four fast PLLs. In addition, there are four receiver PLLs and one transmitter PLL per transceiver block located on the right side of Stratix GX devices.

Global & Hierarchical Clocking

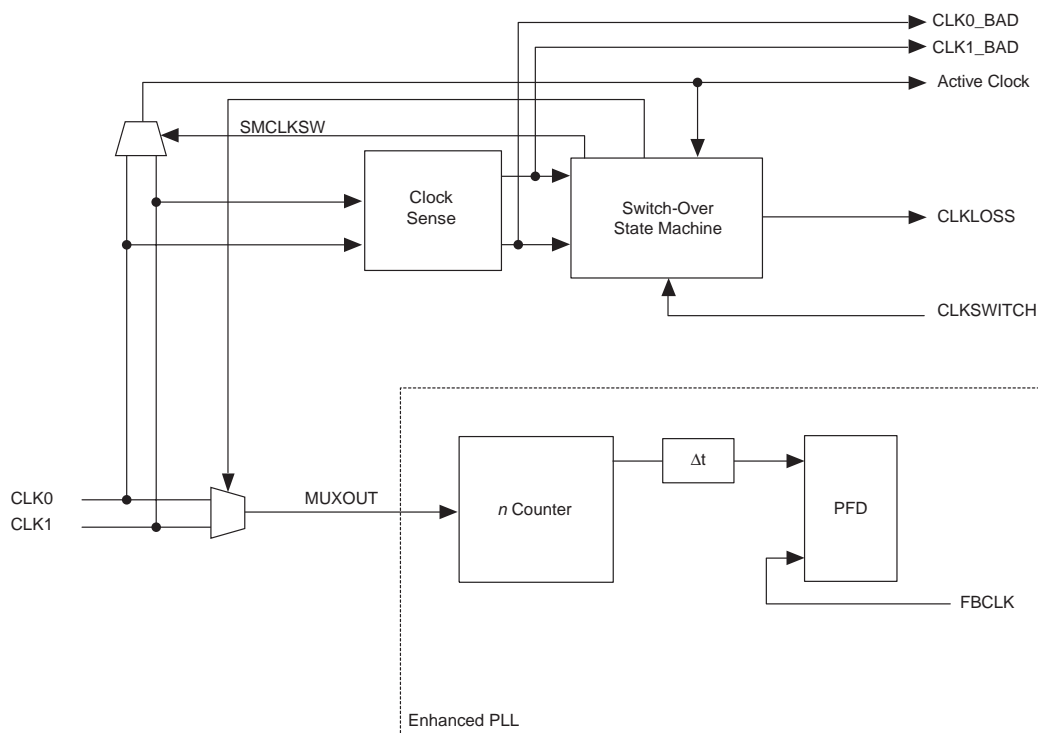
Stratix GX devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), 8 dedicated fast regional clock networks within EP1SGX10 and EP1SGX25, and 16 dedicated fast regional clock networks within EP1SGX40 devices.

Stratix GX devices contain up to four enhanced PLLs with advanced clock management features. [Figure 4-51](#) shows a diagram of the enhanced PLL.



Notes to Figure 4-51:

- (1) External feedback is available in PLLs 5 and 6.
- (2) This external output is available from the g0 counter for PLLs 11 and 12.
- (3) These counters and external outputs are available in PLLs 5 and 6.

Figure 4–52. Clock Switchover Circuitry

Note to Figure 4–52:

(1) PFD: phase frequency detector.

There are two possible ways to use the clock switchover feature.

- You can use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 4–52. In this case, the secondary clock becomes the reference clock for the PLL.
- You can use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than $\pm 20\%$. This feature is useful when clock sources can originate from multiple cards on the backplane,

The `areset` signals are reset/resynchronization inputs for each PLL. The `areset` signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the `areset` signal in designs if any of the following conditions are true:

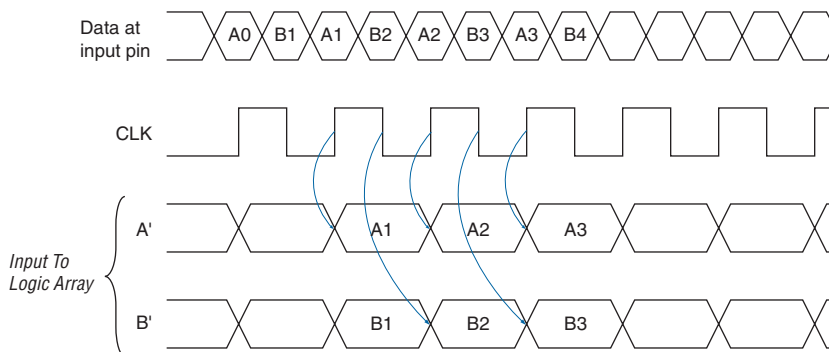
- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters resets, clearing the PLL output and placing the PLL out of lock. The VCO sets back to its nominal setting (~700 MHz). When driven low again, the PLL resynchronizes to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency starts at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a `clkloss` status signal to trigger `pfdena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the `g` and `l` counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. [Figure 4-56](#) shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The `extclkena` signals work in the same way as the `clkena` signals, but they control the external clock output counters (`e0`, `e1`, `e2`, and `e3`). Upon re-enabling, the PLL does not need a resynchronization or relock period

Figure 4–65. Input Timing Diagram in DDR Mode

When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a $\times 2$ rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. [Figure 4–66](#) shows the IOE configured for DDR output. [Figure 4–67](#) shows the DDR output timing diagram.

Table 4–33. Stratix GX JTAG Instructions (Part 2 of 2)

JTAG Instruction	Description
CLAMP (1)	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring a Stratix GX device through the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a .jam file or .jbc file with an embedded processor.
PULSE_NCONFIG	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	Allows the IOE standards to be configured through the JTAG chain. Stops configuration if executed during configuration. Can be executed before or after configuration.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 4–33:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Stratix GX device instruction register length is 10 bits, and the USERCODE register length is 32 bits. Tables 4–34 and 4–35 show the boundary-scan register length and IDCODE information for Stratix GX devices.

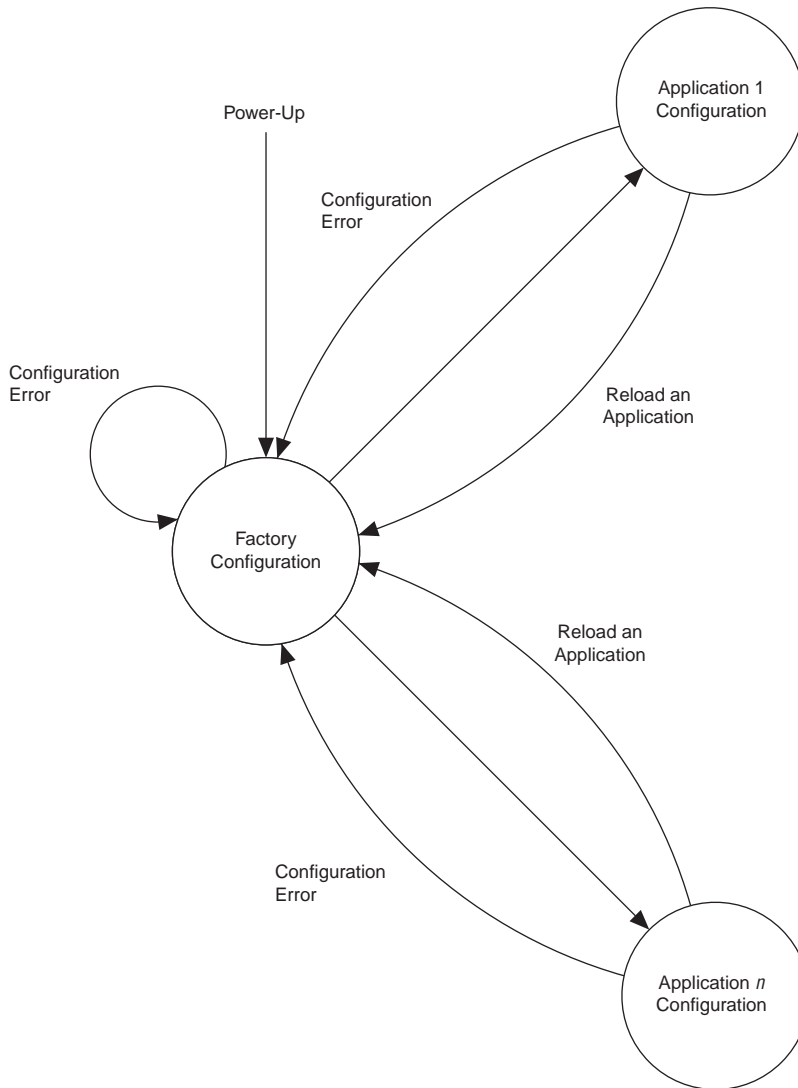
Table 4–34. Stratix GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1SGX10	1,029
EP1SGX25	1,665
EP1SGX40	1,941

Table 4–35. 32-Bit Stratix GX Device IDCODE (Part 1 of 2)

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP1SGX10	0000	0010 0000 0100 0001	000 0110 1110	1
EP1SGX25	0000	0010 0000 0100 0011	000 0110 1110	1

Figure 5–2. Remote Update Transition Diagram *Notes (1), (2)*



Notes to Figure 5–2:

- (1) Remote update of application configuration is controlled by a Nios embedded processor or user logic programmed in the factory or application configurations.
- (2) Up to seven pages can be specified allowing up to seven different configuration applications.

You can implement the error detection CRC feature with existing circuitry in Stratix GX devices, eliminating the need for external logic. For Stratix GX devices, the CRC is computed by Quartus II and downloaded into the device as a part of the configuration bit stream. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix GX devices to perform error detection automatically. This error detection circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Temperature-Sensing Diode

Stratix GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix GX device to connect to the external temperature-sensing device, as shown in [Figure 5-4](#). The temperature-sensing diode is a passive element and therefore can be used before the Stratix GX device is powered.

Figure 5–5. Temperature Versus Temperature-Sensing Diode Voltage

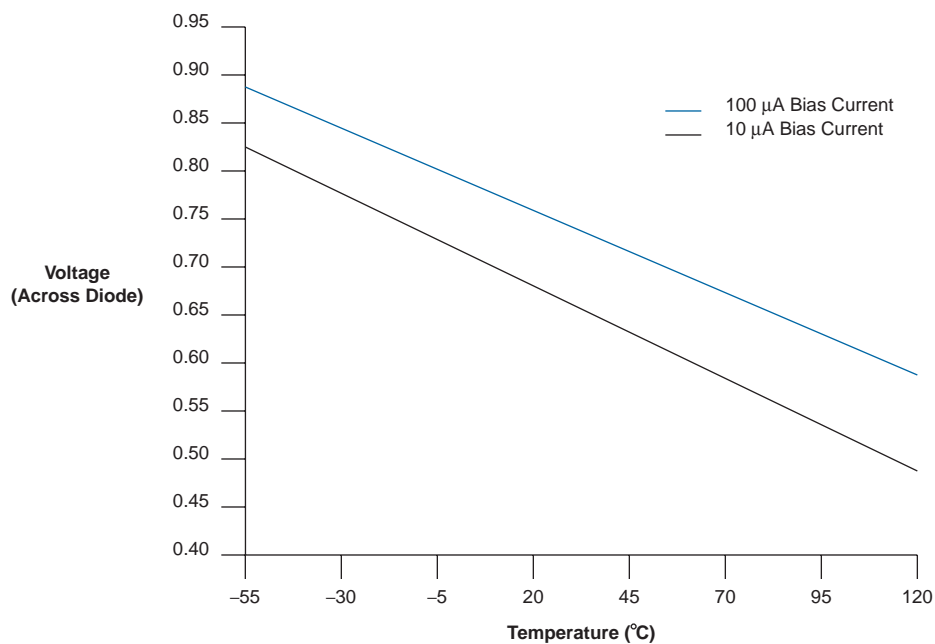


Table 6–32. CTT I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$			$V_{REF} - 0.4$	V
I_O	Output leakage current (when output is high Z)	$GND \leq V_{OUT} \leq V_{CCIO}$	-10		10	μA

Table 6–33. Bus Hold Parameters

Parameter	Conditions	V _{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V _{IN} > V _{IL} (maximum)	25		30		50		70		μA
High sustaining current	V _{IN} < V _{IH} (minimum)	−25		−30		−50		−70		μA
Low overdrive current	0 V < V _{IN} < V _{CCIO}		160		200		300		500	μA
High overdrive current	0 V < V _{IN} < V _{CCIO}		−160		−200		−300		−500	μA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Tables 6–14 through 6–33:

- (1) Drive strength is programmable according to values in the *Stratix GX Architecture* chapter of the *Stratix GX Device Handbook, Volume 1*.
- (2) V_{REF} specifies the center point of the switching range.

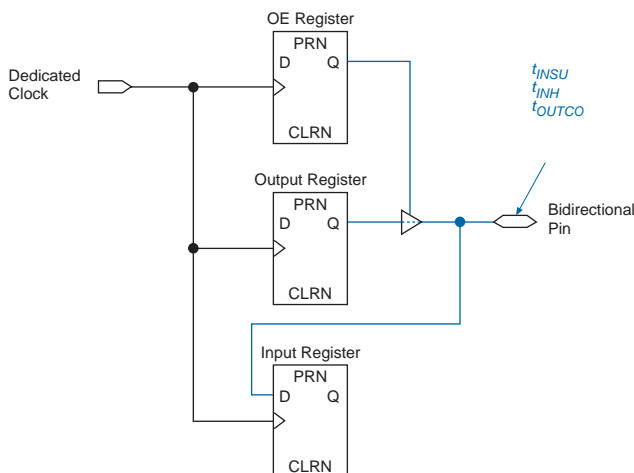
Power Consumption

Detailed power consumption information for Stratix GX devices will be released when available.

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Figure 6–6. External Timing in Stratix GX Devices

All external I/O timing parameters shown are for 3.3-V LVTTTL or LVCMOS I/O standards with the maximum current strength. For external I/O timing using standards other than LVTTTL or LVCMOS use the I/O standard input and output delay adders in [Tables 6–72 through 6–76](#).

[Table 6–51](#) shows the external I/O timing parameters when using fast regional clock networks.

Table 6–51. Stratix GX Fast Regional Clock External I/O Timing Parameters <i>Notes (1), (2)</i>		
Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with fast regional clock fed by FCLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with fast regional clock fed by FCLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with fast regional clock fed by FCLK pin	$C_{LOAD} = 10 \text{ pF}$

Notes to [Table 6–51](#):

- (1) These timing parameters are sample-tested only.
- (2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device and speed grade and whether it is t_{CO} or t_{SU} . You should use the Quartus II software to verify the external timing for any pin.

Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OUTCO}	2.000	5.365	2.000	5.775	2.000	6.621	ns
t_{INSUPLL}	1.126		1.186		1.352		ns
t_{INHPLL}	0.000		0.000		0.000		ns
t_{OUTCOPLL}	0.500	2.304	0.500	2.427	0.500	2.765	ns

External I/O Delay Parameters

External I/O delay timing parameters, both for I/O standard input and output adders and programmable input and output delays, are specified by speed grade, independent of device density.

Tables 6–72 through 6–77 show the adder delays associated with column and row I/O pins. If an I/O standard is selected other than LVTTTL 24 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters.

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVC MOS		0		0		0	ps
3.3-V LVTTTL		0		0		0	ps
2.5-V LVTTTL		30		31		35	ps
1.8-V LVTTTL		150		157		180	ps
1.5-V LVTTTL		210		220		252	ps
GTL		220		231		265	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		120		126		144	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps

Table 6–82. Stratix GX Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[8..7]CLK Pins

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	422	422	390	MHz
2.5 V	422	422	390	MHz
1.8 V	422	422	390	MHz
1.5 V	422	422	390	MHz
LVC MOS	422	422	390	MHz
GTL	300	250	200	MHz
GTL+	300	250	200	MHz
SSTL-3 class I	400	350	300	MHz
SSTL-3 class II	400	350	300	MHz
SSTL-2 class I	400	350	300	MHz
SSTL-2 class II	400	350	300	MHz
SSTL-18 class I	400	350	300	MHz
SSTL-18 class II	400	350	300	MHz
1.5-V HSTL class I	400	350	300	MHz
1.5-V HSTL class II	400	350	300	MHz
1.8-V HSTL class I	400	350	300	MHz
1.8-V HSTL class II	400	350	300	MHz
3.3-V PCI	422	422	390	MHz
3.3-V PCI-X 1.0	422	422	390	MHz
Compact PCI	422	422	390	MHz
AGP 1×	422	422	390	MHz
AGP 2×	422	422	390	MHz
CTT	300	250	200	MHz
Differential HSTL	400	350	300	MHz
LVDS	717	717	640	MHz
LVPECL	717	717	640	MHz
PCML	400	375	350	MHz
HyperTransport technology	717	717	640	MHz

Table 6–83. Stratix GX Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	422	422	390	MHz
2.5 V	422	422	390	MHz

Table 6–90. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{FCOMP}	External feedback clock compensation time (3)			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		420	MHz
$f_{\text{OUT_EXT}}$	Output frequency for external clock (2)	0.3		434	MHz
t_{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output (5)			± 100 ps for >200 MHz outclk ± 20 mUI for <200 MHz outclk	ps or mUI
$t_{\text{CONFIG5,6}}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/t_{\text{SCANCLK}}$	
$t_{\text{CONFIG11,12}}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/t_{\text{SCANCLK}}$	
t_{SCANCLK}	scanclk frequency (4)			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) (6) (10)	(8)		100	μs
t_{LOCK}	Time required to lock from end of device configuration (10)	10		400	μs
f_{VCO}	PLL internal VCO operating range	300		600 (7)	MHz