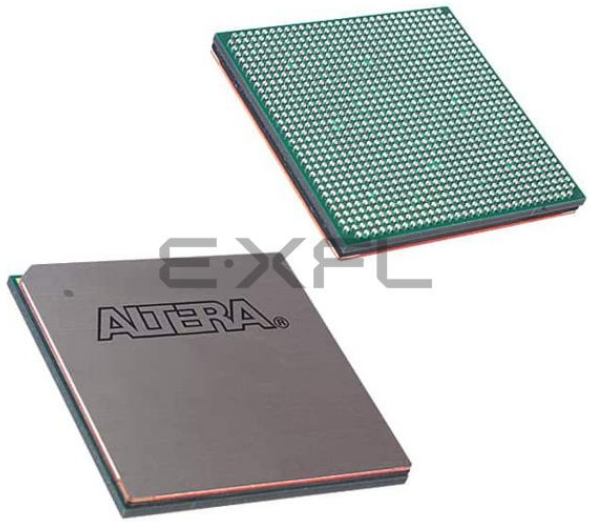

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx40df1020c6n

Table 1–1. Stratix GX Device Features

Feature	EP1SGX10C EP1SGX10D	EP1SGX25C EP1SGX25D EP1SGX25F	EP1SGX40D EP1SGX40G
LEs	10,570	25,660	41,250
Transceiver channels	4, 8	4, 8, 16	8, 20
Source-synchronous channels	22	39	45
M512 RAM blocks (32 × 18 bits)	94	224	384
M4K RAM blocks (128 × 36 bits)	60	138	183
M-RAM blocks (4K ×144 bits)	1	2	4
Total RAM bits	920,448	1,944,576	3,423,744
Digital signal processing (DSP) blocks	6	10	14
Embedded multipliers *(1)*	48	80	112
PLLs	4	4	8

Note to Table 1–1:

(1) This parameter lists the total number of 9- × 9-bit multipliers for each device. For the total number of 18- × 18-bit multipliers per device, divide the total number of 9- × 9-bit multipliers by 2. For the total number of 36- × 36-bit multipliers per device, decide the total number of 9- × 9-bit multipliers by 8.

Stratix GX devices are available in space-saving FineLine BGA® packages (refer to Tables 1–2 and 1–3), and in multiple speed grades (refer to Table 1–4). Stratix GX devices support vertical migration within the same package (that is, you can migrate between the EP1SGX10C and EP1SGX25C devices in the 672-pin FineLine BGA package). See the Stratix GX device pin tables for more information. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type, to identify which I/O pins it is possible to migrate. The Quartus II software can automatically cross reference and place all pins for migration when given a device migration list.

Table 1–2. Stratix GX Package Options & I/O Pin Counts (Part 1 of 2) *Note (1)*

Device	672-Pin FineLine BGA	1,020-Pin FineLine BGA
EP1SGX10C	362	
EP1SGX10D	362	
EP1SGX25C	455	

Each Stratix GX transceiver channel consists of a transmitter and receiver. The transmitter contains the following:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

The receiver contains the following:

- Input buffer
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

You can set all the Stratix GX transceiver functions through the Quartus II software. You can set programmable pre-emphasis, programmable equalizer, and programmable V_{OD} dynamically as well. Each Stratix GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. Figure 2–2 shows the block diagram for the Stratix GX transceiver channel.

Stratix GX transceivers provide physical coding sublayer (PCS) and physical media attachment (PMA) implementation for protocols such as 10-gigabit XAUI and GIGE. The PCS portion of the transceiver consists of the logic array interface, 8B/10B encoder/decoder, pattern detector, word aligner, rate matcher, channel aligner, and the BIST and pseudo-random binary sequence pattern generator/verifier. The PMA portion of the transceiver consists of the serializer/deserializer, the CRU, and the I/O buffers.

Figure 2–30. EP1SGX40 Receiver PLL Recovered Clock to Regional Clock Connection

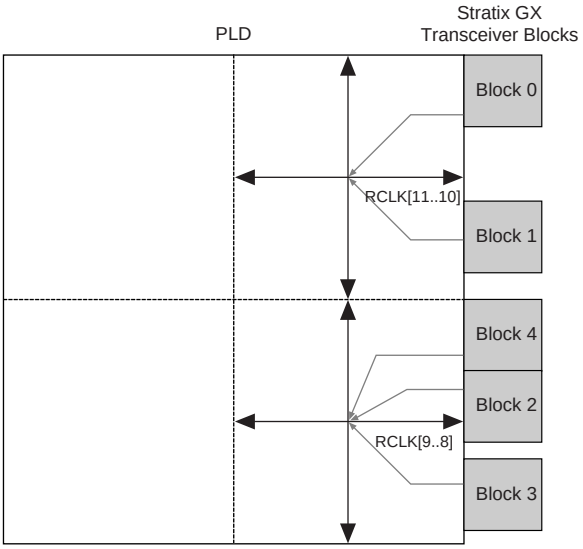


Figure 2–31 shows the possible recovered clock connection to the fast regional clock resource. The fast regional clocks can drive logic in their associated regions.

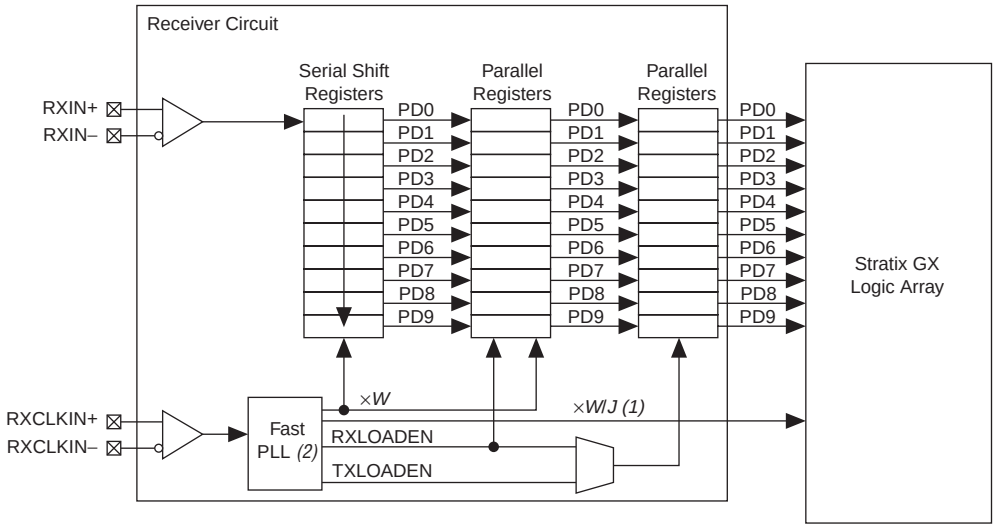
High-Speed Serial Bus Protocols

With wide, serial data rate range, Stratix GX devices can support multiple, high-speed serial bus protocols. Table 2–12 shows some of the protocols that Stratix GX devices can support.

Table 2–12. High-Speed Serial Bus Protocols

Bus Transfer Protocol	Stratix GX (Gbps) (Supports up to 3.1875 Gbps)
SONET backplane	2.488
10 Gigabit Ethernet XAUI	3.125
10 Gigabit fibre channel	3.1875
InfiniBand	2.5
Fibre channel (1G, 2G)	1.0625, 2.125
Serial RapidIO™	1.25, 2.5, 3.125
PCI Express	2.5
SMPTE 292M	1.485

Figure 3–1. Stratix GX High-Speed Interface Deserialized in ×10 Mode

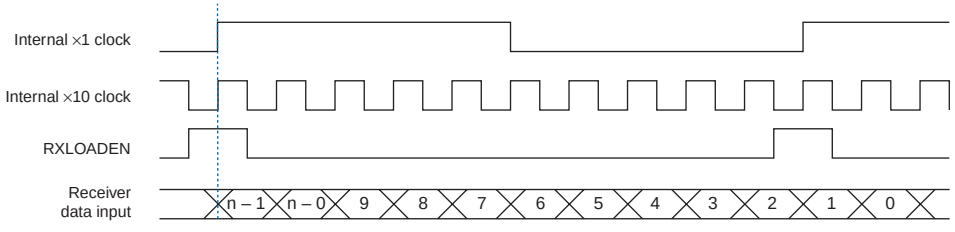


Notes to Figure 3–1:

(1) W = 1, 2, 4, 7, 8, or 10.
J = 4, 7, 8, or 10 for non-DPA (J = 8 or 10 for DPA).
W does not have to equal J. When J = 1 or 2, the deserializer is bypassed. When J = 2, the device uses DDRIO registers.

(2) This figure does not show additional circuitry for clock or data manipulation.

Figure 3–2. Receiver Timing Diagram



Stratix GX Differential I/O Transmitter Operation

You can configure any of the Stratix GX differential output channels as a transmitter channel. The differential transmitter serializes outbound parallel data.

for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain to use for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix™ memory and DSP blocks. A carry chain can continue as far as a full column.

single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix GX devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 512 × 1, 256 × 2, 128 × 4, 64 × 8 (64 × 9 bits with parity), and 32 × 16 (32 × 18 bits with parity). Mixed-width configurations are also possible, allowing different read and write widths. Table 4–3 summarizes the possible M512 RAM block configurations.

Table 4–3. M512 RAM Block Configurations (Simple Dual-Port RAM)

Read Port	Write Port						
	512 × 1	256 × 2	128 × 4	64 × 8	32 × 16	64 × 9	32 × 18
512 × 1	✓	✓	✓	✓	✓		
256 × 2	✓	✓	✓	✓	✓		
128 × 4	✓	✓	✓		✓		
64 × 8	✓	✓		✓			
32 × 16	✓	✓	✓		✓		
64 × 9						✓	
32 × 18							✓

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 4–96 for details on dedicated SERDES in Stratix GX devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, `inclr`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 4–14 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix GX devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 4–15 shows the M512 RAM block to logic array interface.

Figure 4–14. M512 RAM Block Control Signals

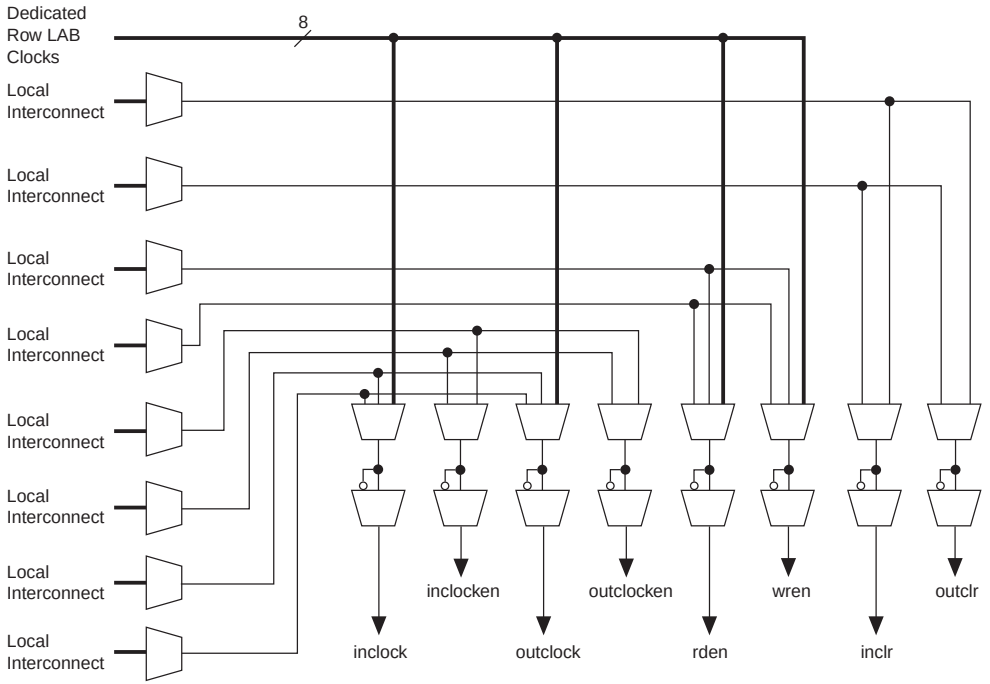
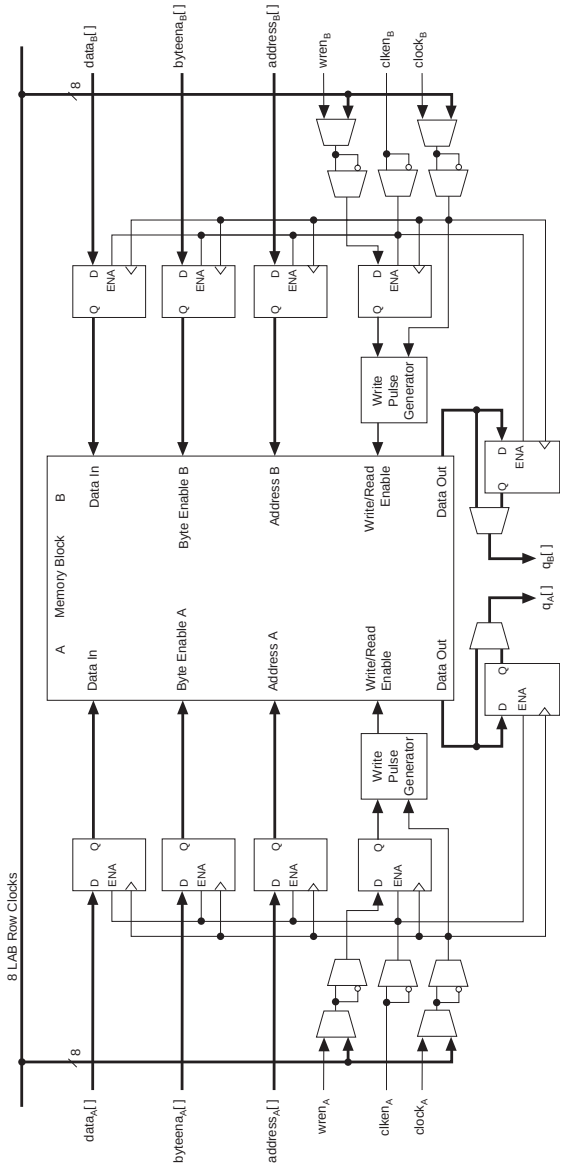
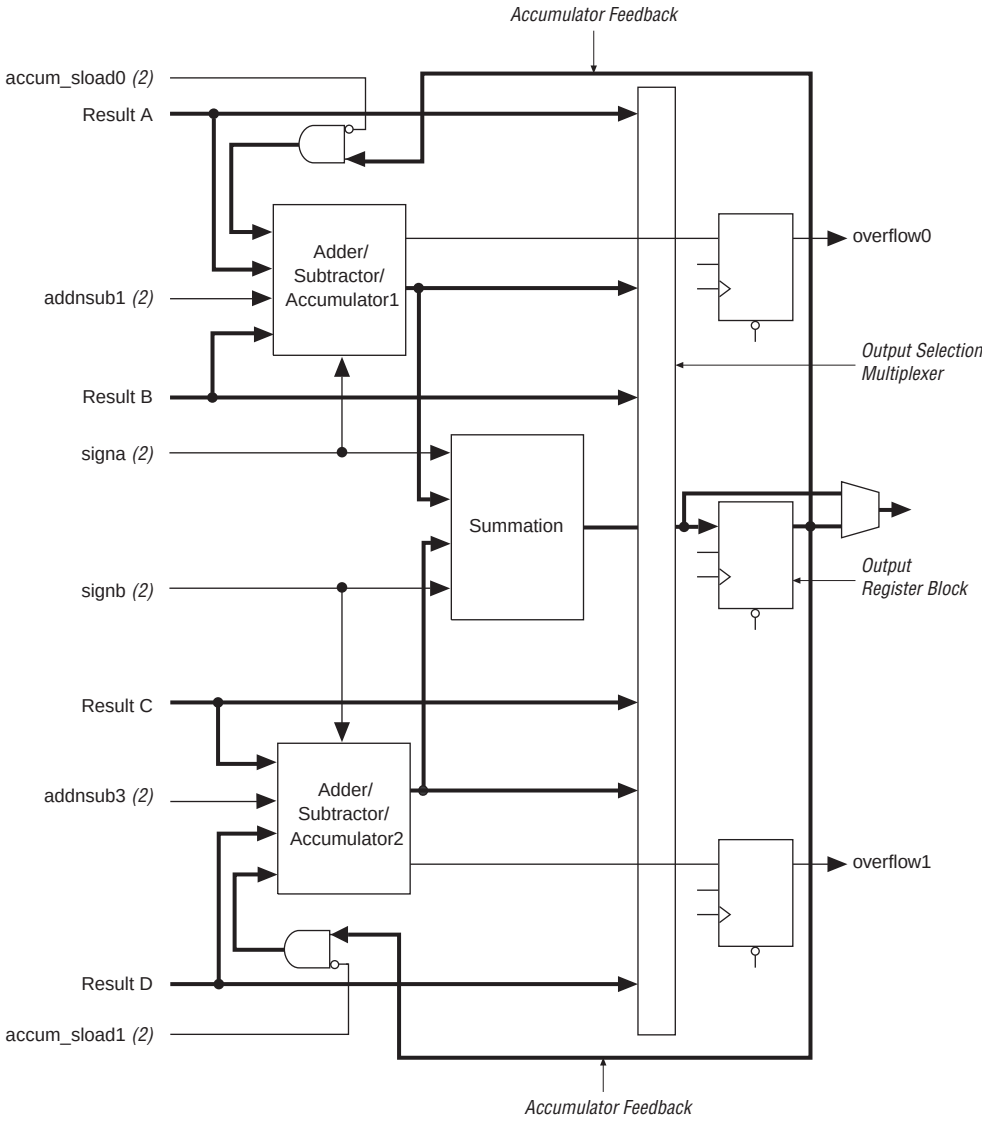


Figure 4–23. Independent Clock Mode *Note (1)*



Note to Figure 4–23:
(1) All registers shown have asynchronous clear ports.

Figure 4–33. Adder/Output Blocks *Note (1)*



Notes to Figure 4–33:

(1) Adder/output block shown in Figure 4–33 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 4–16.

Table 4–16. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
1	signa	A1[17..0]	OA[17..0]
2	aclr0 accum_sload0	B1[17..0]	OB[17..0]
3	addnsub1 clock0 ena0	A2[17..0]	OC[17..0]
4	aclr1 clock1 ena1	B2[17..0]	OD[17..0]
5	aclr2 clock2 ena2	A3[17..0]	OE[17..0]
6	sign_b clock3 ena3	B3[17..0]	OF[17..0]
7	clear3 accum_sload1	A4[17..0]	OG[17..0]
8	addnsub3	B4[17..0]	OH[17..0]

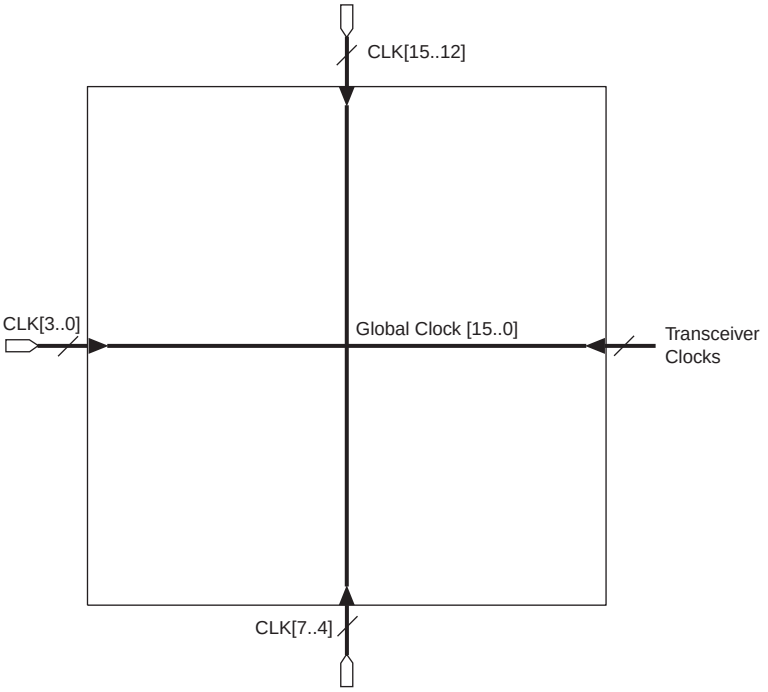
PLLs & Clock Networks

Stratix GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution. Stratix GX devices contain up to four enhanced PLLs and up to four fast PLLs. In addition, there are four receiver PLLs and one transmitter PLL per transceiver block located on the right side of Stratix GX devices.

Global & Hierarchical Clocking

Stratix GX devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), 8 dedicated fast regional clock networks within EP1SGX10 and EP1SGX25, and 16 dedicated fast regional clock networks within EP1SGX40 devices.

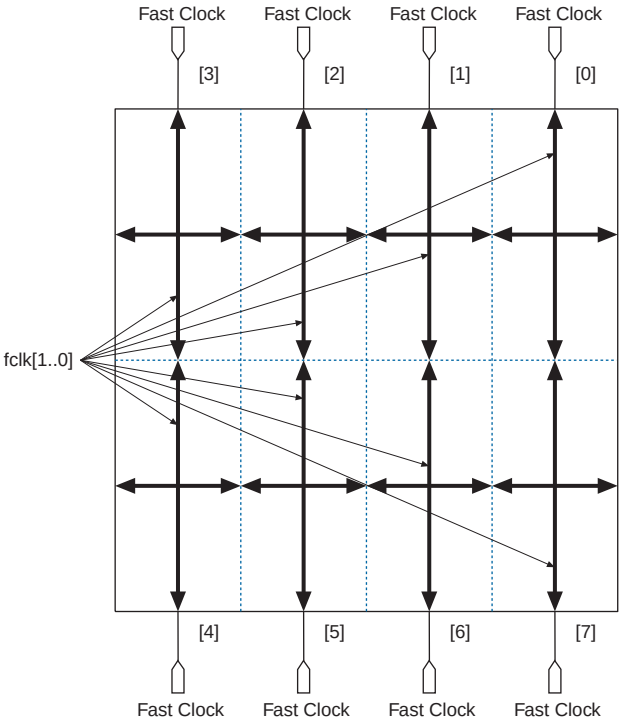
Figure 4–41. Global Clock Resources



Regional Clock Network

There are four regional clock networks RCLK[3..0] within each quadrant of the Stratix GX device that are driven by the same dedicated CLK[7..0] and CLK[15..12] input pins, PLL outputs, or transceiver clocks. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 4–42.

Figure 4–44. EP1SGX40 Device Fast Regional Clock Pin Connections to Fast Regional Clocks



Combined Resources

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, 4 regional clock lines, and 2 fast regional clock lines. Multiplexers are used with these clocks to form 8-bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer at the LAB level selects two of the eight row clocks to feed the LE registers within the LAB. See Figure 4–45.

Figure 4–48. PLL Floorplan

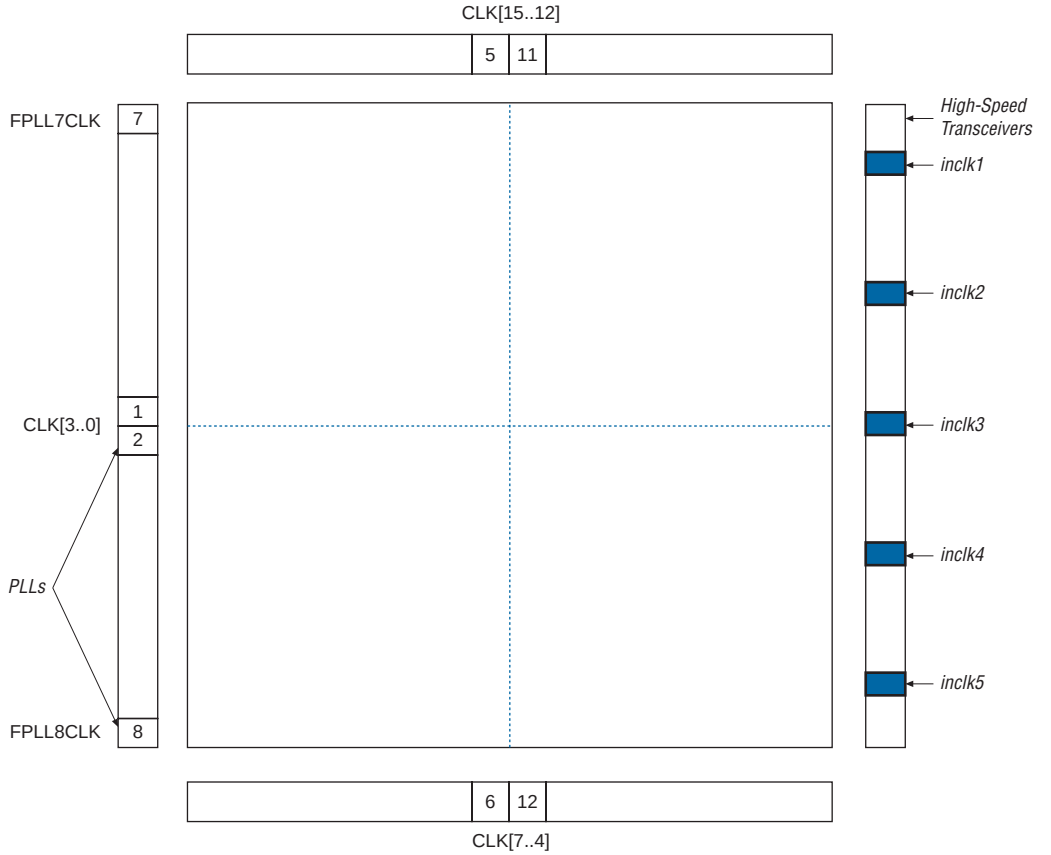


Figure 4–49 shows the global and regional clock connections from the PLL outputs and the CLK pins.

However, there is additional resistance present between the device ball and the input of the receiver buffer, as shown in Figure 4–71. This resistance is because of package trace resistance (which can be calculated as the resistance from the package ball to the pad) and the parasitic layout metal routing resistance (which is shown between the pad and the intersection of the on-chip termination and input buffer).

Figure 4–71. Differential Resistance of LVDS Differential Pin Pair (R_D)

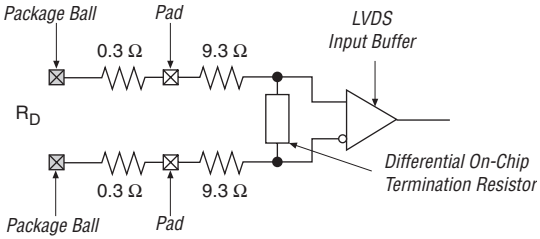


Table 4–31 defines the specification for internal termination resistance for commercial devices.

Table 4–31. Differential On-Chip Termination

Symbol	Description	Conditions	Resistance			Unit
			Min	Typ	Max	
R_D *(2)*	Internal differential termination for LVDS	Commercial *(1)*, *(3)*	110	135	165	Ω
		Industrial *(2)*, *(3)*	100	135	170	Ω

Notes to Table 4–31:

(1) Data measured over minimum conditions (T_j = 0 C, V_{CCIO} +5%) and maximum conditions (T_j = 85 C, V_{CCIO} = –5%).

(2) Data measured over minimum conditions (T_j = –40 C, V_{CCIO} +5%) and maximum conditions (T_j = 100 C, V_{CCIO} = –5%).

(3) LVDS data rate is supported for 840 Mbps using internal differential termination.

MultiVolt I/O Interface

The Stratix GX architecture supports the MultiVolt I/O interface feature, which allows Stratix GX devices in all packages to interface with systems of different supply voltages.

The Stratix GX VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V,

and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

SRAM configuration elements allow Stratix GX devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

Configuration Schemes

You can load the configuration data for a Stratix GX device with one of five configuration schemes (see Table 5–1), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix GX device. A configuration device can automatically configure a Stratix GX device at system power-up.

You can configure multiple Stratix GX devices in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 5–1. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	ByteBlasterMV™ or MasterBlaster™ download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file (.jam or .jbc)

- Receive new configuration data and write it into the configuration device

The factory configuration is the default and takes control if an error occurs while loading the application configuration.

While in the factory configuration, the factory-configuration logic performs the following operations:

- Loads a remote update-control register to determine the page address of the new application configuration
- Determines whether to enable a user watchdog timer for the application configuration
- Determines what the watchdog timer setting should be if it is enabled

The user watchdog timer is a counter that must be continually reset within a specific amount of time in the user mode of an application configuration to ensure that valid configuration occurred during a remote update. Only valid application configurations designed for remote update can reset the user watchdog timer in user mode. If a valid application configuration does not reset the user watchdog timer in a specific amount of time, the timer updates a status register and loads the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

If an error occurs in loading the application configuration, the configuration logic writes a status register to specify the cause of the reconfiguration. Once this occurs, the Stratix GX device automatically loads the factory configuration, which reads the status register and determines the reason for reconfiguration. Based on the reason, the factory configuration takes appropriate steps and writes the remote update control register to specify the next application configuration page to be loaded.

When the Stratix GX device successfully loads the application configuration, it enters into user mode. The Stratix GX device then executes the main application of the user. Intellectual property (IP), such as a Nios® embedded processor, can help the Stratix GX device determine when remote update is coming. The Nios embedded processor or user logic receives incoming data, writes it to the configuration device, and loads the factory configuration. The factory configuration reads the remote update status register and determine the valid application configuration to load. Figure 5–1 shows the Stratix GX remote update. Figure 5–2 shows the transition diagram for remote update mode.

Table 6–21. SSTL-18 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Table 6–22. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			V_{TT} – 0.630	V

Table 6–23. SSTL-2 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V

Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTL	2 mA		830		872		1,002	ps
	8 mA		250		263		302	ps
	12 mA		140		147		169	ps
	16 mA		100		105		120	ps
1.8-V LVTTL	2 mA		1,510		1,586		1,824	ps
	8 mA		420		441		507	ps
	12 mA		350		368		423	ps
1.5-V LVTTL	2 mA		1,740		1,827		2,101	ps
	4 mA		1,160		1,218		1,400	ps
	8 mA		690		725		833	ps
CTT			50		53		61	ps
SSTL-3 class I			90		95		109	ps
SSTL-3 class II			–50		–52		–60	ps
SSTL-2 class I			100		105		120	ps
SSTL-2 class II			20		21		24	ps
LVDS *(1)*			–20		–21		–24	ps
LVPECL *(1)*			40		42		48	ps
PCML *(1)*			–60		–63		–73	ps
HyperTransport Technology *(1)*			70		74		85	ps

Table 6–76. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,911		2,011		2,312	ps
	4 mA		1,911		2,011		2,312	ps
	8 mA		1,691		1,780		2,046	ps
	12 mA		1,471		1,549		1,780	ps
	24 mA		1,341		1,412		1,623	ps