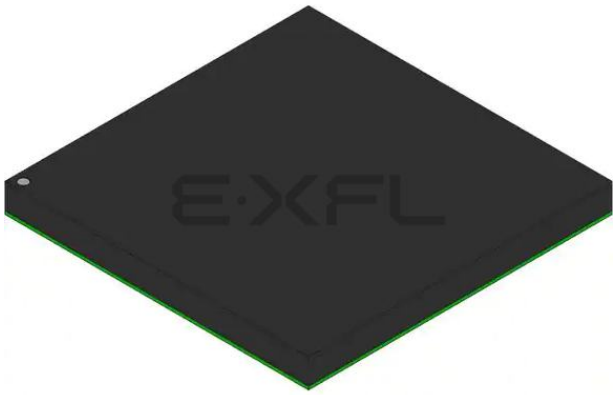
Altera - EP1SGX40DF1020C7N Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

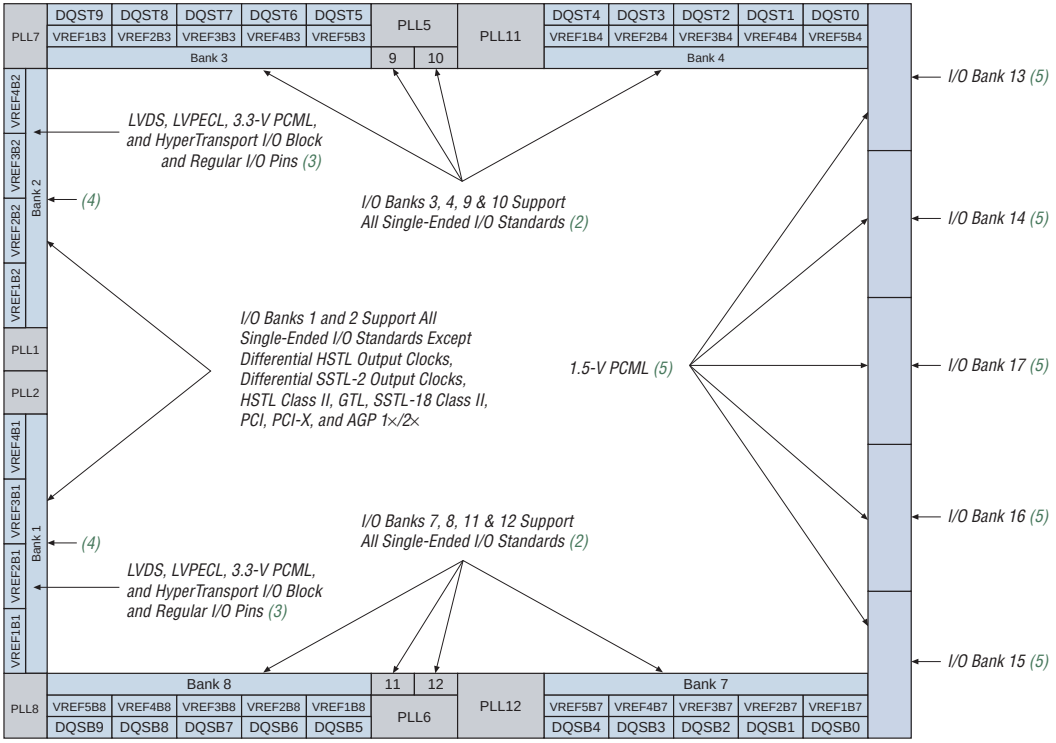
Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx40df1020c7n

Revision History

The table below shows the revision history for Chapters 1 through 7.

Chapter(s)	Date / Version	Changes Made	Comments
1	February 2005, v1.0	Initial Release.	
2	June 2006, v1.1	• Updated "Serial Loopback" section. • Updated Figures 2–1 through 2–3. • Updated Figure 2–13. • Updated Figures 2–26 and 2–27.	
	February 2005, v1.0	Initial Release.	
3	August 2005, v1.1	Added Note (3) to Figure 3-7.	
4	February 2005, v1.0	Initial Release.	
5	February 2005, v1.0	Initial Release.	
6	June 2006, v1.2	• Updated "Operating Conditions" section. • Updated Table 6–4. • Updated note 3 in Table 6–6. • Added note 12 in Table 6–7. • Updated Figure 6–1. • Added Figure 6–2. • Updated Tables 6–13 through 6–16.	• Changed V_{OD} to V_{ID} for receiver input voltage and `refclkb` input voltage in Table 6–4. • Changed value for undershoot during transition from -0.5 V to -2.0 V in note 3 of Table 6–6. • Changed value of V_{OCM} from mV to V in Table 6–15. • Changed unit value of W to Ω.
	August 2005, v1.1	Updated Tables 6-7 and 6-50.	
7	February 2005, v1.0	Initial Release.	

Figure 1–1. Stratix GX I/O Blocks *Note (1)*



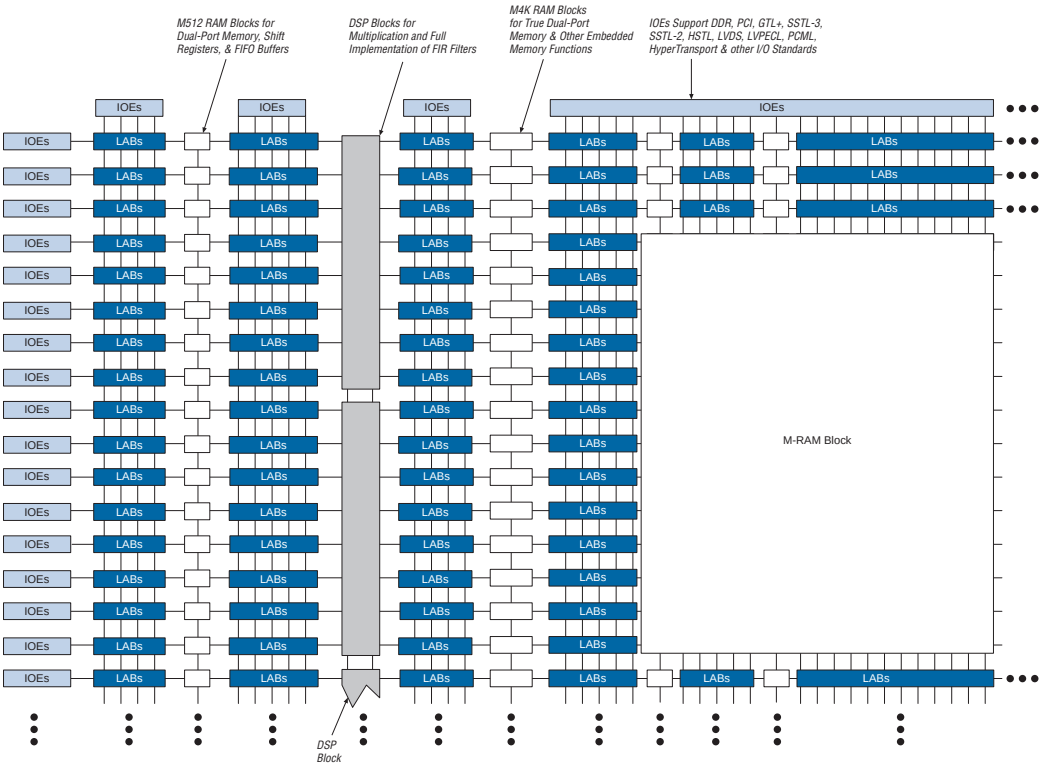
Notes to Figure 1–1:

(1) Figure 1–1 is a top view of the Stratix GX silicon die.
(2) Banks 9 through 12 are enhanced PLL external clock output banks.
(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.
(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.
(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled).

FPGA Functional Description

Stratix GX devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

Figure 1–2. Stratix GX Block Diagram



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 1–5 lists the resources available in Stratix GX devices.

Table 1–5. Stratix GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1SGX10	4 / 94	2 / 60	1	2 / 6	40	30
EP1SGX25	6 / 224	3 / 138	2	2 / 10	62	46
EP1SGX40	8 / 384	3 / 183	4	2 / 14	77	61

The transmitter PLL can support up to 3.1875 Mbps. The input clock frequency for –5 and –6 speed grade devices is limited to 650 MHz if you use the REFCLKB pin or to 325 MHz if you use the other clock routing resources. For –7 speed grade devices, the maximum input clock frequency is 312.5 MHz with the REFCLKB pin, and the maximum is 156.25 MHz for all other clock routing resources. An optional PLL_LOCKED port is available to indicate whether the transmitter PLL is locked to the reference clock. The transmitter PLL has a programmable loop bandwidth that can be set to low or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	25 MHz to 650 MHz
Data rate support	500 Mbps to 3.1875 Gbps
Multiplication factor (W)	2, 4, 5, 8, 10, 16, or 20 *(1)*
Bandwidth	Low, high

Note to Table 2–2:
(1) Multiplication factors 2 and 5 can only be achieved with the use of the pre-divider on the REFCLKB pin.

Transmitter Phase Compensation FIFO Buffer

The transmitter phase compensation FIFO buffer resides in the transceiver block at the PLD boundary. This FIFO buffer compensates for the phase differences between the transmitter reference clock (inclk) and the PLD interface clock (tx_coreclk). The phase difference between the two clocks must be less than 360° . The PLD interface clock must also be frequency locked to the transmitter reference clock. The phase compensation FIFO buffer is four words deep and cannot be bypassed.

Byte Serializer

The byte serializer takes double-width words (16 or 20 bits) from the PLD interface and converts them to a single width word (8 or 10 bits) for use in the transceiver. The transmit data path after the byte serializer is single width (8 or 10 bits). The byte serializer is bypassed when single width mode (8 or 10 bits) is used at the PLD interface.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 shows the code conversion.

Table 2–3. Code Conversion

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, `/K28.0/` (`/R/`) and `/K28.5/` (`/K/`), are automatically randomized based on a PRBS7 pattern with an x^7+x^6+1 polynomial. The `/K28.3/` (`/A/`) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the `/A/`, `/K/`, and `/R/` code groups are done automatically by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8-bit or 10-bit data into a serial stream, transmitting the LSB first. The serialized stream is then fed to the transmit buffer. Figure 2–5 is a diagram of the serializer.

have four dedicated fast PLLs for clock multiplication. Table 3–3 shows the maximum number of channels in each Stratix GX device that support DPA.

Table 3–3. Stratix GX Source-Synchronous Differential I/O Resources

Device	Fast PLLs	Pin Count	Receiver Channels *(1)*	Transmitter Channels *(1)*	Receiver & Transmitter Channel Speed (Gbps) *(2)*	LEs
EP1SGX10C	2 *(3)*	672	22	22	1	10,570
EP1SGX10D	2 *(3)*	672	22	22	1	10,570
EP1SGX25C	2	672	39	39	1	25,660
EP1SGX25D	2	672	39	39	1	25,660
		1,020	39	39	1	25,660
EP1SGX25F	2	1,020	39	39	1	25,660
EP1SGX40D	4 *(4)*	1,020	45	45	1	41,250
EP1SGX40G	4 *(4)*	1,020	45	45	1	41,250

Notes to Table 3–3:

(1) This is the number of receiver or transmitter channels in the source-synchronous (I/O bank 1 and 2) interface of the device.

(2) Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps.

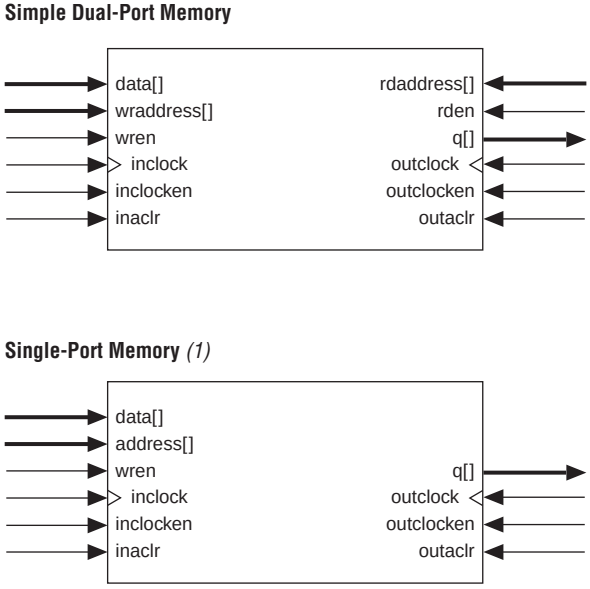
(3) One of the two fast PLLs in EP1SGX10C and EP1SGX10D devices supports DPA.

(4) Two of the four fast PLLs in EP1SGX40D and EP1SGX40G devices support DPA

The receiver and transmitter channels are interleaved so that each I/O row in I/O banks 1 and 2 of the device has one receiver channel and one transmitter channel per row. Figures 3–6 and 3–7 show the fast PLL and channels with DPA layout in EP1SGX10, EP1SGX25, and EP1SGX40 devices. In EP1SGX10 devices, only fast PLL 2 supports DPA operations.

occurs or just read the don't care bits. Single-port memory supports non-simultaneous reads and writes, but the q[] port outputs the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see the *TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*. Figure 4–12 shows these different RAM memory port configurations for TriMatrix memory.

Figure 4–12. Simple Dual-Port & Single-Port Memory Configurations



Note to Figure 4–12:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (WREN) signal derived from the global

Table 4–10. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2)	
byteena[15..0]	**datain ×144**
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

Notes to Tables 4–9 and 4–10:

(1) Any combination of byte enables is possible.

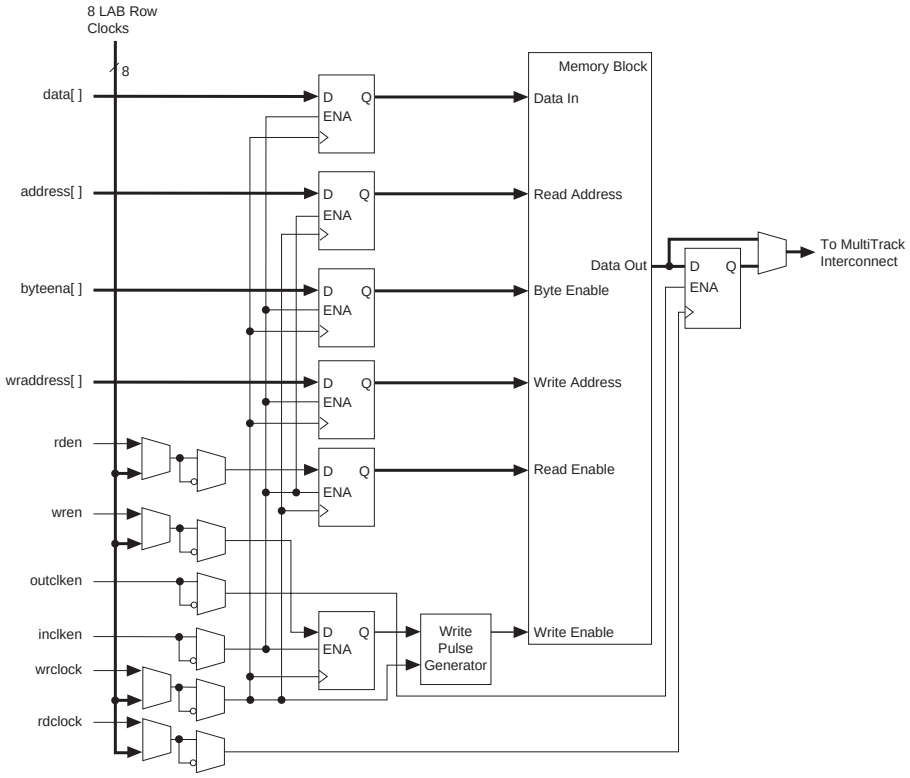
(2) Byte enables can be used in the same manner with 8-bit words, that is, in ×16, ×32, ×64, and ×128 modes.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals as shown in Figure 4–18.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 4–24 and 4–25 show the memory block in input/output clock mode.

Figure 4–25. Input/Output Clock Mode in Simple Dual-Port Mode *Note (1)*



Note to Figure 4–25:
(1) All registers shown except the `rden` register have asynchronous clear ports.

Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. You can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 4–26 shows a memory block in read/write clock mode.

the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 4–28 shows one of the columns with surrounding LAB rows.

Pipeline/Post Multiply Register

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register pipelines the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. You can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 4–33 shows the adder and output stages.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

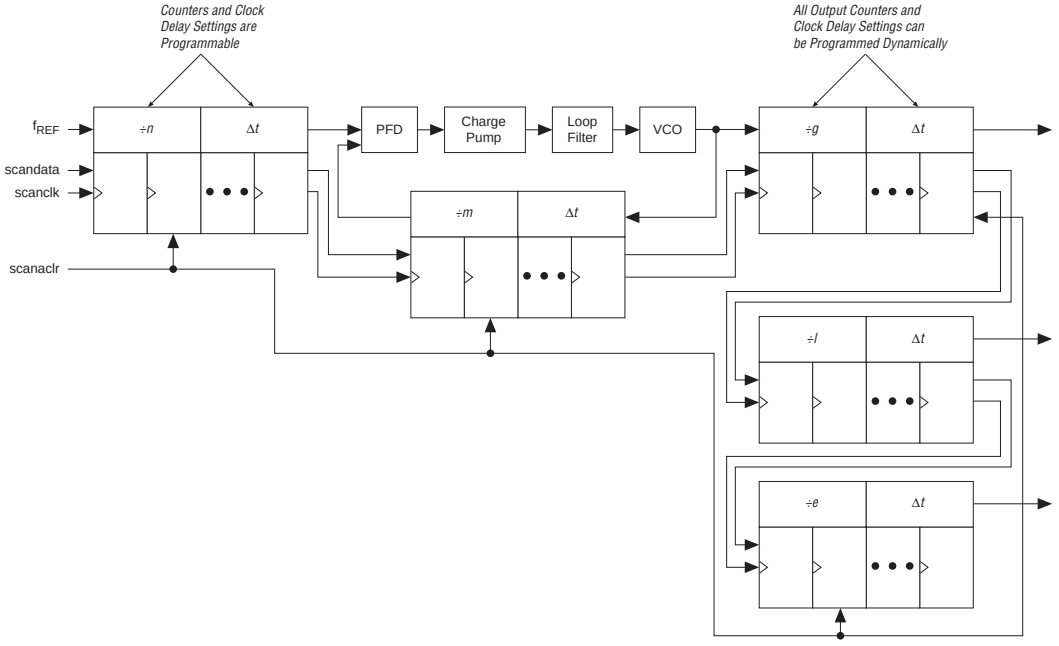
- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18 × 18-bit multipliers or eight 9 × 9-bit multipliers can drive their results directly out of one DSP block. See Figure 4–34.

Figure 4–53. Dynamically Programmable Counters & Delays in Stratix GX Device Enhanced PLLs



PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.

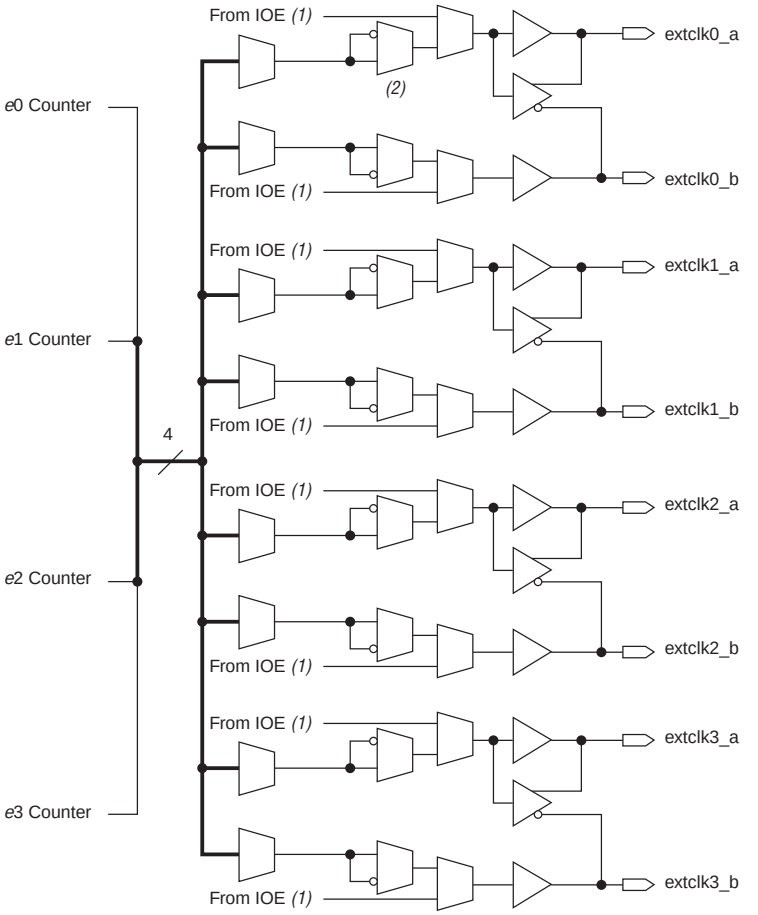
Programmable Bandwidth

You have advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also allows a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL takes longer to lock, but it attenuates all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and *m* counter value. You can manually adjust these values if desired. Bandwidth is programmable from 150 kHz to 2 MHz.

External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See Figure 4–54.

Figure 4–54. External Clock Outputs for PLLs 5 & 6



Notes to Figure 4–54:

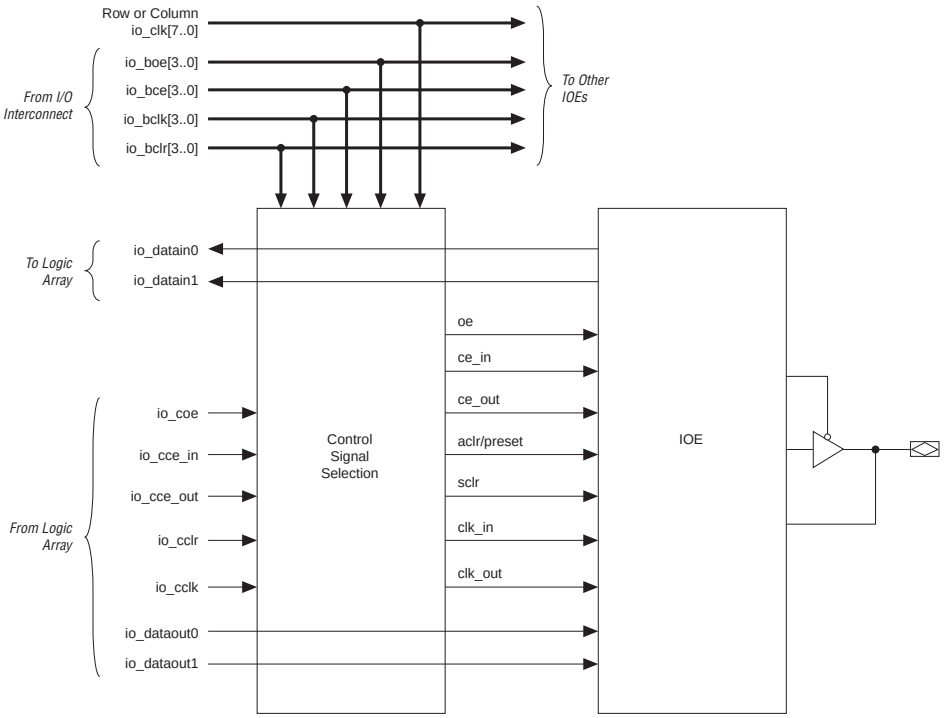
(1) Each external clock output pin can be used as a general purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each

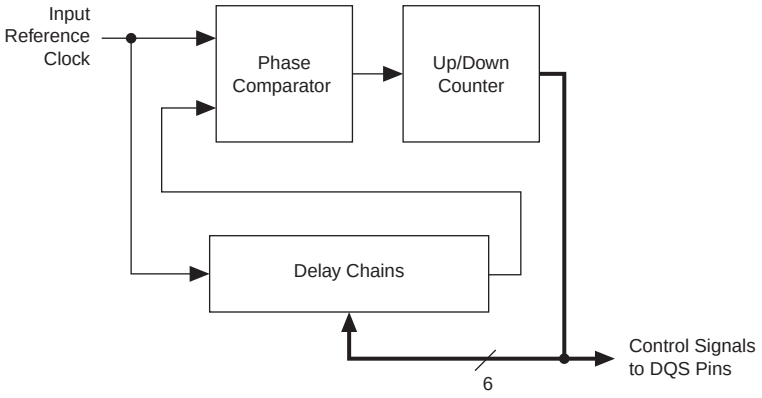
Stratix GX devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 4–68). Figure 4–61 illustrates the signal paths through the I/O block.

Figure 4–61. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 4–62 illustrates the control signal selection.

Figure 4–68. Simplified Diagram of the DQS Phase-Shift Circuitry



See the *External Memory Interfaces* chapter of the *Stratix GX Device Handbook, Volume 2* for more information on external memory interfaces.

Programmable Drive Strength

The output buffer for each Stratix GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 6–48. M4K Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{M4KDATACO1}$		571		635		729	ps
$t_{M4KDATACO2}$		3,984		4,507		5,182	ps
$t_{M4KCLKHL}$	150		167		192		ps
t_{M4KCLR}	170		189		255		ps

Table 6–49. M-RAM Block Internal Timing Microparameters

Symbol	-5		-6		-7		Unit
	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562	ps
t_{MRAMWC}		3,654		4,127		4,746	ps
$t_{MRAMWERESU}$	25		25		28		ps
$t_{MRAMWERH}$	18		20		23		ps
$t_{MRAMDATASU}$	25		25		28		ps
$t_{MRAMDATAH}$	18		20		23		ps
$t_{MRAMWADDRASU}$	25		25		28		ps
$t_{MRAMWADDRH}$	18		20		23		ps
$t_{MRAMRADDRASU}$	25		25		28		ps
$t_{MRAMRADDRH}$	18		20		23		ps
$t_{MRAMDATABSU}$	25		25		28		ps
$t_{MRAMDATABH}$	18		20		23		ps
$t_{MRAMADDRBSU}$	25		25		28		ps
$t_{MRAMADDRBH}$	18		20		23		ps
$t_{MRAMDATACO1}$		1,038		1,053		1,210	ps
$t_{MRAMDATACO2}$		4,362		4,939		5,678	ps
$t_{MRAMCLKHL}$	270		300		345		ps
$t_{MRAMCLR}$	135		150		172		ps