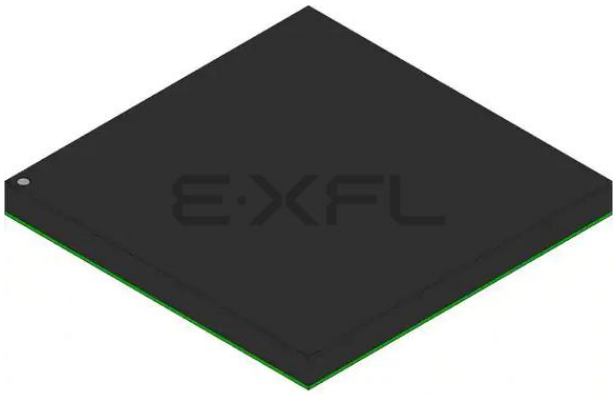
Altera - EP1SGX40GF1020C5 Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx40gf1020c5

1. Introduction to the Stratix GX Device Data Sheet

SGX51001-1.0

Overview

The Stratix® GX family of devices is Altera's second FPGA family to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES capability at data rates of up to 3.1875 gigabits per second (Gbps). These transceivers are grouped by four-channel transceiver blocks, and are designed for low power consumption and small die size. The Stratix GX FPGA technology is built upon the Stratix architecture, and offers a 1.5-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

- Transceiver block features are as follows:
  - High-speed serial transceiver channels with CDR provides 500-megabits per second (Mbps) to 3.1875-Gbps full-duplex operation
  - Devices are available with 4, 8, 16, or 20 high-speed serial transceiver channels providing up to 127.5 Gbps of full-duplex serial bandwidth
  - Support for transceiver-based protocols, including 10 Gigabit Ethernet attachment unit interface (XAUI), Gigabit Ethernet (GigE), and SONET/SDH
  - Compatible with PCI Express, SMPTE 292M, Fibre Channel, and Serial RapidIO I/O standards
  - Programmable differential output voltage (V_{OD}), pre-emphasis, and equalization settings for improved signal integrity
  - Individual transmitter and receiver channel power-down capability implemented automatically by the Quartus® II software for reduced power consumption during non-operation
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, and 20-bit wide data paths
  - 1.5-V pseudo current mode logic (PCML) for 500 Mbps to 3.1875 Gbps
  - Support for LVDS, LVPECL, and 3.3-V PCML on reference clocks and receiver input pins (AC-coupled)
  - Built-in self test (BIST)
  - Hot insertion/removal protection circuitry

Transmitter Path

This section describes the data path through the Stratix GX transmitter (see Figure 2–2). Data travels through the Stratix GX transmitter via the following modules:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

Transmitter PLL

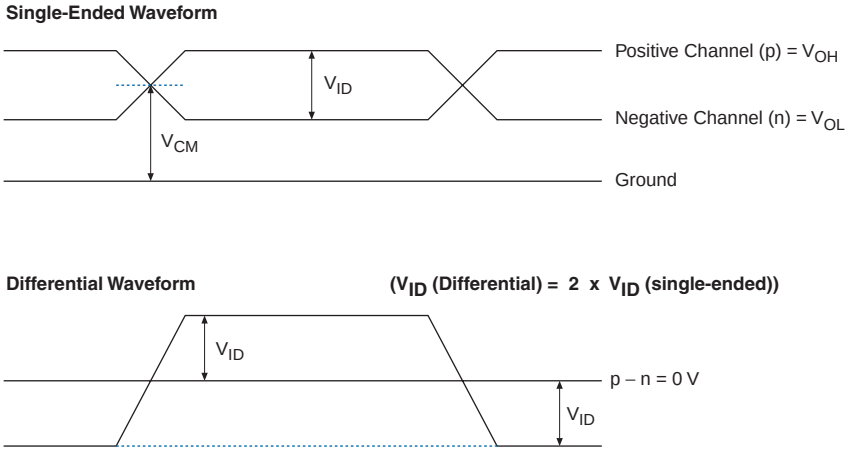
Each transceiver block has one transmitter PLL, which receives the reference clock and generates the following signals:

- High-speed serial clock used by the serializer
- Slow-speed reference clock used by the receiver
- Slow-speed clock used by the logic array (divisible by two for double-width mode)

The INCLK clock is the input into the transmitter PLL. There is one INCLK clock per transceiver block. This clock can be fed by either the REFCLKB pin, PLD routing, or the inter-transceiver routing line. See the section "Stratix GX Clocking" on page 2–30 for more information about the inter-transceiver lines.

The transmitter PLL in each transceiver block clocks the circuits in the transmit path. The transmitter PLL is also used to train the receiver PLL. If no transmit channels are used in the transceiver block, the transmitter PLL can be turned off. Figure 2–3 is a block diagram of the transmitter PLL.

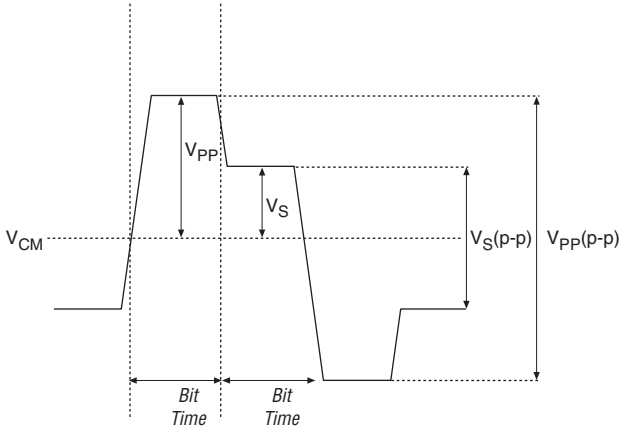
Figure 2–7. V_{OD} Differential



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost the high frequency components, to compensate for losses in the transmission medium, as shown in Figure 2–8. The pre-emphasis can be dynamically or statically set. There are five possible pre-emphasis settings (1 through 5), with 5 being the highest and 0 being no pre-emphasis.

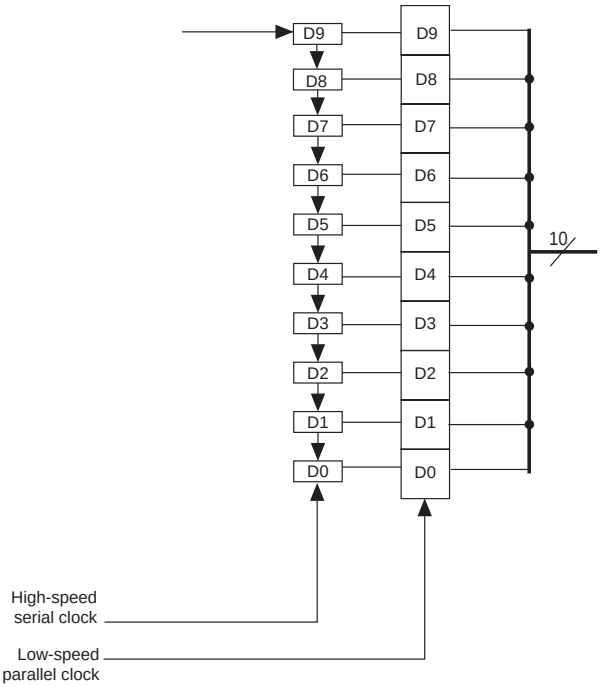
Figure 2–8. Programmable Pre-Emphasis Model



Deserializer (Serial-to-Parallel Converter)

The deserializer converts the serial stream into a parallel 8- or 10-bit data bus. The deserializer receives the least significant bit first. Figure 2–14 is a diagram of the deserializer.

Figure 2–14. Deserializer

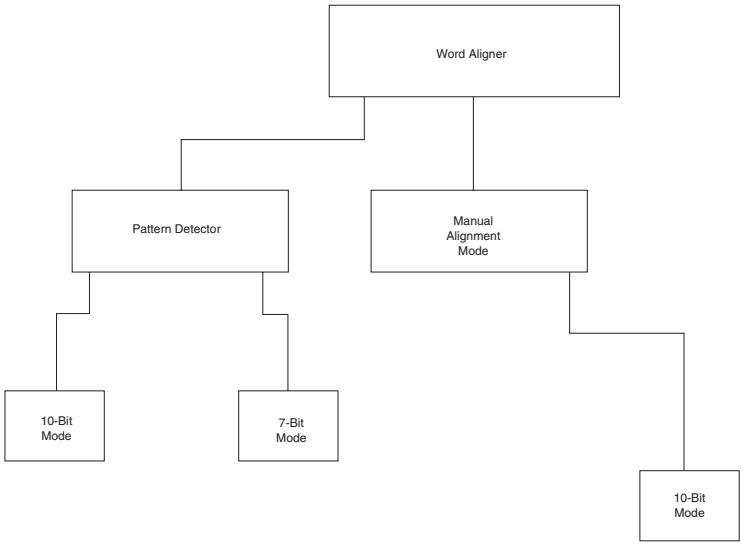


Word Aligner

The word aligner aligns the incoming data based on the specific byte boundaries. The word aligner has three customizable modes of operation: bit-slip mode, 16-bit mode, and 10-bit mode, the last of which is available for the basic and SONET modes. The word aligner also has two non-customizable modes of operation, which are the XAUI and GIGE modes.

Figure 2–15 shows the word aligner in bit-slip mode.

Figure 2–17. Word Aligner in 10-Bit Mode

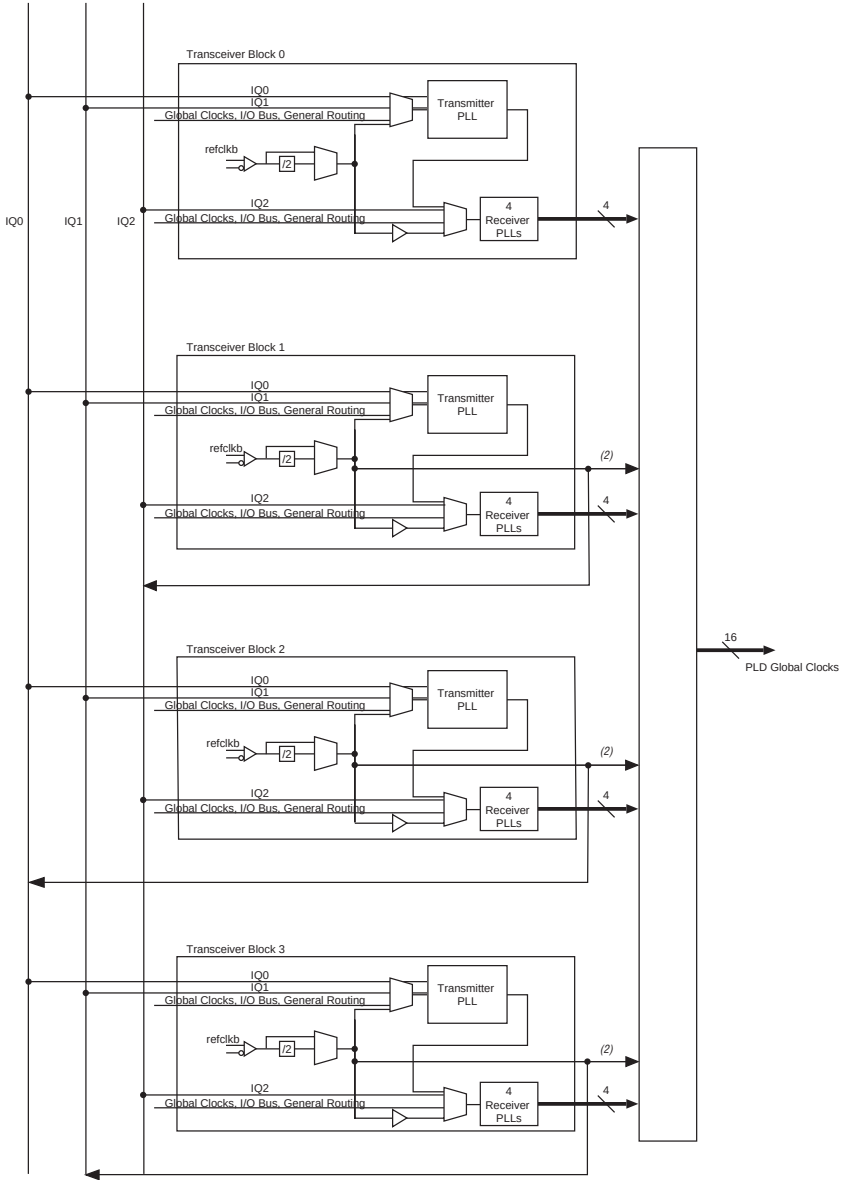


In the 10-bit mode, the word aligner automatically aligns the user's predefined 10-bit alignment pattern. The pattern detector can detect the full 10-bit pattern or only the lower seven bits of the pattern. The word aligner and pattern detector detect both the positive and the negative disparity of the pattern. A user-controlled enable port is available for the word aligner.

The 10-bit mode is available only for the Custom mode.

Figure 2–18 shows the word aligner in XAUI mode.

Figure 2–26. EP1SGX25F Device Inter-Transceiver & Global Clock Connections *Note (1)*



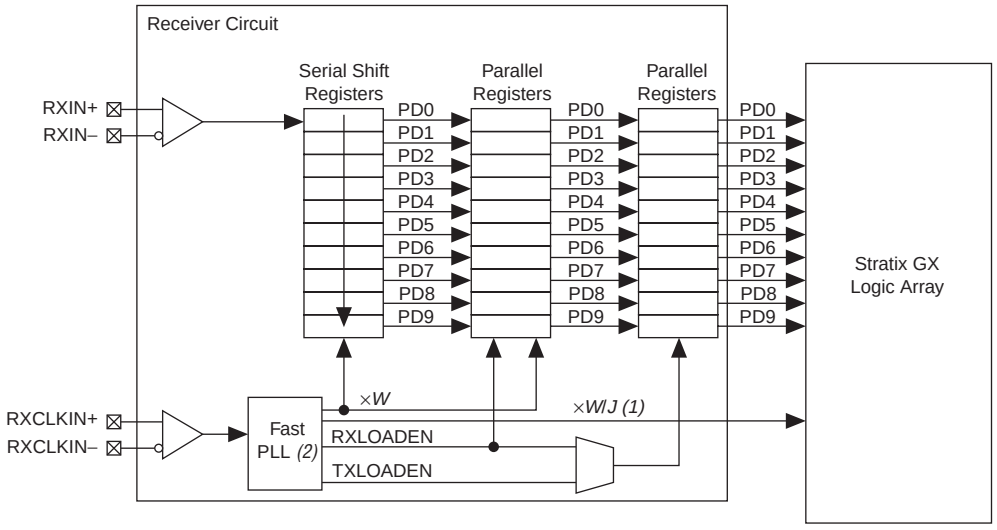
Notes to Figure 2–26:

(1) IQ lines are inter-transceiver block lines.

(2) If the /2 pre-divider is used, the path to drive the PLD logic array, local, or global clocks is not allowed.

(3) There are four receiver PLLs in each transceiver block.

Figure 3–1. Stratix GX High-Speed Interface Deserialized in ×10 Mode

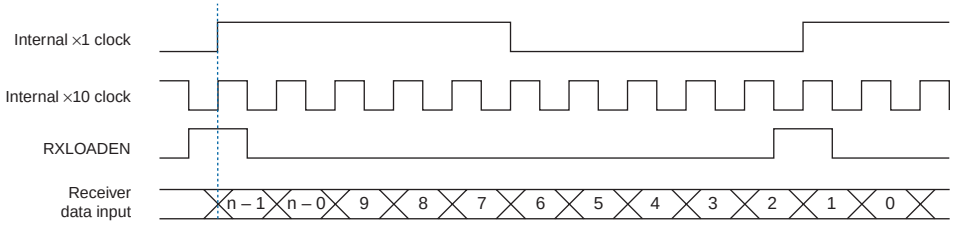


Notes to Figure 3–1:

(1) W = 1, 2, 4, 7, 8, or 10.
J = 4, 7, 8, or 10 for non-DPA (J = 8 or 10 for DPA).
W does not have to equal J. When J = 1 or 2, the deserializer is bypassed. When J = 2, the device uses DDRIO registers.

(2) This figure does not show additional circuitry for clock or data manipulation.

Figure 3–2. Receiver Timing Diagram



Stratix GX Differential I/O Transmitter Operation

You can configure any of the Stratix GX differential output channels as a transmitter channel. The differential transmitter serializes outbound parallel data.

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 4–4 and 4–5 summarize the possible M4K RAM block configurations.

Table 4–4. M4K RAM Block Configurations (Simple Dual-Port)

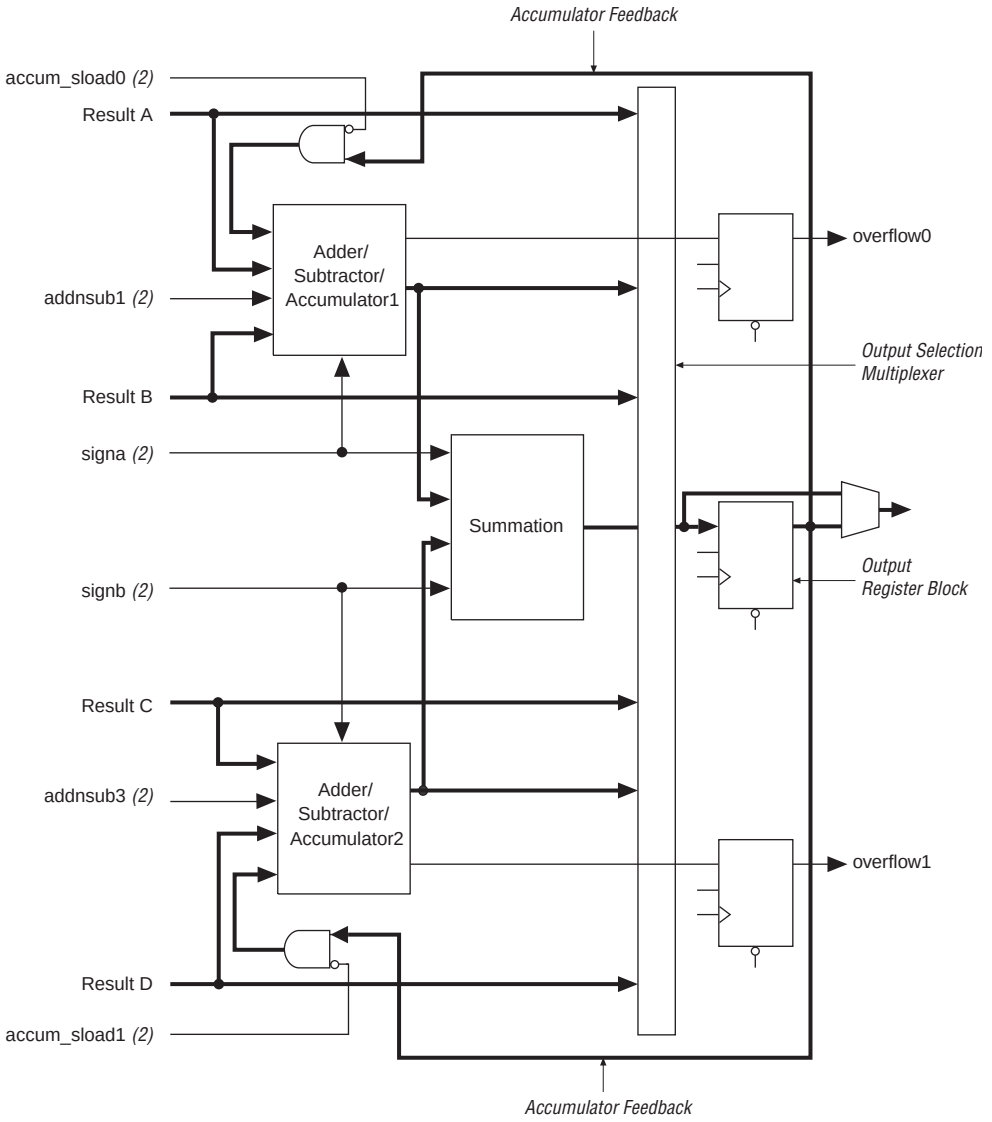
Read Port	Write Port								
	4K 1	2K × 2	1K ° 4	512 ° 8	256 ° 16	128 ° 32	512 ° 9	256 ° 18	128 ° 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 4–5. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 4–33. Adder/Output Blocks *Note (1)*



Notes to Figure 4–33:

(1) Adder/output block shown in Figure 4–33 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

Adder/Subtractor/Accumulator

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

Adder/Subtractor
Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 × 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 × 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

Accumulator
When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 4–33. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

Summation

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 × 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 × 9-bit multipliers. In 18 × 18-bit mode, there is one summation providing the sum of one set of four 18 × 18-bit multipliers.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (that is, implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 4–15 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 4–15. Multiplier Size & Configurations per DSP block

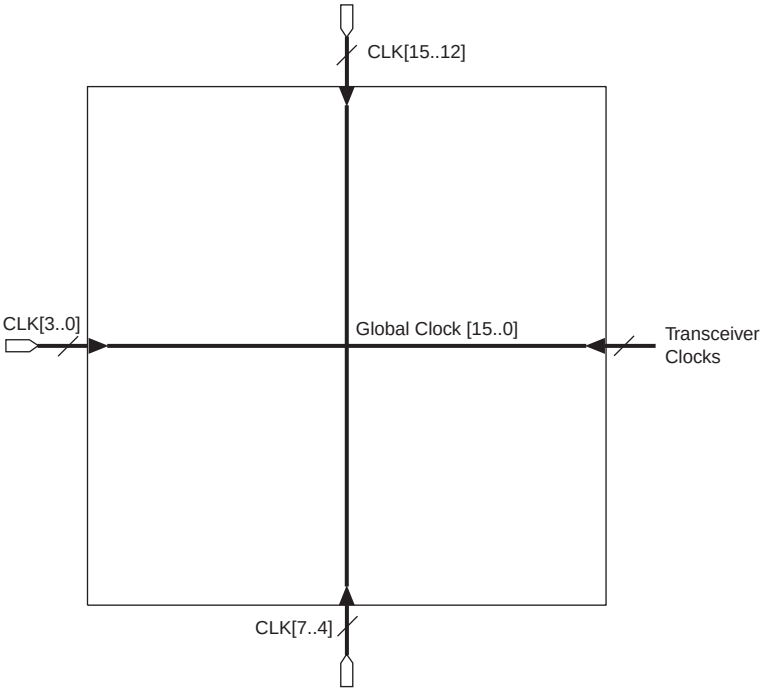
DSP Block Mode	9 × 9	18 × 18	36 × 36 *(1)*
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

Note to Table 4–15:
(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP Block Interface

Stratix GX device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

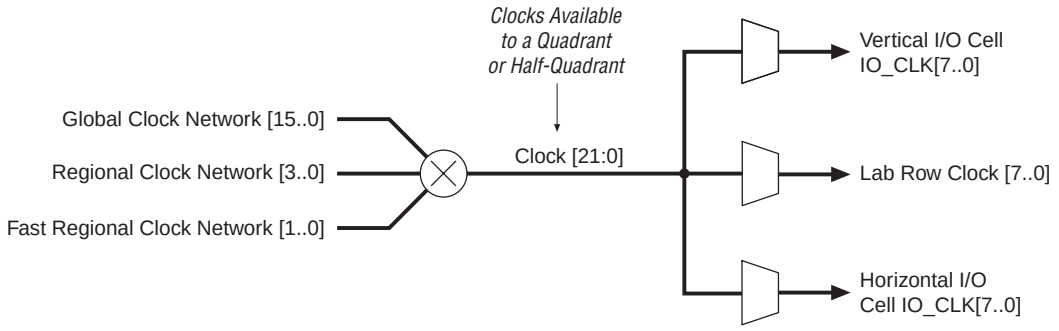
Figure 4–41. Global Clock Resources



Regional Clock Network

There are four regional clock networks RCLK[3..0] within each quadrant of the Stratix GX device that are driven by the same dedicated CLK[7..0] and CLK[15..12] input pins, PLL outputs, or transceiver clocks. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 4–42.

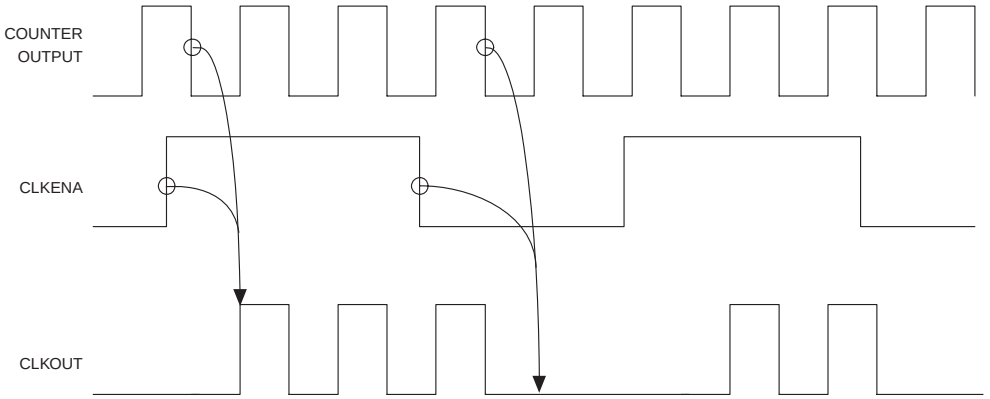
Figure 4–45. Regional Clock Bus



IOE clocks have horizontal and vertical block regions that are clocked by eight I/O clock signals chosen from the 22-quadrant or half-quadrant clock resources. Figures 4–46 and 4–47 show the quadrant and half-quadrant relationship to the I/O clock regions, respectively. The vertical regions (column pins) have less clock delay than the horizontal regions (row pins).

unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

Figure 4–56. extclkena Signals



Fast PLLs

Stratix GX devices contain up to four fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 4–57 shows a diagram of the fast PLL.

Phase Shifting

Stratix GX device fast PLLs have advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 150 to 400 ps. This resolution is a function of the VCO period.

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

For more information on high-speed differential I/O support, see the *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

The IOE in Stratix GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 4–58 shows the Stratix GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Table 4–22 shows the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1SGX10 through EP1SGX40 devices. The DDR SDRAM and QDR SRAM numbers in Table 4–22 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 4–22. External RAM Support in EP1SGX10 Through EP1SGX40 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)		
		-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
DDR SDRAM *(1)*, *(2)*	SSTL-2	200	167	133
DDR SDRAM - side banks *(2)*, *(3)*, *(4)*	SSTL-2	150	133	133
RLDRAM II *(4)*	1.8-V HSTL	200	*(5)*	*(5)*
QDR SRAM *(6)*	1.5-V HSTL	167	167	133
QDRII SRAM *(6)*	1.5-V HSTL	200	167	133
ZBT SRAM *(7)*	LVTTL	200	200	167

Notes to Table 4–22:

(1) These maximum clock rates apply if the Stratix GX device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).
(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*
(3) DDR SDRAM is supported on the Stratix GX device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.
(4) These performance specifications are preliminary.
(5) This device does not support RLDRAM II.
(6) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.
(7) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

In addition to six I/O registers and one input latch in the IOE for interfacing to these high-speed memory interfaces, Stratix GX devices also have dedicated circuitry for interfacing with DDR SDRAM. In every Stratix GX device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR SDRAM up to 200 MHz. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32.

Table 4–24 shows the possible settings for the I/O standards with drive strength control.

Table 4–24. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL class I and II 1.8-V HSTL class I and II SSTL-3 class I and II SSTL-2 class I and II SSTL-18 class I and II	Support maximum and minimum strength

Notes to Table 4–24:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1 and 2 do not support this setting.

The Quartus II software, beginning with version 4.2, reports current strength as "PCI Compliant" for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix GX devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix GX devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

SRAM configuration elements allow Stratix GX devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

Configuration Schemes

You can load the configuration data for a Stratix GX device with one of five configuration schemes (see Table 5–1), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix GX device. A configuration device can automatically configure a Stratix GX device at system power-up.

You can configure multiple Stratix GX devices in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 5–1. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	ByteBlasterMV™ or MasterBlaster™ download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file (.jam or .jbc)

Tables 6–13 through 6–33 provide information about specifications and bus hold parameters for 1.5-V Stratix GX devices. Notes for Tables 6–14 through 6–33 immediately follow Table 6–33.

Table 6–13. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} *(1)*	Input differential voltage swing (single-ended)	0.1 V < V_{CM} < 1.1 V *W* = 1 through 10	300		1,000	mV
		1.1 V < V_{CM} < 1.6 V *W* = 1	200		1,000	mV
		1.1 V < V_{CM} < 1.6 V *W* = 2 through 10	100		1,000	mV
		1.6 V < V_{CM} < 1.8 V *W* = 1 through 10	300		1,000	mV
V_{ICM} *(1)*	Input common-mode voltage	LVDS 0.3 V < V_{ID} < 1.0 V *W* = 1 through 10	100		1,100	mV
		LVDS 0.3 V < V_{ID} < 1.0 V *W* = 1 through 10	1,600		1,800	mV
		LVDS 0.2 V < V_{ID} < 1.0 V *W* = 1	1,100		1,600	mV
		LVDS 0.1 V < V_{ID} < 1.0 V *W* = 2 through 10	1,100		1,600	mV
V_{OD}	Differential output voltage (single ended)	R_L = 100 Ω	250	375	550	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OCM}	Output common-mode voltage	R_L = 100 Ω	1,125	1,200	1,375	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor, external		90	100	110	Ω

Note to Table 6–13:
(1) For up to 1 Gbps in DPA mode and 840 Mbps in non-DPA mode

Table 6–45. IOE Internal Timing Microparameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	64		68		68		ps
t_{H}	76		80		80		ps
t_{CO}		162		171		171	ps
$t_{PIN2COMBOUT\_R}$		1,038		1,093		1,256	ps
$t_{PIN2COMBOUT\_C}$		927		976		1,122	ps
$t_{COMBIN2PIN\_R}$		2,944		3,099		3,563	ps
$t_{COMBIN2PIN\_C}$		3,189		3,357		3,860	ps
t_{CLR}	262		276		317		ps
t_{PRE}	262		276		317		ps
t_{CLKHL}	90		95		109		ps

Table 6–46. DSP Block Internal Timing Microparameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0		0		0		ps
t_{H}	67		75		86		ps
t_{CO}		142		158		181	ps
$t_{INREG2PIPE18}$		2,613		2,982		3,429	ps
$t_{INREG2PIPE9}$		3,390		3,993		4,591	ps
$t_{PIPE2OUTREG2ADD}$		2,002		2,203		2,533	ps
$t_{PIPE2OUTREG4ADD}$		2,899		3,189		3,667	ps
t_{PD9}		3,709		4,081		4,692	ps
t_{PD18}		4,795		5,275		6,065	ps
t_{PD36}		7,495		8,245		9,481	ps
t_{CLR}	450		500		575		ps
t_{CLKHL}	1,350		1,500		1,724		ps