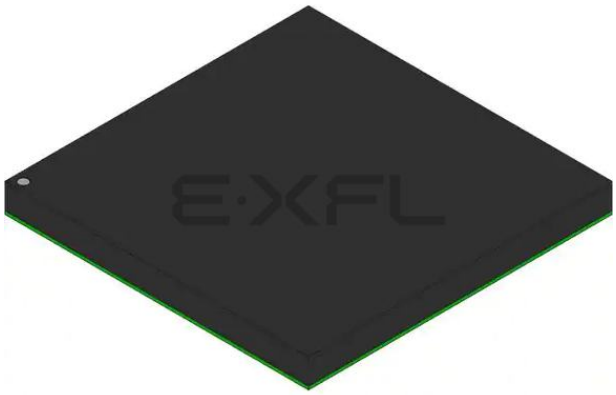

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

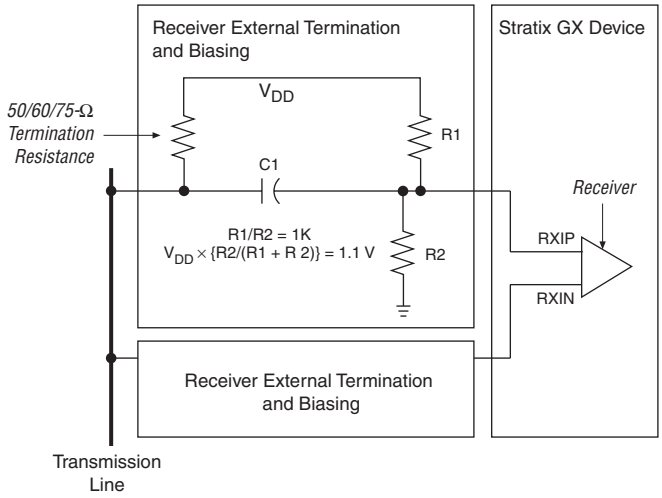
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx40gf1020c5n

Figure 2–12. External Termination & Biasing Circuit



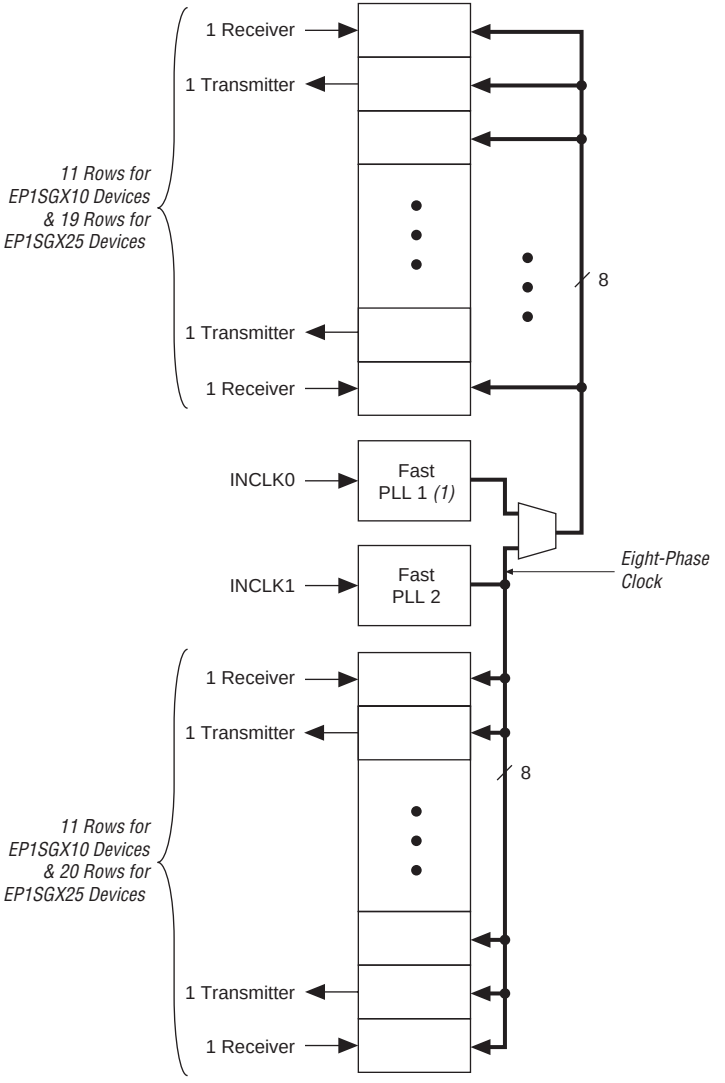
Programmable Equalizer

The programmable equalizer module boosts the high frequency components of the incoming signal to compensate for losses in the transmission medium. There are five possible equalization settings (0, 1, 2, 3, 4) to compensate for 0", 10", 20", 30", and 40" of FR4 trace. These settings should be interpreted loosely. The programmable equalizer can be set dynamically or statically.

Receiver PLL & CRU

Each transceiver block has four receiver PLLs and CRUs, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, then the receiver PLL or CRU is powered down for the channel. Figure 2–13 is a diagram of the receiver PLL and CRU circuits.

Figure 3–6. PLL & Channel Layout in EP1SGX10 & EP1SGX25 Devices *Notes (1), (2)*



Notes to Figure 3–6:

(1) Fast PLL 1 in EP1SGX10 devices does not support DPA.

(2) Not all eight phases are used by the receiver channel or transmitter channel in non-DPA mode.

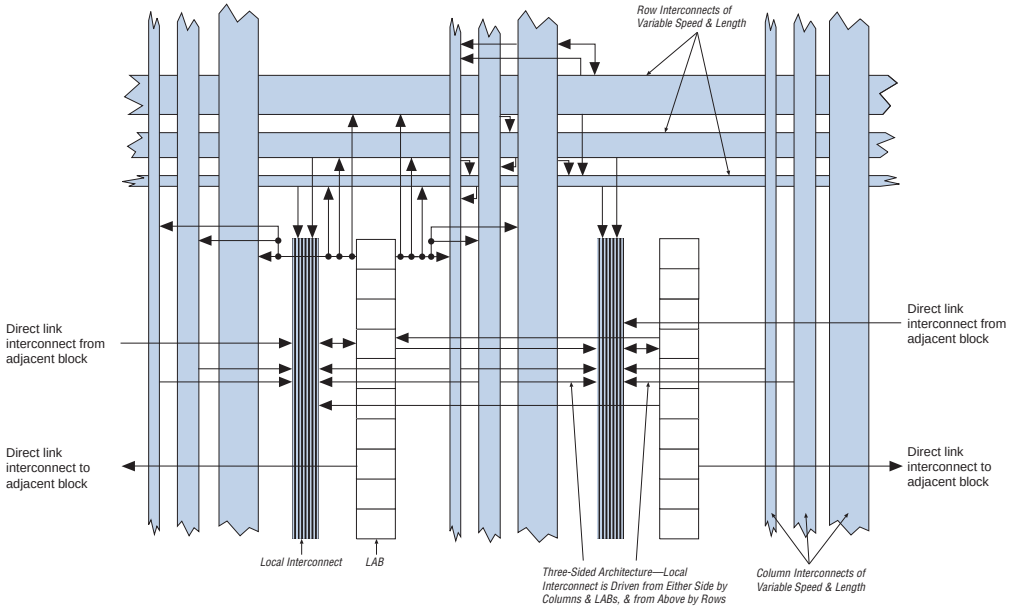
4. Stratix GX Architecture

SGX51004-1.0

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 4–1 shows the Stratix® GX LAB.

Figure 4–1. Stratix GX LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks,

its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 4–11 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Stratix GX LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset load, synchronous clear, synchronous load, and

or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM WREN signal while ensuring its data and address signals meet setup and hold time specifications relative to the WREN signal. The output registers can be bypassed. Flow-through reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 × 16-bit RAM blocks can be combined to form a 256 × 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words available in one memory block. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

Parity Bit Support

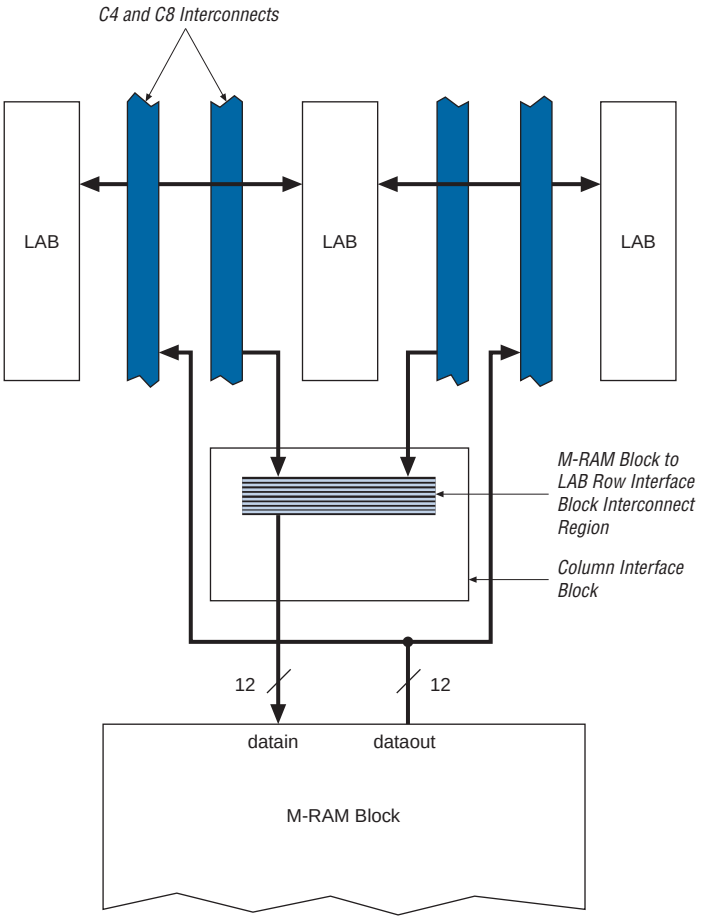
The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

Shift Register Support

You can configure embedded memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512

Figure 4–22. M-RAM Column Unit Interface to Interconnect



Pipeline/Post Multiply Register

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register pipelines the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. You can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 4–33 shows the adder and output stages.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (that is, implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 4–15 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 4–15. Multiplier Size & Configurations per DSP block

DSP Block Mode	9 × 9	18 × 18	36 × 36 *(1)*
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

Note to Table 4–15:
(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP Block Interface

Stratix GX device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

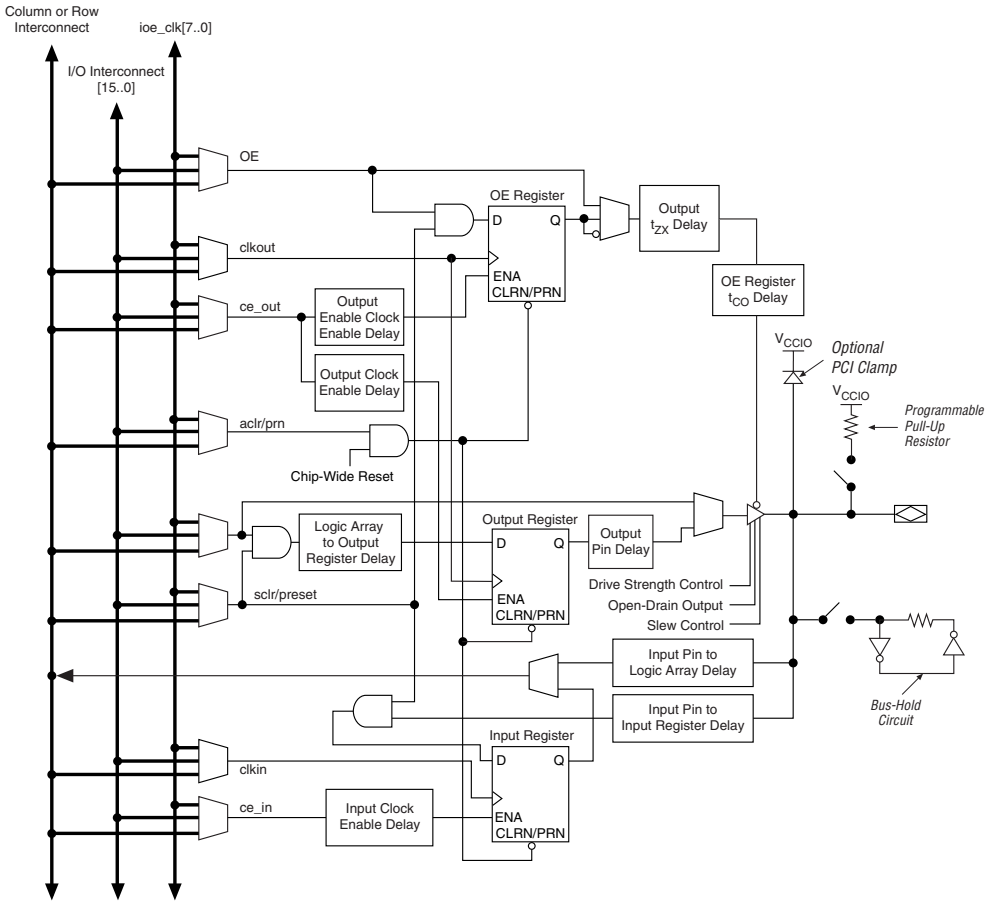
Table 4–18. Stratix GX Enhanced PLL & Fast PLL Features (Part 2 of 2) Notes (1)–(8)		
Feature	**Enhanced PLL**	**Fast PLL**
Number of external clock outputs	Four differential/eight singled-ended or one single-ended *(6)*	*(7)*
Number of feedback clock inputs	4 *(8)*	

Notes to Table 4–18:

(1) The maximum count value is 1024, with a 50% duty cycle setting on the counter. The maximum count value for any other duty cycle setting is 512.
(2) For fast PLLs, *m* and post-scale counters range from 1 to 32.
(3) The smallest phase shift is determined by the VCO period divided by 8.
(4) For degree increments, Stratix GX devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) PLLs 7 and 8 have two output ports per PLL. PLLs 1 and 2 have three output ports per PLL.
(6) Every Stratix GX device has two enhanced PLLs (PLLs 5 and 6) with eight single-ended or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1SGX40 devices each have one single-ended output.
(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(8) Every Stratix GX device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 4–48 shows a top-level diagram of the Stratix GX device and the PLL floorplan.

Figure 4–63. Stratix GX IOE in Bidirectional I/O Configuration *Note (1)*



Note to Figure 4–63:
(1) All input signals to the IOE can be inverted at the IOE.

The Stratix GX device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time.

Table 4–24 shows the possible settings for the I/O standards with drive strength control.

Table 4–24. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL class I and II 1.8-V HSTL class I and II SSTL-3 class I and II SSTL-2 class I and II SSTL-18 class I and II	Support maximum and minimum strength

Notes to Table 4–24:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1 and 2 do not support this setting.

The Quartus II software, beginning with version 4.2, reports current strength as "PCI Compliant" for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix GX devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix GX devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

Table 6–21. SSTL-18 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Table 6–22. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			V_{TT} – 0.630	V

Table 6–23. SSTL-2 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V

Table 6–35. Stratix GX Device Performance (Part 3 of 3) *Notes (1), (2)*

Applications		Resources Used			Performance			
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
TriMatrix memory M-RAM block	True dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	MHz
	Single port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	MHz
	Single port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	MHz
DSP block	9 × 9-bit multiplier *(3)*	0	0	1	335.0	293.94	255.68	MHz
	18 × 18-bit multiplier *(4)*	0	0	1	278.78	237.41	206.52	MHz
	36 × 36-bit multiplier *(4)*	0	0	1	148.25	134.71	117.16	MHz
	36 × 36-bit multiplier *(5)*	0	0	1	278.78	237.41	206.52	MHz
	18-bit, 4-tap FIR filter	0	0	1	278.78	237.41	206.52	MHz
Larger Designs	8-bit, 16-tap parallel FIR filter	58	0	4	141.26	133.49	114.88	MHz
	8-bit, 1,024-point FFT function	870	5	1	261.09	235.51	205.21	MHz

Notes to Table 6–35:

(1) These design performance numbers were obtained using the Quartus II software.
(2) Numbers not listed will be included in a future version of the data sheet.
(3) This application uses registered inputs and outputs.
(4) This application uses registered multiplier input and output stages within the DSP block.
(5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Table 6–41. M-RAM Block Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
$t_{MRAMDATABSU}$	B port setup time before clock
$t_{MRAMDATABH}$	B port hold time after clock
$t_{MRAMADDRBSU}$	B port address setup time before clock
$t_{MRAMADDRBH}$	B port address hold time after clock
$t_{MRAMDATACO1}$	Clock-to-output delay when using output registers
$t_{MRAMDATACO2}$	Clock-to-output delay without output registers
$t_{MRAMCLKHL}$	Minimum clock high or low time
$t_{MRAMCLR}$	Minimum clear pulse width

Table 6–42. Routing Delay Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns
t_{R8}	Delay for an R8 line with average loading; covers a distance of eight LAB columns
t_{R24}	Delay for an R24 line with average loading; covers a distance of 24 LAB columns
t_{C4}	Delay for an C4 line with average loading; covers a distance of four LAB rows
t_{C8}	Delay for an C8 line with average loading; covers a distance of eight LAB rows
t_{C16}	Delay for an C16 line with average loading; covers a distance of 16 LAB rows
t_{LOCAL}	Local interconnect delay

Table 6–43. Stratix GX Reset & PLL Lock Time Parameter Descriptions (Part 1 of 2)

Symbol	Parameter
$t_{ANALOGRESETPW}$	Pulse width to power down analog circuits.
$t_{DIGITALRESETPW}$	Pulse width to reset digital circuits
$t_{TX\_PLL\_LOCK}$	The time it takes the `tx_pll` to lock to the reference clock.

Table 6–62. EP1SGX25 Column Pin Global Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.790		1.883		2.120		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.194	2.000	5.569	2.000	6.381	ns
$t_{INSUPLL}$	1.046		1.141		1.220		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.676	0.500	2.813	0.500	3.208	ns

Table 6–63. EP1SGX25 Row Pin Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.394		2.594		2.936		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.456	2.000	4.761	2.000	5.454	ns

Table 6–64. EP1SGX25 Row Pin Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.970		2.109		2.377		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.880	2.000	5.246	2.000	6.013	ns
$t_{INSUPLL}$	1.326		1.386		1.552		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

Table 6–65. EP1SGX25 Row Pin Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.963		2.108		2.379		ns
t_{INH}	0.000		0.000		0.000		ns

Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OUTCO}	2.000	5.365	2.000	5.775	2.000	6.621	ns
$t_{INSUPLL}$	1.126		1.186		1.352		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

External I/O Delay Parameters

External I/O delay timing parameters, both for I/O standard input and output adders and programmable input and output delays, are specified by speed grade, independent of device density.

Tables 6–72 through 6–77 show the adder delays associated with column and row I/O pins. If an I/O standard is selected other than LVTTL 24 mA with a fast slew rate, add the selected delay to the external t_{CO} and t_{SU} I/O parameters.

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		30		31		35	ps
1.8-V LVTTL		150		157		180	ps
1.5-V LVTTL		210		220		252	ps
GTL		220		231		265	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		120		126		144	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps

Table 6–73. Stratix GX I/O Standard Row Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
1.5-V HSTL class II		0		0		0	ps
1.8-V HSTL class I		70		73		83	ps
1.8-V HSTL class II		70		73		83	ps
LVDS *(1)*		40		42		48	ps
LVPECL *(1)*		–50		–53		–61	ps
3.3-V PCML *(1)*		330		346		397	ps
HyperTransport *(1)*		80		84		96	ps

Table 6–74. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		570		599		689	ps
	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	24 mA		0		0		0	ps
3.3-V LVTTL	4 mA		570		599		689	ps
	8 mA		350		368		423	ps
	12 mA		130		137		157	ps
	16 mA		70		74		85	ps
	24 mA		0		0		0	ps
2.5-V LVTTL	2 mA		830		872		1,002	ps
	8 mA		250		263		302	ps
	12 mA		140		147		169	ps
	16 mA		100		105		120	ps
1.8-V LVTTL	2 mA		420		441		507	ps
	8 mA		350		368		423	ps
	12 mA		350		368		423	ps
1.5-V LVTTL	2 mA		1,740		1,827		2,101	ps
	4 mA		1,160		1,218		1,400	ps
	8 mA		690		725		833	ps
GTL			–150		–157		–181	ps

Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTL	2 mA		830		872		1,002	ps
	8 mA		250		263		302	ps
	12 mA		140		147		169	ps
	16 mA		100		105		120	ps
1.8-V LVTTL	2 mA		1,510		1,586		1,824	ps
	8 mA		420		441		507	ps
	12 mA		350		368		423	ps
1.5-V LVTTL	2 mA		1,740		1,827		2,101	ps
	4 mA		1,160		1,218		1,400	ps
	8 mA		690		725		833	ps
CTT			50		53		61	ps
SSTL-3 class I			90		95		109	ps
SSTL-3 class II			–50		–52		–60	ps
SSTL-2 class I			100		105		120	ps
SSTL-2 class II			20		21		24	ps
LVDS *(1)*			–20		–21		–24	ps
LVPECL *(1)*			40		42		48	ps
PCML *(1)*			–60		–63		–73	ps
HyperTransport Technology *(1)*			70		74		85	ps

Table 6–76. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,911		2,011		2,312	ps
	4 mA		1,911		2,011		2,312	ps
	8 mA		1,691		1,780		2,046	ps
	12 mA		1,471		1,549		1,780	ps
	24 mA		1,341		1,412		1,623	ps

Table 6–76. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	4 mA		1,993		2,097		2,411	ps
	8 mA		1,773		1,866		2,145	ps
	12 mA		1,553		1,635		1,879	ps
	16 mA		1,493		1,572		1,807	ps
	24 mA		1,423		1,498		1,722	ps
2.5-V LVTTL	2 mA		2,631		2,768		3,182	ps
	8 mA		2,051		2,159		2,482	ps
	12 mA		1,941		2,043		2,349	ps
	16 mA		1,901		2,001		2,300	ps
1.8-V LVTTL	2 mA		4,632		4,873		5,604	ps
	8 mA		3,542		3,728		4,287	ps
	12 mA		3,472		3,655		4,203	ps
1.5-V LVTTL	2 mA		6,620		6,964		8,008	ps
	4 mA		6,040		6,355		7,307	ps
	8 mA		5,570		5,862		6,740	ps
GTL			1,191		1,255		1,442	ps
GTL+			1,231		1,297		1,90	ps
3.3-V PCI			1,111		1,171		1,346	ps
3.3-V PCI-X 1.0			1,111		1,171		1,346	ps
Compact PCI			1,111		1,171		1,346	ps
AGP 1×			1,311		1,381		1,587	ps
AGP 2×			1,311		1,381		1,587	ps
CTT			1,391		1,465		1,684	ps
SSTL-3 class I			1,431		1,507		1,732	ps
SSTL-3 class II			1,291		1,360		1,563	ps
SSTL-2 class I			1,912		2,013		2,314	ps
SSTL-2 class II			1,832		1,929		2,218	ps
SSTL-18 class I			3,097		3,260		3,748	ps
SSTL-18 class II			2,867		3,018		3,470	ps
1.5-V HSTL class I			4,916		5,174		5,950	ps
1.5-V HSTL class II			4,726		4,975		5,721	ps
1.8-V HSTL class I			3,247		3,417		3,929	ps
1.8-V HSTL class II			3,257		3,428		3,941	ps

Table 6–90. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		420	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		434	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* *(10)*	*(8)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration *(10)*	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		600 *(7)*	MHz