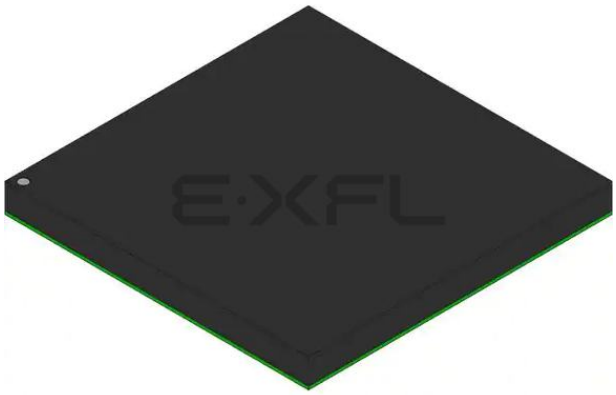
Altera - EP1SGX40GF1020C6 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx40gf1020c6

Table 1–2. Stratix GX Package Options & I/O Pin Counts (Part 2 of 2) *Note (1)*

Device	672-Pin FineLine BGA	1,020-Pin FineLine BGA
EP1SGX25D	455	607
EP1SGX25F		607
EP1SGX40D		624
EP1SGX40G		624

Note to Table 1–2:

(1) The number of I/O pins listed for each package includes dedicated clock pins and dedicated fast I/O pins. However, these numbers do not include high-speed or clock reference pins for high-speed I/O standards.

Table 1–3. Stratix GX FineLine BGA Package Sizes

Dimension	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00
Area (mm^2)	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

Table 1–4. Stratix GX Device Speed Grades

Device	672-Pin FineLine BGA	1,020-pin FineLine BGA
EP1SGX10	-5, -6, -7	
EP1SGX25	-5, -6, -7	-5, -6, -7
EP1SGX40		-5, -6, -7

High-Speed I/O Interface Functional Description

The Stratix GX device family supports high-speed serial transceiver blocks with CDR circuitry as well as source-synchronous interfaces. The channels on the right side of the device use an embedded circuit dedicated for receiving and transmitting high-speed serial data streams to and from the system board. These channels are clustered in a four-channel serial transceiver building block and deliver high-speed bidirectional point-to-point data transmissions to provide up to 3.1875 Gbps of full-duplex data transmission per channel. The channels on the left side of the device support source-synchronous data transfers at up to 1 Gbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards. Figure 1–1 shows the Stratix GX I/O blocks. The differential source-synchronous serial interface and the high-speed serial interface are described in the *Stratix GX Transceivers* chapter of the *Stratix GX Device Handbook, Volume 1*.

2. Stratix GX Transceivers

SGX51002-1.1

Transceiver Blocks

Stratix® GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

There are up to 20 transceiver channels available on a single Stratix GX device. Table 2–1 shows the number of transceiver channels available on each Stratix GX device.

Table 2–1. Stratix GX Transceiver Channels

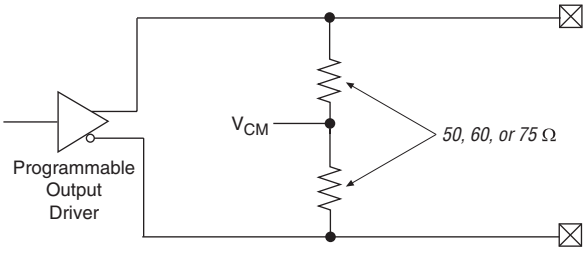
Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 2–1 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GIGE applications, in addition to channel bonding for XAUI applications.

Pre-emphasis percentage is defined as $V_{PP}/V_S - 1$, where V_{PP} is the differential emphasized voltage (peak-to-peak) and V_S is the differential steady-state voltage (peak-to-peak).

Programmable Transmitter Termination
The programmable termination can be statically set in the Quartus II software. The values are 100 Ω, 120 Ω, 150 Ω, and off. Figure 2–9 shows the setup for programmable termination.

Figure 2–9. Programmable Transmitter Termination



Receiver Path

This section describes the data path through the Stratix GX receiver (refer to Figure 2–2 on page 2–4). Data travels through the Stratix GX receiver via the following modules:

- Input buffer
- Clock Recovery Unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

Receiver Input Buffer

The Stratix GX receiver input buffer supports the 1.5-V PCML I/O standard at a rate up to 3.1875 Gbps. Additional I/O standards, LVDS, 3.3-V PCML, and LVPECL can be supported when AC coupled. The common mode of the input buffer is 1.1 V. The receiver can support Stratix GX-to-Stratix GX DC coupling.

interconnects can drive and be driven by all types of architecture blocks similar to C4 interconnects. C8 interconnects can drive each other to extend their range as well as R8 interconnects for column-to-column connections. C8 interconnects are faster than two C4 interconnects.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[7..0]`.

Figure 4–14. M512 RAM Block Control Signals

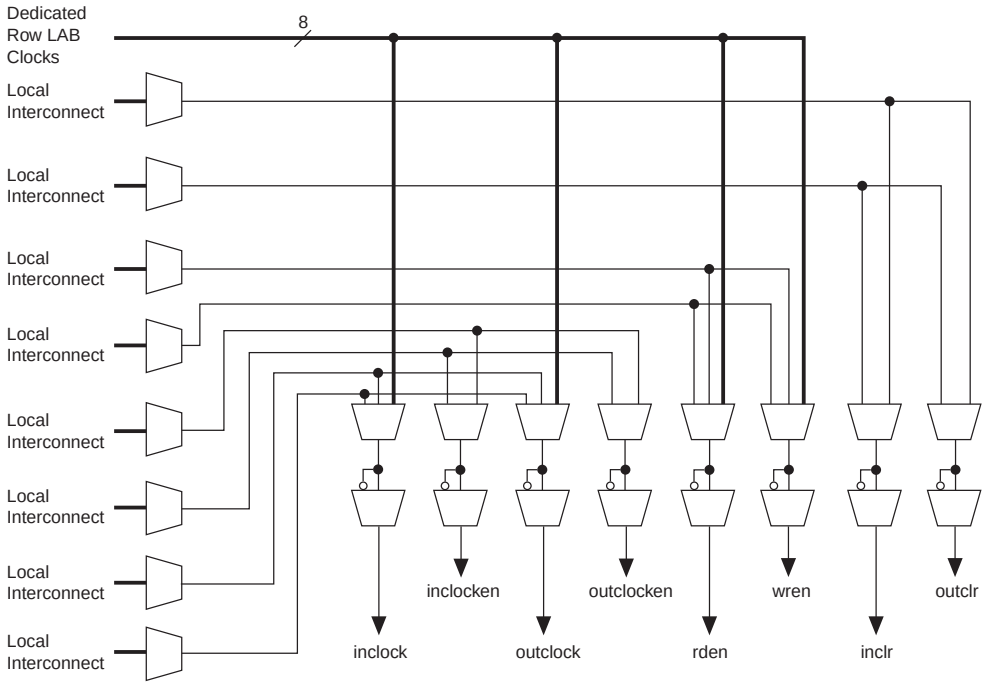


Table 4–8. M-RAM Block Configurations (True Dual-Port)				
Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the WREN signal, which sets the ports into either read or write modes. There is no separate read enable (RE) signal.

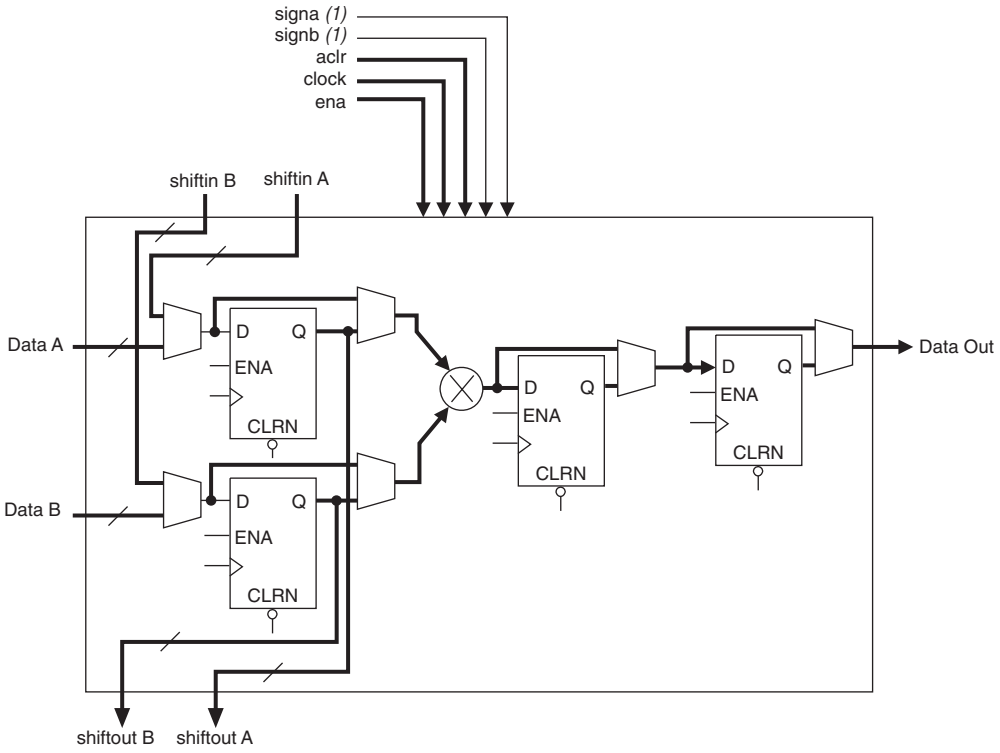
Writing into RAM is controlled by both the WREN and byte enable (byteena) signals for each port. The default value for the byteena signal is high, in which case writing is controlled only by the WREN signal. The byte enables are available for the ×18, ×36, and ×72 modes. In the ×144 simple dual-port mode, the two sets of byteena signals (byteena_a and byteena_b) are combined to form the necessary 16 byte enables. Tables 4–9 and 4–10 summarize the byte selection.

Table 4–9. Byte Enable for M-RAM Blocks Notes (1), (2)			
byteena[3..0]	datain ×18	datain ×36	datain ×72
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 4–24 and 4–25 show the memory block in input/output clock mode.

Figure 4–34. Simple Multiplier Mode



Note to Figure 4–34:
(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 4–35 shows the 36 × 36-bit multiply mode.

Clock Multiplication & Division

Each Stratix GX device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale divider, n, and one multiply divider, m, per PLL, with a range of 1 to 512 on each. There are two post-scale dividers (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 512. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix GX device enhanced PLLs support a flexible clock switchover capability. Figure 4–52 shows a block diagram of the switchover circuit.The switchover circuit is configurable, so you can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL class I and II
- 1.8-V HSTL Class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II
- CTT

Table 4–27 describes the I/O standards supported by Stratix GX devices.

Table 4–27. Stratix GX Supported I/O Standards (Part 1 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X 1.0	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	0.75	1.5	0.75
Differential SSTL *(2)*	Differential	1.25	2.5	1.25
GTL	Voltage-referenced	0.8	N/A	1.20
GTL+	Voltage-referenced	1.0	N/A	1.5
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25

However, there is additional resistance present between the device ball and the input of the receiver buffer, as shown in Figure 4–71. This resistance is because of package trace resistance (which can be calculated as the resistance from the package ball to the pad) and the parasitic layout metal routing resistance (which is shown between the pad and the intersection of the on-chip termination and input buffer).

Figure 4–71. Differential Resistance of LVDS Differential Pin Pair (R_D)

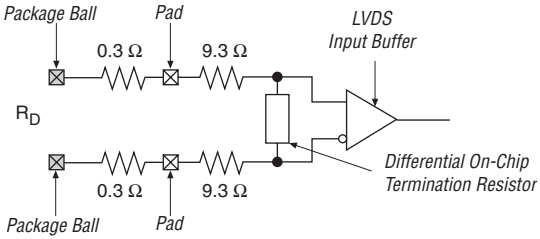


Table 4–31 defines the specification for internal termination resistance for commercial devices.

Table 4–31. Differential On-Chip Termination

Symbol	Description	Conditions	Resistance			Unit
			Min	Typ	Max	
R_D *(2)*	Internal differential termination for LVDS	Commercial *(1)*, *(3)*	110	135	165	Ω
		Industrial *(2)*, *(3)*	100	135	170	Ω

Notes to Table 4–31:

(1) Data measured over minimum conditions (T_j = 0 C, V_{CCIO} +5%) and maximum conditions (T_j = 85 C, V_{CCIO} = –5%).

(2) Data measured over minimum conditions (T_j = –40 C, V_{CCIO} +5%) and maximum conditions (T_j = 100 C, V_{CCIO} = –5%).

(3) LVDS data rate is supported for 840 Mbps using internal differential termination.

MultiVolt I/O Interface

The Stratix GX architecture supports the MultiVolt I/O interface feature, which allows Stratix GX devices in all packages to interface with systems of different supply voltages.

The Stratix GX VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V,

2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 4–32 summarizes Stratix GX MultiVolt I/O support.

Table 4–32. Stratix GX MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal *(5)*					Output Signal *(6)*				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*		✓				
1.8	✓ *(2)*	✓	✓ *(2)*	✓ *(2)*		✓ *(3)*	✓			
2.5			✓	✓		✓ *(3)*	✓ *(3)*	✓		
3.3			✓ *(2)*	✓	✓ *(4)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 4–32:

(1) To drive inputs higher than V_{CCIO} but less than 4.1 V, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent V_I from rising above 4.0 V.

(2) The input pin current may be slightly higher than the typical value.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix GX device to drive out, a receiving device powered at a different level can still interface with the Stratix GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix GX devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.

(5) This is the external signal that is driving the Stratix GX device.

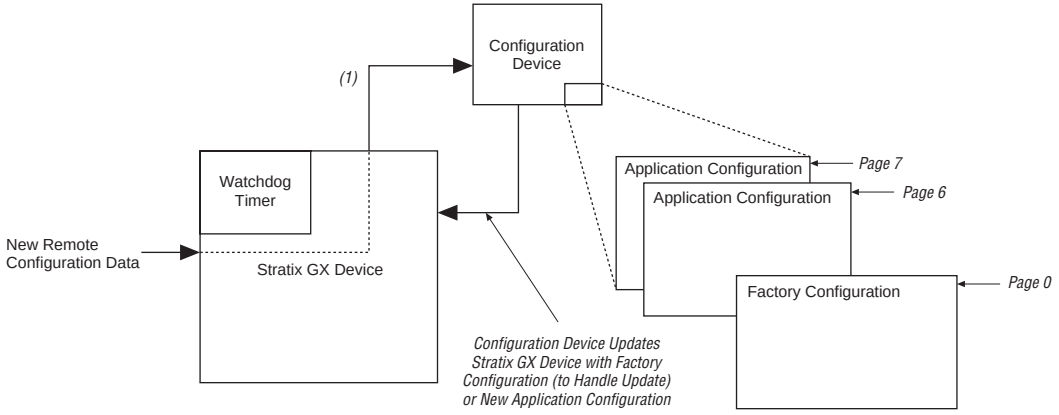
(6) This represents the system voltage that Stratix GX supports when a VCCIO pin is connected to a specific voltage level. For example, when VCCIO is 3.3 V and if the I/O standard is LVTTL/LVCMOS, the output high of the signal coming out from Stratix GX is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Power Sequencing & Hot Socketing

Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the VCCIO and VCCINT power supplies may be powered in any order.

Signals can be driven into Stratix GX devices before and during power up without damaging the device. In addition, Stratix GX devices do not drive out during power up. Once operating conditions are reached and the device is configured, Stratix GX devices operate as specified by the user. For more information, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

Figure 5–1. Stratix GX Device Remote Update



Note to Figure 5–1:

(1) When the Stratix GX device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Figure 5–5. Temperature Versus Temperature-Sensing Diode Voltage

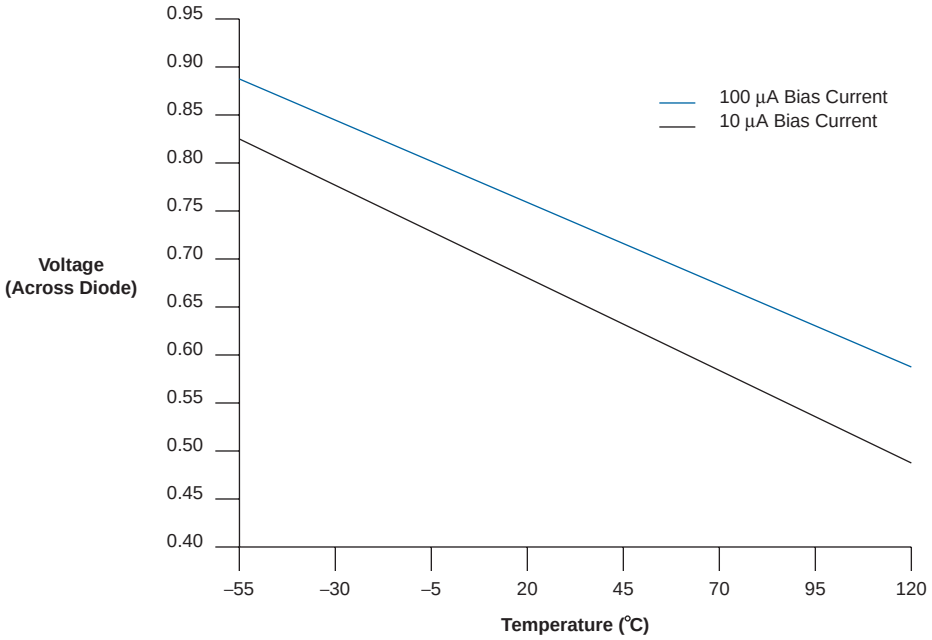


Table 6–2. Stratix GX Device Recommended Operating Conditions (Part 2 of 2) *Note (7), (12), (13)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C

Table 6–3. Stratix GX Device DC Operating Conditions *Note (12)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 6–4. Stratix GX Transceiver Block Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	2.4	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
V_{CCG}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V
Receiver input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V
`refclkb` input voltage	V_{ICM} ±V_{ID} single / 2	Commercial and industrial		1.675 *(10)*, *(13)*	V

Table 6–9. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 6–10. 2.5-V I/O Specifications *Note (1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OH} = 1 mA		0.4	V
		I_{OH} = 2 to 16 mA *(1)*		0.7	V

Table 6–11. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(1)*		0.45	V

Table 6–12. 1.5-V I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	0.75 × V_{CCIO}		V

Table 6–29. 1.5-V HSTL Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Table 6–30. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Table 6–31. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 6–32. CTT I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Tables 6–54 through 6–59 show the external timing parameters on column and row pins for EP1SGX10 devices.

Table 6–54. EP1SGX10 Column Pin Fast Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.245		2.332		2.666		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.597	2.000	4.920	2.000	5.635	ns

Table 6–55. EP1SGX10 Column Pin Regional Clock External I/O Timing Parameters							
Symbol	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.114		2.218		2.348		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.728	2.000	5.078	2.000	6.004	ns
$t_{INSUPLL}$	1.035		0.941		1.070		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.629	0.500	2.769	0.500	3.158	ns

Table 6–83. Stratix GX Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins (Part 2 of 2)				
I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.8 V	422	422	390	MHz
1.5 V	422	422	390	MHz
LVCMOS	422	422	390	MHz
GTL	300	250	200	MHz
GTL+	300	250	200	MHz
SSTL-3 class I	400	350	300	MHz
SSTL-3 class II	400	350	300	MHz
SSTL-2 class I	400	350	300	MHz
SSTL-2 class II	400	350	300	MHz
SSTL-18 class I	400	350	300	MHz
SSTL-18 class II	400	350	300	MHz
1.5-V HSTL class I	400	350	300	MHz
1.5-V HSTL class II	400	350	300	MHz
1.8-V HSTL class I	400	350	300	MHz
1.8-V HSTL class II	400	350	300	MHz
3.3-V PCI	422	422	390	MHz
3.3-V PCI-X 1.0	422	422	390	MHz
Compact PCI	422	422	390	MHz
AGP 1×	422	422	390	MHz
AGP 2×	422	422	390	MHz
CTT	300	250	200	MHz
Differential HSTL	400	350	300	MHz
LVDS	645	645	640	MHz
LVPECL	645	645	640	MHz
PCML	300	275	275	MHz
HyperTransport technology	645	645	640	MHz

Tables 6–84 and 6–85 show the maximum output clock rate for column and row pins in Stratix GX devices.

Table 6–84. Stratix GX Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 1 of 2)				
I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	350	300	250	MHz
2.5 V	350	300	300	MHz