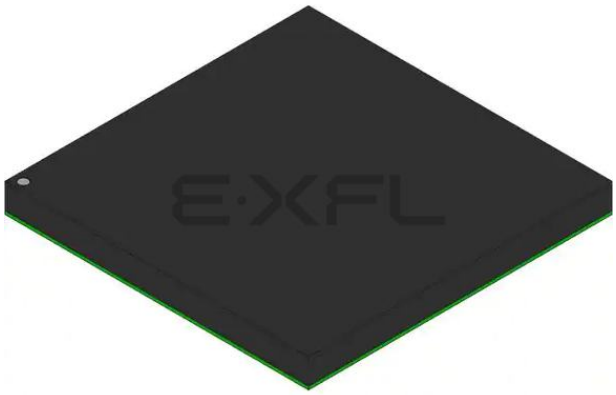

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

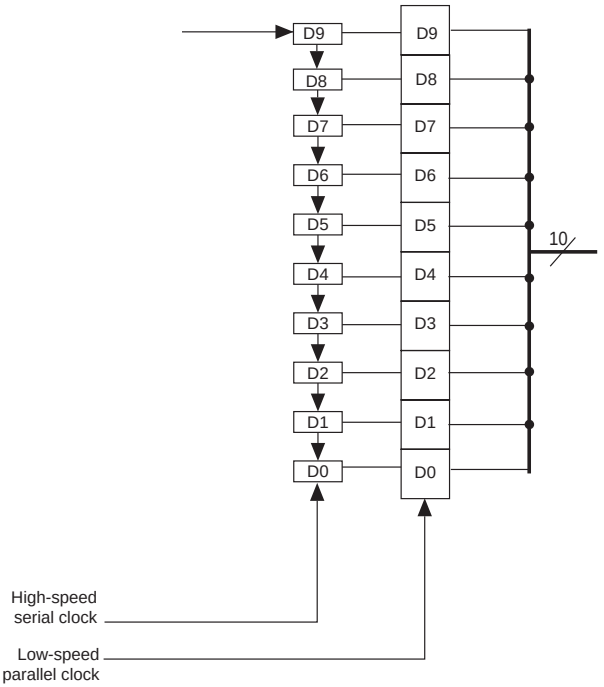
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1sgx40gf1020c7n

Deserializer (Serial-to-Parallel Converter)

The deserializer converts the serial stream into a parallel 8- or 10-bit data bus. The deserializer receives the least significant bit first. Figure 2–14 is a diagram of the deserializer.

Figure 2–14. Deserializer



Word Aligner

The word aligner aligns the incoming data based on the specific byte boundaries. The word aligner has three customizable modes of operation: bit-slip mode, 16-bit mode, and 10-bit mode, the last of which is available for the basic and SONET modes. The word aligner also has two non-customizable modes of operation, which are the XAUI and GIGE modes.

Figure 2–15 shows the word aligner in bit-slip mode.

High-Speed Serial Bus Protocols

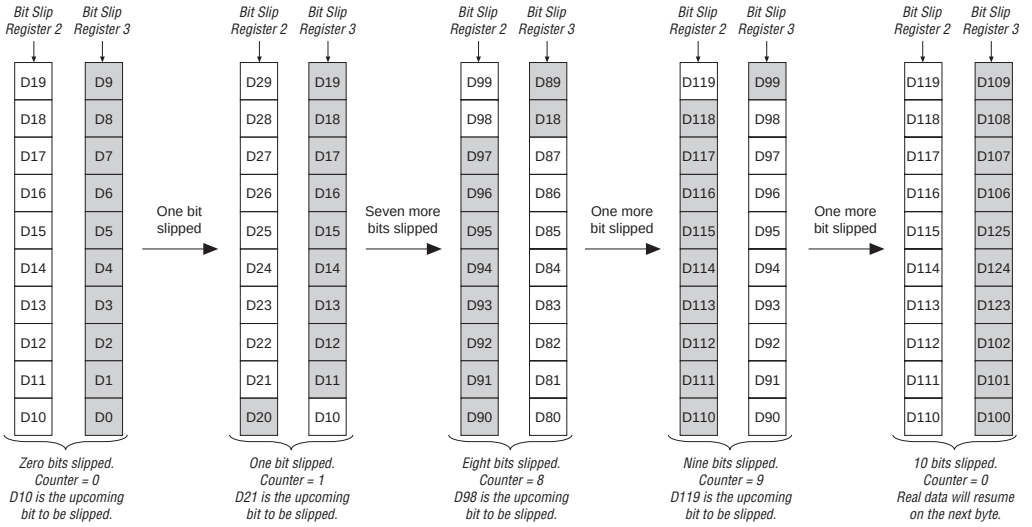
With wide, serial data rate range, Stratix GX devices can support multiple, high-speed serial bus protocols. Table 2–12 shows some of the protocols that Stratix GX devices can support.

Table 2–12. High-Speed Serial Bus Protocols

Bus Transfer Protocol	Stratix GX (Gbps) (Supports up to 3.1875 Gbps)
SONET backplane	2.488
10 Gigabit Ethernet XAUI	3.125
10 Gigabit fibre channel	3.1875
InfiniBand	2.5
Fibre channel (1G, 2G)	1.0625, 2.125
Serial RapidIO™	1.25, 2.5, 3.125
PCI Express	2.5
SMPTE 292M	1.485

The DPA data-realignment circuitry allows further realignment beyond what the *J* multiplication factor allows. You can set the *J* multiplication factor to be 8 or 10. However, because data must be continuously clocked in on each low-speed clock cycle, the upcoming bit to be realigned and previous *n* –1 bits of data are selected each time the data realignment logic's counter passes *n* –1. At this point the data is selected entirely from bit-slip register 3 (see Figure 3–11) as the counter is reset to 0. The logic array receives a new valid byte of data on the next divided low speed clock cycle. Figure 3–11 shows the data realignment logic output selection from data in the data realignment register 2 and data realignment register 3 based on its current counter value upon continuous request of data slipping from the logic array.

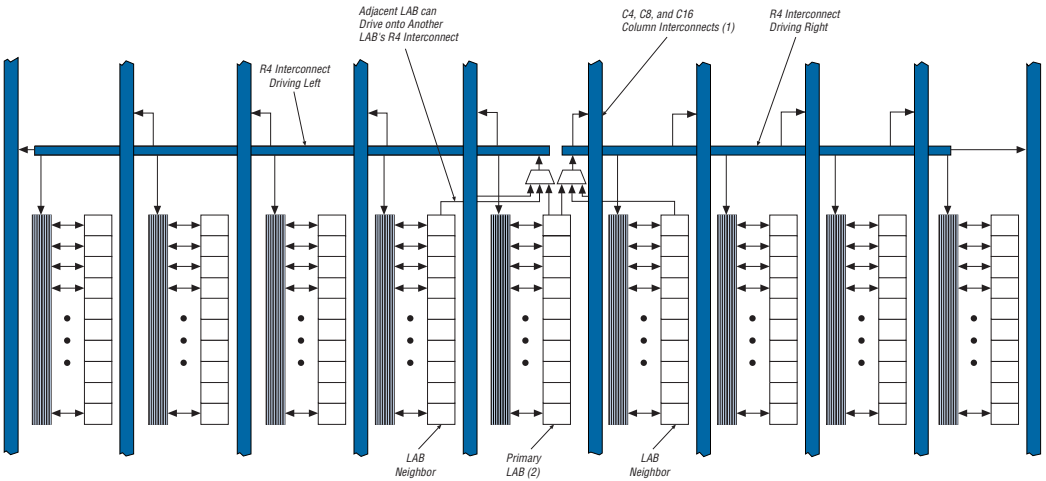
Figure 3–11. DPA Data Realigner



Use the `rx_channel_data_align` signal within the device to activate the data realigner. You can use internal logic or an external pin to control the `rx_channel_data_align` signal. To ensure the rising edge of the `rx_channel_data_align` signal is latched into the control logic, the `rx_channel_data_align` signal should stay high for at least two low-frequency clock cycles.

can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 4–8. R4 Interconnect Connections



Notes to Figure 4–8:
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.

The R8 interconnects span eight LABs, M512 or M4K RAM blocks, or DSP blocks to the right or left from a source LAB. These resources are used for fast row connections in an eight-LAB region. Every LAB has its own set of R8 interconnects to drive either left or right. R8 interconnect connections between LABs in a row are similar to the R4 connections shown in Figure 4–8, with the exception that they connect to eight LABs to the right or left, not four. Like R4 interconnects, R8 interconnects can drive and be driven by all types of architecture blocks. R8 interconnects can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth

Table 4–2. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Configurations	512 ×1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 4–2:

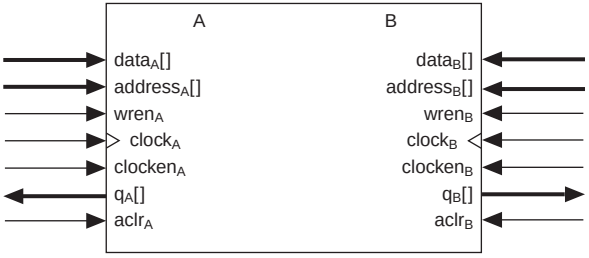
(1) See the *DC & Switching Characteristics* chapter of the *Stratix GX Device Handbook, Volume 1* for maximum performance information.

(2) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix GX device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Modes

TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K and M-RAM memory blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 4–11 shows true dual-port memory.

Figure 4–11. True Dual-Port Memory Configuration



In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write and can either read old data before the write

M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO RAM

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as 64K × 8 (or 64K × 9 bits), 32K × 16 (or 32K × 18 bits), 16K × 32 (or 16K × 36 bits), 8K × 64 (or 8K × 72 bits), and 4K × 128 (or 4K × 144 bits). The 4K × 128 configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. Tables 4–7 and 4–8 summarize the possible M-RAM block configurations:

Table 4–7. M-RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port				
	64K × 9	32K × 18	16K × 36	8K × 72	4K × 144
64K × 9	✓	✓	✓	✓	
32K × 18	✓	✓	✓	✓	
16K × 36	✓	✓	✓	✓	
8K × 72	✓	✓	✓	✓	
4K × 144					✓

Figure 4–21. M-RAM Row Unit Interface to Interconnect

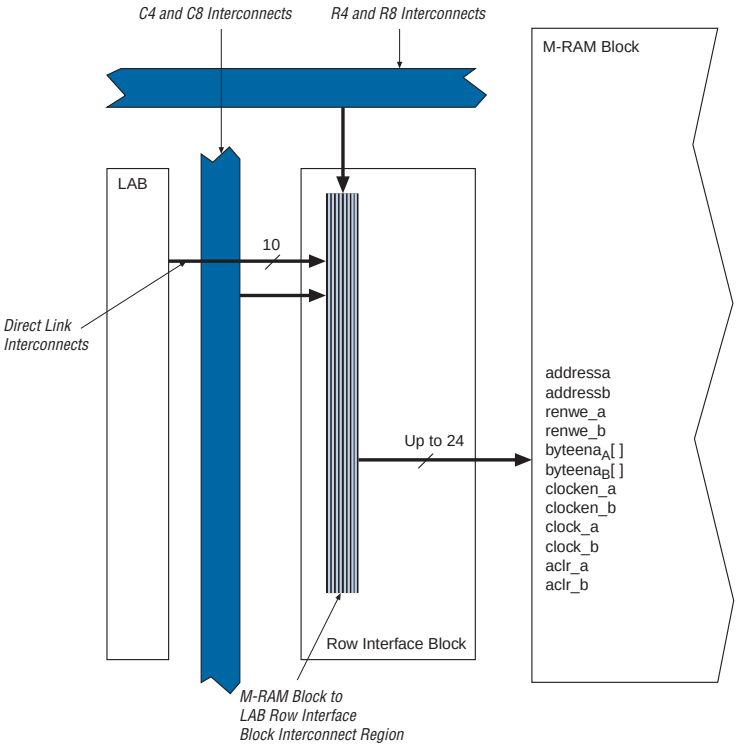
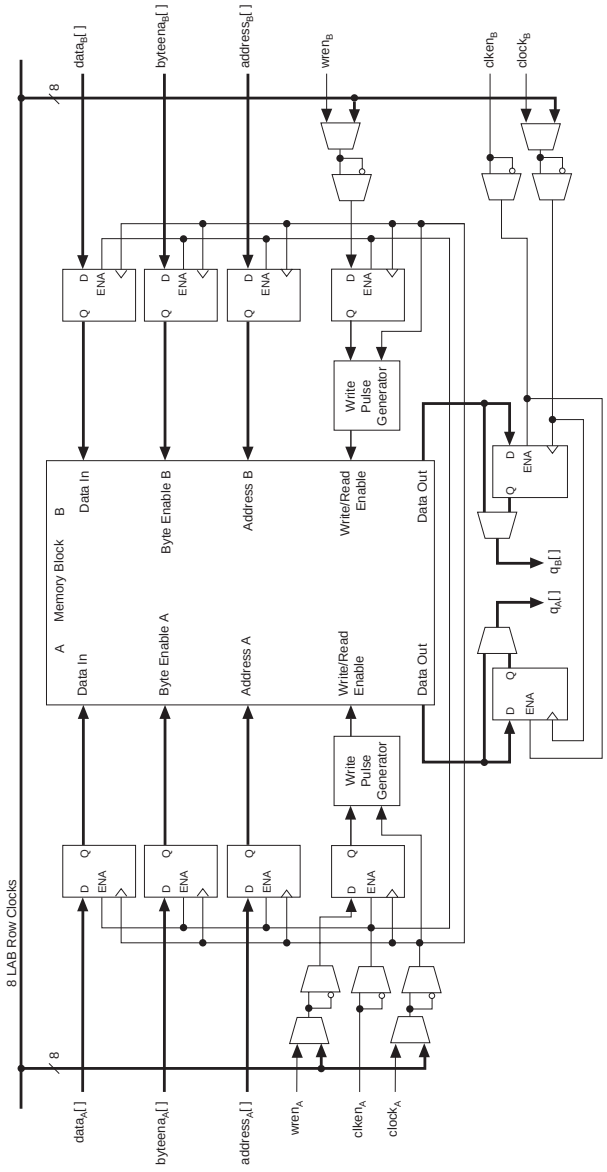
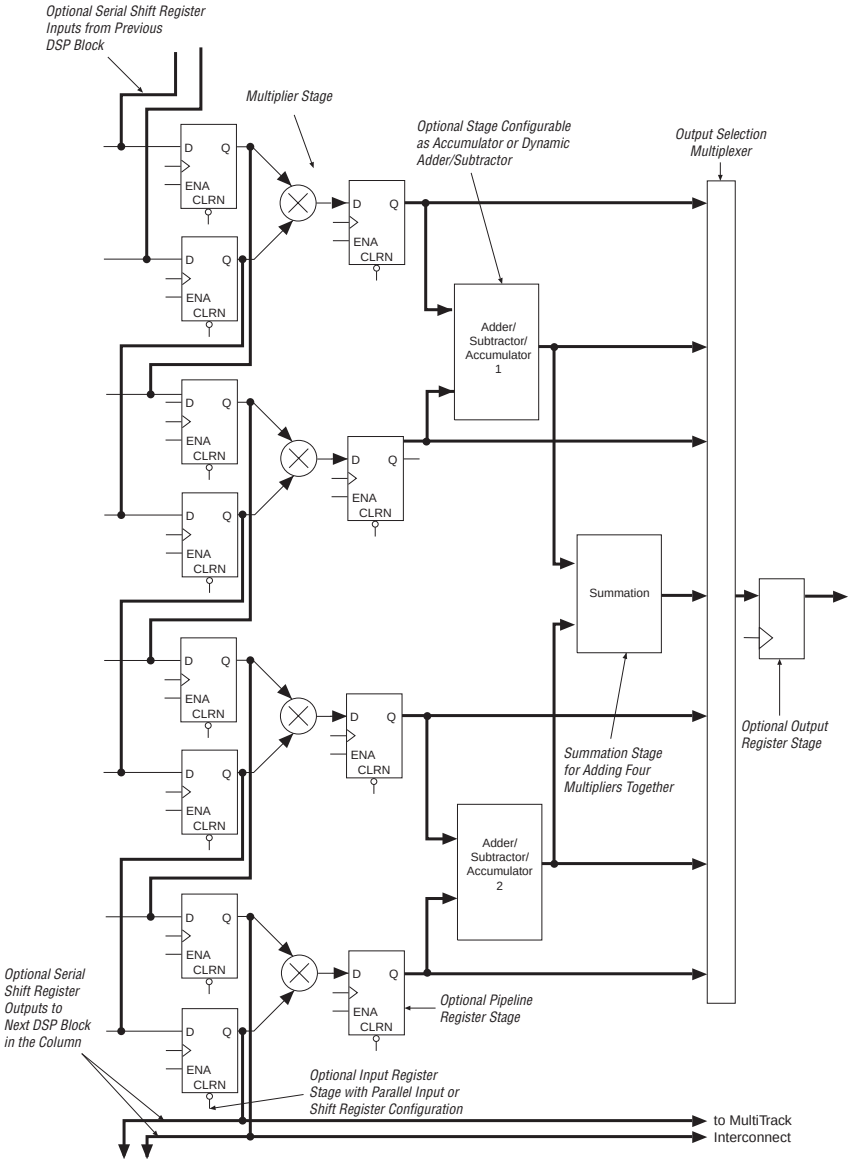


Figure 4–24. Input/Output Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 4–24:
(1) All registers shown have asynchronous clear ports.

Figure 4–29. DSP Block Diagram for 18 × 18-Bit Configuration



For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (that is, implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 4–15 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 4–15. Multiplier Size & Configurations per DSP block

DSP Block Mode	9 × 9	18 × 18	36 × 36 *(1)*
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

Note to Table 4–15:
(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP Block Interface

Stratix GX device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

The DSP block is divided into eight block units that interface with eight LAB rows on the left and right. Each block unit can be considered half of an 18 × 18-bit multiplier sub-block with 18 inputs and 18 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 10 direct link interconnects from the LAB to the left or right of the DSP block in the same row. All row and column routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Nine outputs from the DSP block can drive to the left LAB through direct link interconnects and nine can drive to the right LAB though direct link interconnects. All 18 outputs can drive to all types of row and column routing. Outputs can drive right- or left-column routing. Figures 4–39 and 4–40 show the DSP block interfaces to LAB rows.

Figure 4–39. DSP Block Interconnect Interface

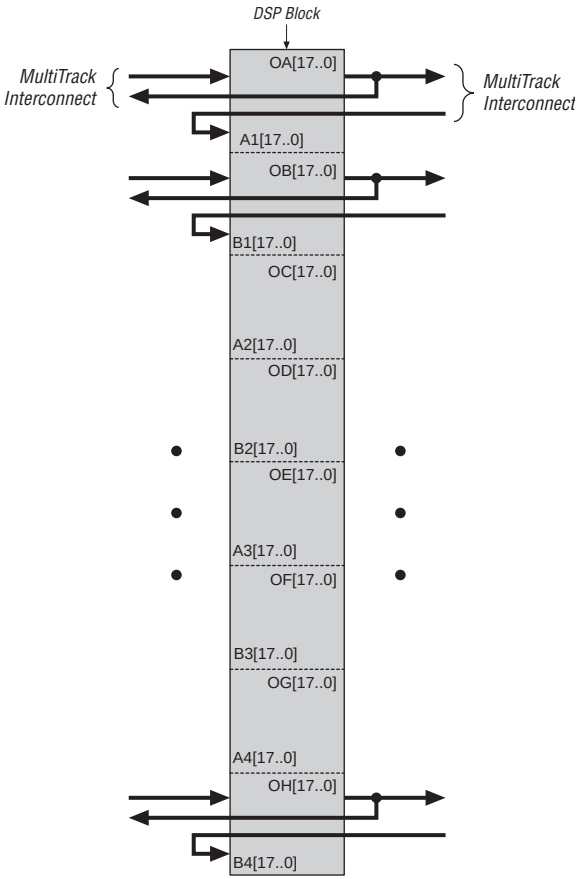
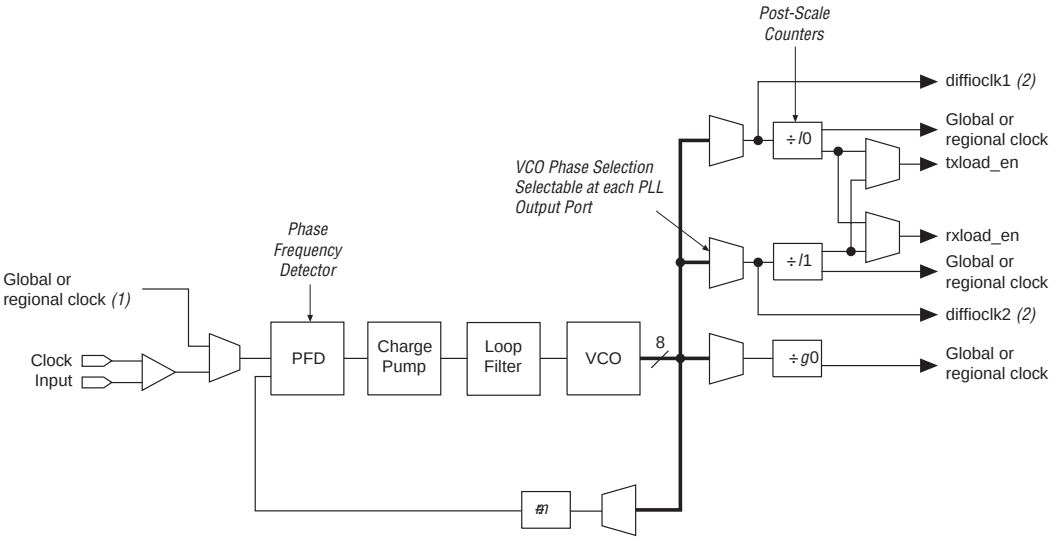


Figure 4–57. Stratix GX Device Fast PLL



Notes to Figure 4–57:

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

The Stratix GX device's fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output

Phase Shifting

Stratix GX device fast PLLs have advanced clock shift capability that enables programmable phase shifts. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 150 to 400 ps. This resolution is a function of the VCO period.

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

For more information on high-speed differential I/O support, see the *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

The IOE in Stratix GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 4–58 shows the Stratix GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Table 6–12. 1.5-V I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(1)*		0.25 × V_{CCIO}	V

Note to Tables 6–8 through 6–12:

(1) Drive strength is programmable according to values in found in the *Stratix GX Architecture* chapter of the *Stratix GX Device Handbook, Volume 1*.

Figures 6–1 through 6–3 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 6–1. Receiver Input Waveforms for Differential I/O Standards

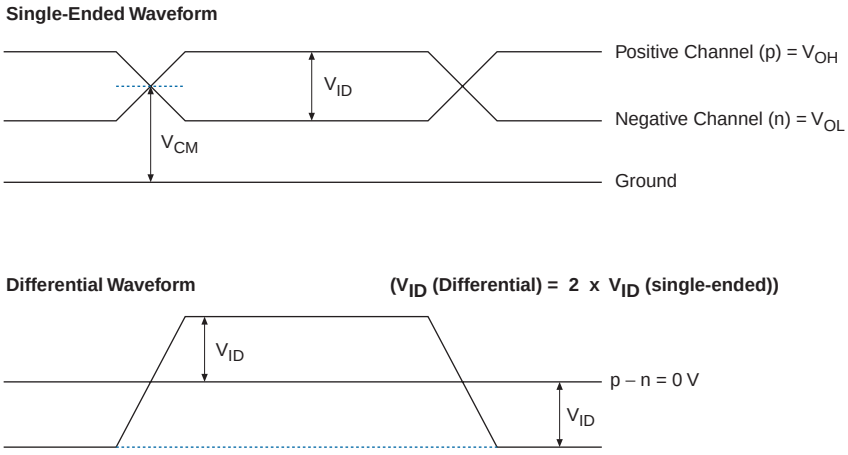


Table 6–65. EP1SGX25 Row Pin Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OUTCO}	2.000	4.887	2.000	5.247	2.000	6.011	ns
$t_{INSUPLL}$	1.326		1.386		1.552		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

Tables 6–66 through 6–71 show the external timing parameters on column and row pins for EP1SGX40 devices.

Table 6–66. EP1SGX40 Column Pin Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.704		2.912		3.235		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.060	2.000	5.432	2.000	6.226	ns

Table 6–67. EP1SGX40 Column Pin Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.467		2.671		3.011		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.255	2.000	5.673	2.000	6.501	ns
$t_{INSUPLL}$	1.254		1.259		1.445		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.610	0.500	2.751	0.500	3.134	ns

Table 6–68. EP1SGX40 Column Pin Global Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.033		2.184		2.451		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	5.689	2.000	6.116	2.000	7.010	ns
$t_{INSUPLL}$	1.228		1.278		1.415		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.594	0.500	2.732	0.500	3.113	ns

Table 6–69. EP1SGX40 Row Pin Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.450		2.662		3.046		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.880	2.000	5.241	2.000	6.004	ns

Table 6–70. EP1SGX40 Row Pin Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.398		2.567		2.938		ns
t_{INH}	0.000		0.000		0.000		ns
t_{OUTCO}	2.000	4.932	2.000	5.336	2.000	6.112	ns
$t_{INSUPLL}$	1.126		1.186		1.352		ns
t_{INHPLL}	0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	0.500	2.304	0.500	2.427	0.500	2.765	ns

Table 6–71. EP1SGX40 Row Pin Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.965		2.128		2.429		ns
t_{INH}	0.000		0.000		0.000		ns

Table 6–75. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)

Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
2.5-V LVTTL	2 mA		830		872		1,002	ps
	8 mA		250		263		302	ps
	12 mA		140		147		169	ps
	16 mA		100		105		120	ps
1.8-V LVTTL	2 mA		1,510		1,586		1,824	ps
	8 mA		420		441		507	ps
	12 mA		350		368		423	ps
1.5-V LVTTL	2 mA		1,740		1,827		2,101	ps
	4 mA		1,160		1,218		1,400	ps
	8 mA		690		725		833	ps
CTT			50		53		61	ps
SSTL-3 class I			90		95		109	ps
SSTL-3 class II			–50		–52		–60	ps
SSTL-2 class I			100		105		120	ps
SSTL-2 class II			20		21		24	ps
LVDS *(1)*			–20		–21		–24	ps
LVPECL *(1)*			40		42		48	ps
PCML *(1)*			–60		–63		–73	ps
HyperTransport Technology *(1)*			70		74		85	ps

Table 6–76. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,911		2,011		2,312	ps
	4 mA		1,911		2,011		2,312	ps
	8 mA		1,691		1,780		2,046	ps
	12 mA		1,471		1,549		1,780	ps
	24 mA		1,341		1,412		1,623	ps

Table 6–86. High-Speed Timing Specifications & Definitions (Part 2 of 2)	
High-Speed Timing Specification	**Definitions**
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. SW = t_{SW} (max) – t_{SW} (min).
Input jitter (peak-to-peak)	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 6–87 shows the high-speed I/O timing specifications for Stratix GX devices.

Table 6–87. High-Speed I/O Specifications (Part 1 of 4) Notes (1), (2)											
Symbol	**Conditions**	**-5 Speed Grade**			**-6 Speed Grade**			**-7 Speed Grade**			**Unit**
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
f_{HSCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) f_{HSCLK} = f_{HSDR} / W	*W* = 1 to 30 for ≤717 Mbps W = 2 to 30 for > 717 Mbps	10		717	10		717	10		624	MHz
f_{HSCLK_DPA}		74		717	74		717	74		717	MHz

Table 6–87. High-Speed I/O Specifications (Part 3 of 4) *Notes (1), (2)*

Symbol	Conditions			-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA Lock Time	Standard	Training Pattern	Transition Density										
	SPI-4, CSIX	0000 0000 0011 1111 1111	10%	256			256			256			*(4)*
	Rapid IO	0000 1111	25%	256			256			256			*(4)*
		1001 0000	50%	256			256			256			*(4)*
	Misc	1010 1010	100 %	256			256			256			*(4)*
		0101 0101		256			256			256			*(4)*
TCCS	All					200			200			300	ps
SW	PCML (J = 4, 7, 8, 10)			750			750			800			ps
	PCML (J = 2)			900			900			1,200			ps
	PCML (J = 1)			1,500			1,500			1,700			ps
	LVDS and LVPECL (J = 1)			500			500			550			ps
	LVDS, LVPECL, HyperTransport technology (J = 2 through 10)			440			440			500			ps
Input jitter tolerance (peak-to-peak)	All					250			250			250	ps
Output jitter (peak-to-peak)	All					160			160			200	ps
Output t_{RISE}	LVDS			80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology			110	170	200	110	170	200	120	170	200	ps
	LVPECL			90	130	150	90	130	150	100	135	150	ps
	PCML			80	110	135	80	110	135	80	110	135	ps