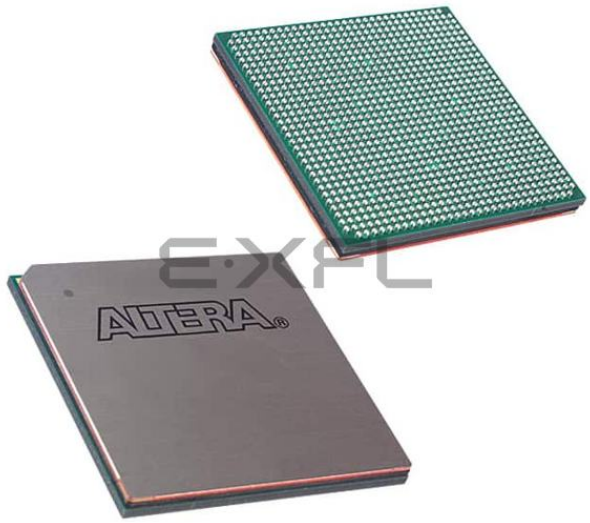

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx40gf1020i6

Revision History

The table below shows the revision history for Chapters 1 through 7.

Chapter(s)	Date / Version	Changes Made	Comments
1	February 2005, v1.0	Initial Release.	
2	June 2006, v1.1	• Updated "Serial Loopback" section. • Updated Figures 2–1 through 2–3. • Updated Figure 2–13. • Updated Figures 2–26 and 2–27.	
	February 2005, v1.0	Initial Release.	
3	August 2005, v1.1	Added Note (3) to Figure 3-7.	
4	February 2005, v1.0	Initial Release.	
5	February 2005, v1.0	Initial Release.	
6	June 2006, v1.2	• Updated "Operating Conditions" section. • Updated Table 6–4. • Updated note 3 in Table 6–6. • Added note 12 in Table 6–7. • Updated Figure 6–1. • Added Figure 6–2. • Updated Tables 6–13 through 6–16.	• Changed V_{OD} to V_{ID} for receiver input voltage and `refclkb` input voltage in Table 6–4. • Changed value for undershoot during transition from -0.5 V to -2.0 V in note 3 of Table 6–6. • Changed value of V_{OCM} from mV to V in Table 6–15. • Changed unit value of W to Ω.
	August 2005, v1.1	Updated Tables 6-7 and 6-50.	
7	February 2005, v1.0	Initial Release.	

2. Stratix GX Transceivers

SGX51002-1.1

Transceiver Blocks

Stratix® GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

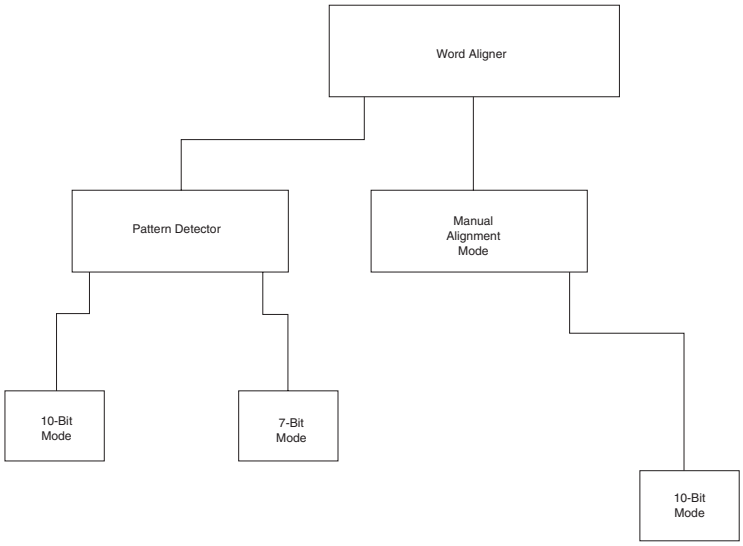
There are up to 20 transceiver channels available on a single Stratix GX device. Table 2–1 shows the number of transceiver channels available on each Stratix GX device.

Table 2–1. Stratix GX Transceiver Channels

Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 2–1 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GIGE applications, in addition to channel bonding for XAUI applications.

Figure 2–17. Word Aligner in 10-Bit Mode



In the 10-bit mode, the word aligner automatically aligns the user's predefined 10-bit alignment pattern. The pattern detector can detect the full 10-bit pattern or only the lower seven bits of the pattern. The word aligner and pattern detector detect both the positive and the negative disparity of the pattern. A user-controlled enable port is available for the word aligner.

The 10-bit mode is available only for the Custom mode.

Figure 2–18 shows the word aligner in XAUI mode.

3. Source-Synchronous Signaling With DPA

SGX51003-1.1

Introduction

Expansion in the telecommunications market and growth in Internet use requires systems to move more data faster than ever. To meet this demand, rely on solutions such as differential signaling and emerging high-speed interface standards including RapidIO, POS-PHY 4, SFI-4, or XSBI.

These new protocols support differential data rates up to 1 Gbps and higher. At these high data rates, it becomes more challenging to manage the skew between the clock and data signals. One solution to this challenge is to use CDR to eliminate skew between data channels and clock signals. Another potential solution, DPA, is beginning to be incorporated into some of these protocols.

The source-synchronous high-speed interface in Stratix GX devices is a dedicated circuit embedded into the PLD allowing for high-speed communications. The *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2* provides information on the high-speed I/O standard features and functions of the Stratix GX device.

Stratix GX I/O Banks

Stratix GX devices contain 17 I/O banks. I/O banks one and two support high-speed LVDS, LVPECL, and 3.3-V PCML inputs and outputs. These two banks also incorporate an embedded dynamic phase aligner within the source-synchronous interface (see Figure 3–8 on page 3–10). The dynamic phase aligner corrects for the phase difference between the clock and data lines caused by skew. The dynamic phase aligner operates automatically and continuously without requiring a fixed training pattern, and allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-clock skew.

Principles of SERDES Operation

Stratix GX devices support source-synchronous differential signaling up to 1 Gbps in DPA mode, and up to 840 Mbps in non-DPA mode. Serial data is transmitted and received along with a low-frequency clock. The PLL can multiply the incoming low-frequency clock by a factor of 1 to 10. The SERDES factor *J* can be 8 or 10 for the DPA mode, or 4, 7, 8, or 10 for all other modes. The SERDES factor does not have to equal the clock

have four dedicated fast PLLs for clock multiplication. Table 3–3 shows the maximum number of channels in each Stratix GX device that support DPA.

Table 3–3. Stratix GX Source-Synchronous Differential I/O Resources

Device	Fast PLLs	Pin Count	Receiver Channels *(1)*	Transmitter Channels *(1)*	Receiver & Transmitter Channel Speed (Gbps) *(2)*	LEs
EP1SGX10C	2 *(3)*	672	22	22	1	10,570
EP1SGX10D	2 *(3)*	672	22	22	1	10,570
EP1SGX25C	2	672	39	39	1	25,660
EP1SGX25D	2	672	39	39	1	25,660
		1,020	39	39	1	25,660
EP1SGX25F	2	1,020	39	39	1	25,660
EP1SGX40D	4 *(4)*	1,020	45	45	1	41,250
EP1SGX40G	4 *(4)*	1,020	45	45	1	41,250

Notes to Table 3–3:

(1) This is the number of receiver or transmitter channels in the source-synchronous (I/O bank 1 and 2) interface of the device.

(2) Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps.

(3) One of the two fast PLLs in EP1SGX10C and EP1SGX10D devices supports DPA.

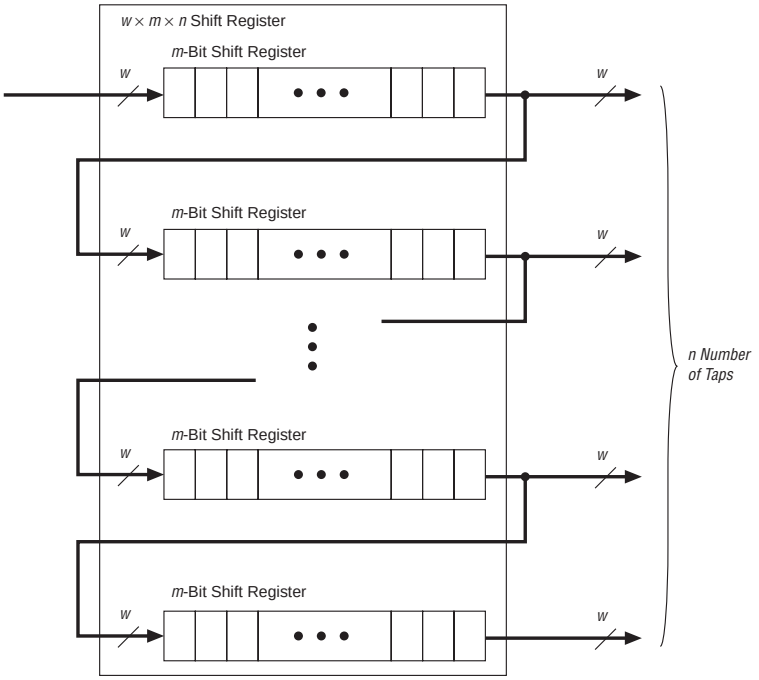
(4) Two of the four fast PLLs in EP1SGX40D and EP1SGX40G devices support DPA

The receiver and transmitter channels are interleaved so that each I/O row in I/O banks 1 and 2 of the device has one receiver channel and one transmitter channel per row. Figures 3–6 and 3–7 show the fast PLL and channels with DPA layout in EP1SGX10, EP1SGX25, and EP1SGX40 devices. In EP1SGX10 devices, only fast PLL 2 supports DPA operations.

RAM block and 4,608 bits for the M4K RAM block. The total number of shift register outputs (number of taps n × width w) must be less than the maximum data width of the RAM block (18 for M512 blocks, 36 for M4K blocks). To create larger shift registers, the memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 4–13 shows the TriMatrix memory block in the shift register mode.

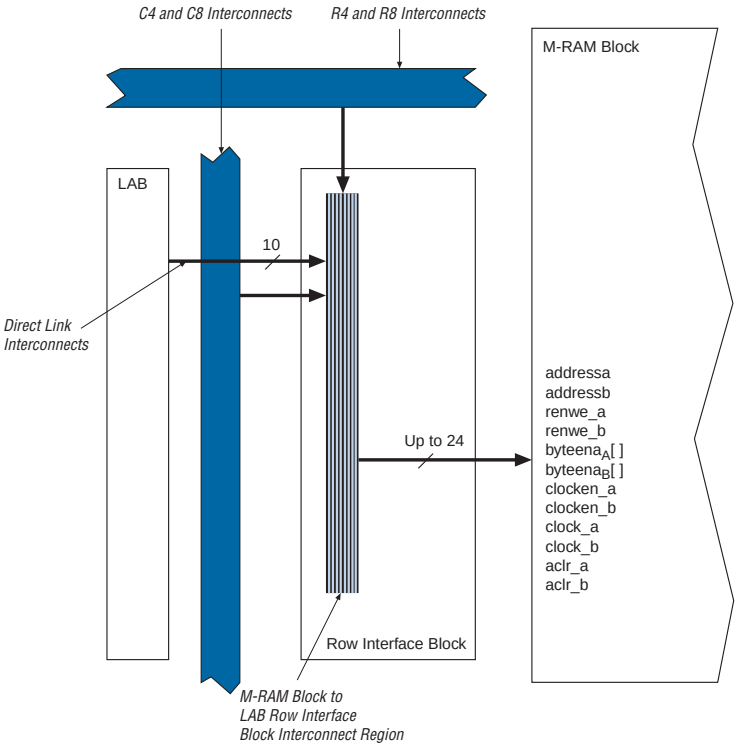
Figure 4–13. Shift Register Memory Configuration



Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large

Figure 4–21. M-RAM Row Unit Interface to Interconnect



the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

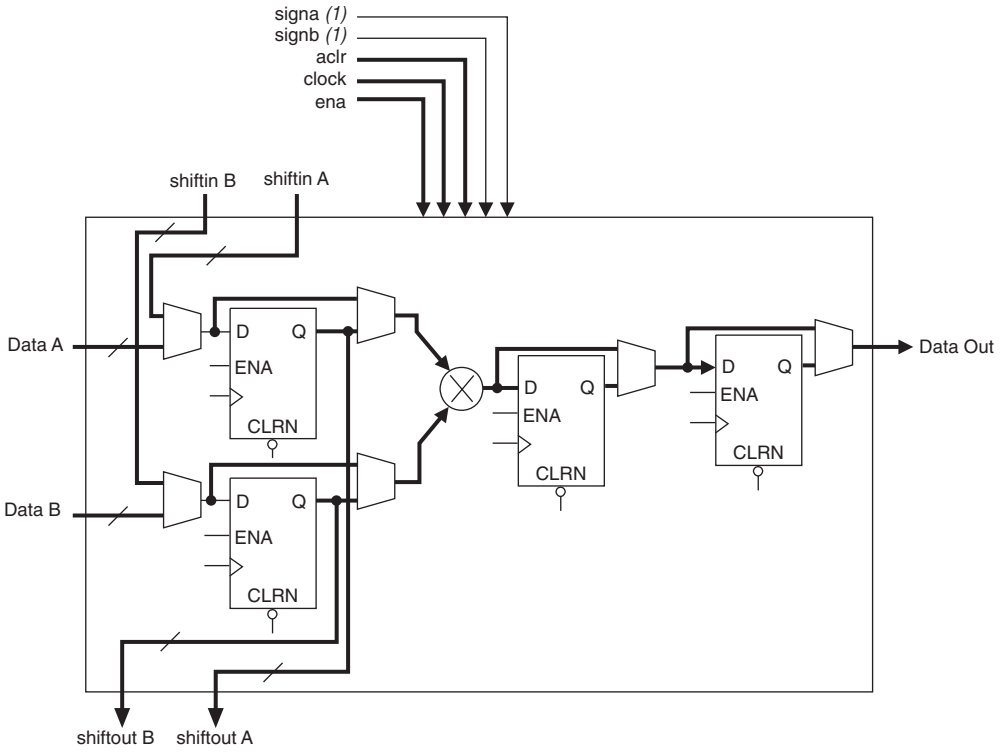
Figure 4–28 shows one of the columns with surrounding LAB rows.

Input Registers

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. You can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. You select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

You can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in Figure 4–32, to form a shift register chain. This chain can terminate in any block, that is, you can create any length of shift register chain up to 224 registers. You can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9 × 9- and 18 × 18-bit multipliers, you do not need to implement external shift registers in LAB LEs. You implement all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36 × 36-bit multipliers.

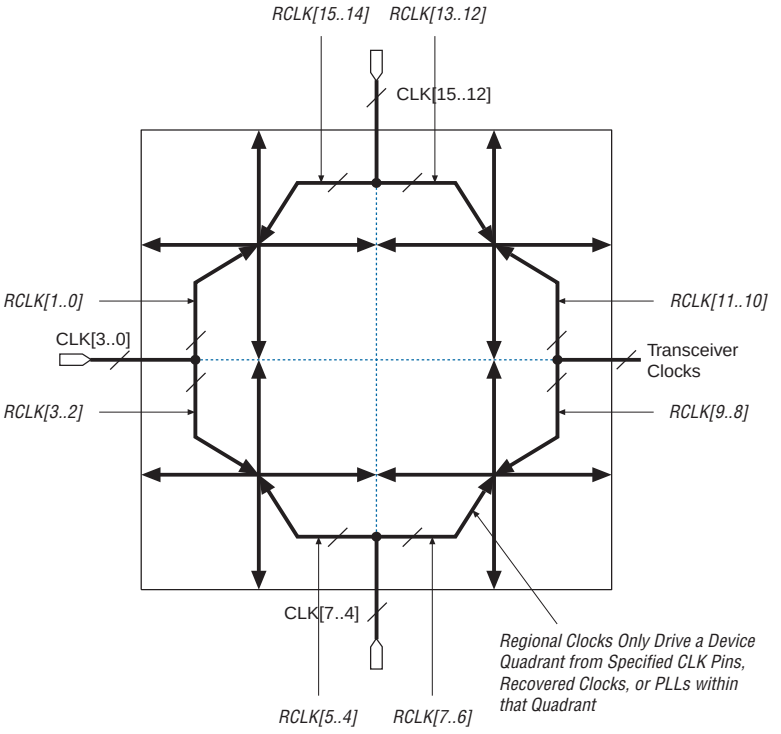
Figure 4–34. Simple Multiplier Mode



Note to Figure 4–34:
(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 4–35 shows the 36 × 36-bit multiply mode.

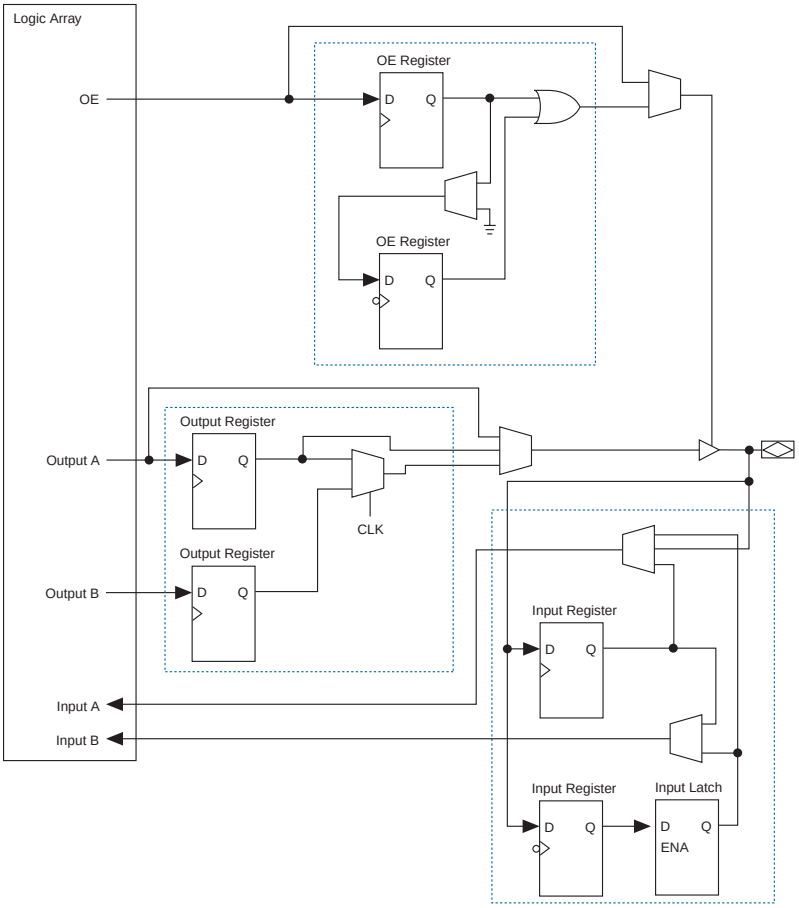
Figure 4–42. Regional Clocks



Fast Regional Clock Network

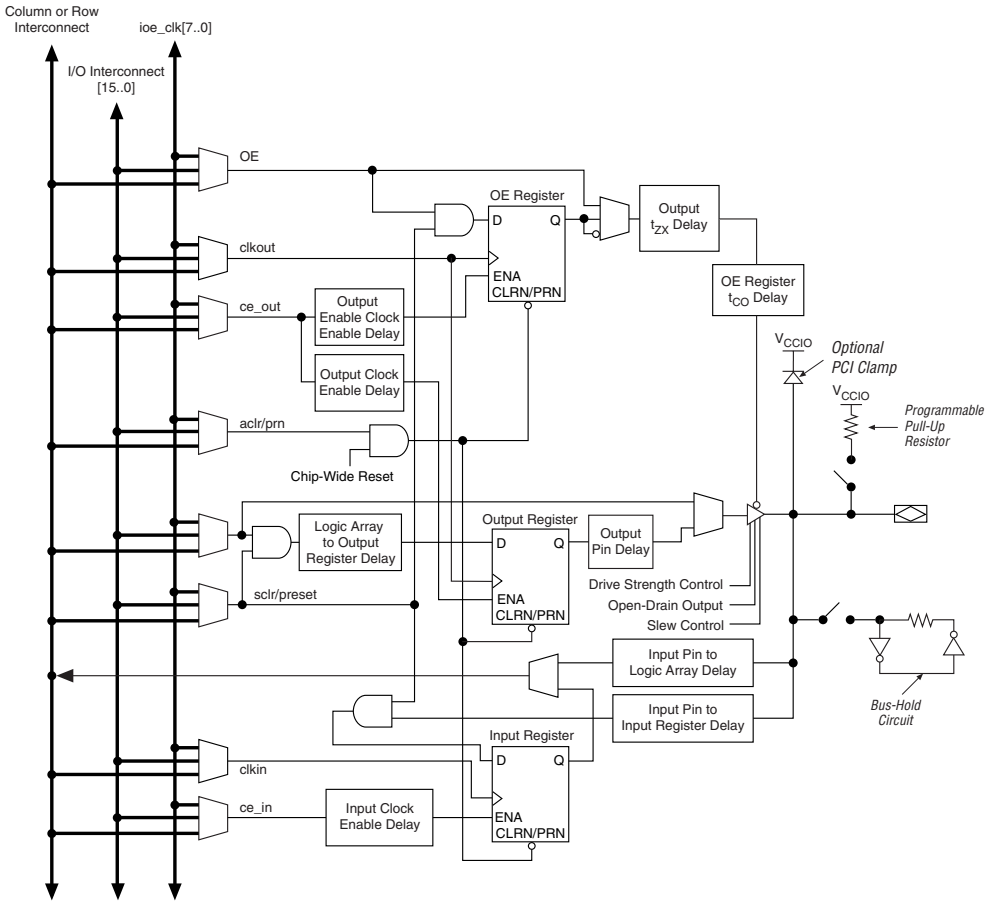
In EP1SGX25 and EP1SGX10 devices, there are two fast regional clock networks, FCLK[1..0], within each quadrant, fed by input pins (see Figure 4–43). In EP1SGX40 devices, there are two fast regional clock networks within each half-quadrant (see Figure 4–44). The FCLK[1..0] clocks can also be used for high fanout control signals, such as asynchronous clears, presets, clock enables, or protocol control signals such as TRDY and IRDY for PCI. Dual-purpose FCLK pins drive the fast clock networks. All devices have eight FCLK pins to drive fast regional clock networks. Any I/O pin can drive a clock or control signal onto any fast regional clock network with the addition of a delay. The I/O interconnect drives this signal.

Figure 4–58. Stratix GX IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix GX device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 4–59 shows how a row I/O block connects to the logic array. Figure 4–60 shows how a column I/O block connects to the logic array.

Figure 4–63. Stratix GX IOE in Bidirectional I/O Configuration *Note (1)*



Note to Figure 4–63:
(1) All input signals to the IOE can be inverted at the IOE.

The Stratix GX device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time.

Table 4–27. Stratix GX Supported I/O Standards (Part 2 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

Notes to Table 4–27:
(1) This I/O standard is only available on input and output clock pins.
(2) This I/O standard is only available on output column clock pins.

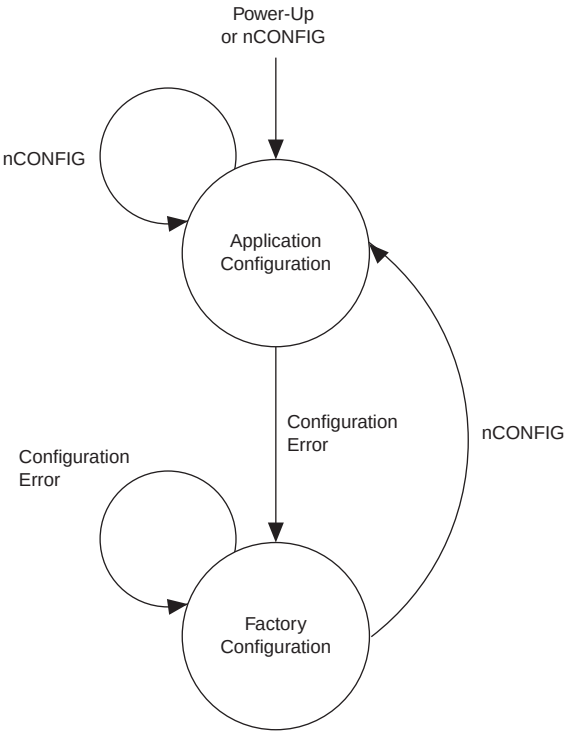
For more information on I/O standards supported by Stratix GX devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

Stratix GX devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 4–69. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 4–27 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix GX devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 4–28 shows I/O standard support for each I/O bank.

Local Update Mode

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power-up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 5–3 shows the transition diagram for local update mode.

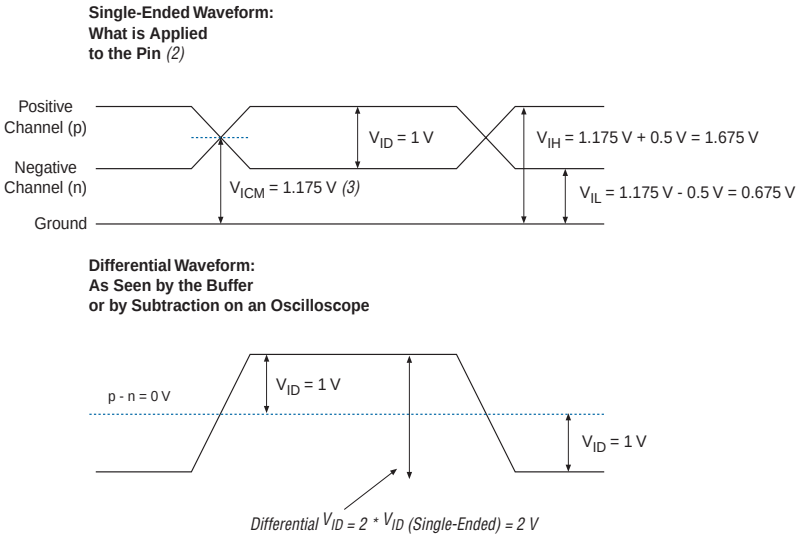
Figure 5–3. Local Update Transition Diagram



Stratix GX Automated Single Event Upset (SEU) Detection

Stratix GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy code (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

Figure 6–2. Receiver Input Waveform Example with Values



Notes to Figure 6–2:

(1) The values in this figure are for example only.

(2) These values must meet the voltages specified in the section "Operating Conditions" on page 6–1.

(3) If internal termination is used, the common mode is generated after the pins.

Figure 6–3. Transmitter Output Waveforms for Differential I/O Standards

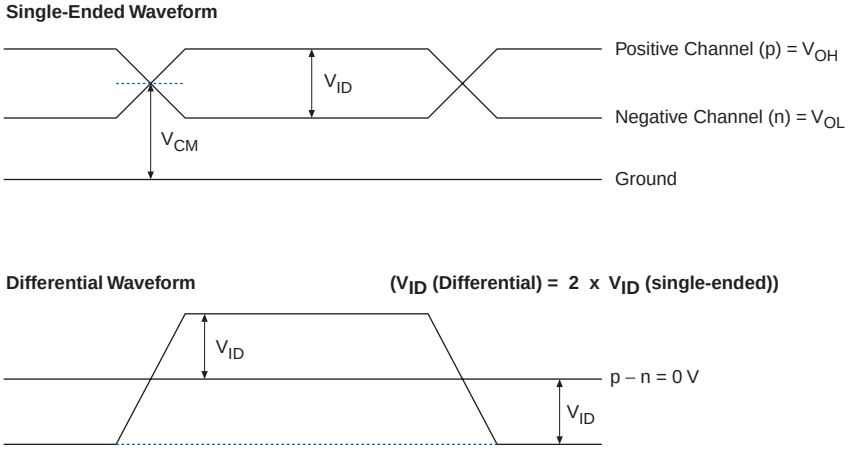


Table 6–14. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300		600	mV
V_{ICM}	Input common mode voltage		1.5		3.465	V
V_{OD}	Output differential voltage (single-ended)		300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low				50	mV
V_{OCM}	Output common mode voltage		2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low				50	mV
V_T	Output termination voltage			V_{CCIO}		V
R_1	Output external pull-up resistors		45	50	55	Ω
R_2	Output external pull-up resistors		45	50	55	Ω

Table 6–15. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300		1,000	mV
V_{ICM}	Input common mode voltage		1		2	V
V_{OD}	Differential output voltage (single ended)	R_L = 100 Ω	525	700	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.5	1.7	1.9	V
R_L	Receiver differential input resistor, external		90	100	110	Ω

Table 6–21. SSTL-18 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Table 6–22. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			V_{TT} – 0.630	V

Table 6–23. SSTL-2 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V

Table 6–72. Stratix GX I/O Standard Column Pin Input Delay Adders (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		180		189		217	ps
1.5-V HSTL class I		120		126		144	ps
1.5-V HSTL class II		120		126		144	ps
1.8-V HSTL class I		70		73		83	ps
1.8-V HSTL class II		70		73		83	ps

Table 6–73. Stratix GX I/O Standard Row Pin Input Delay Adders (Part 1 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0	ps
3.3-V LVTTL		0		0		0	ps
2.5-V LVTTL		30		31		35	ps
1.8-V LVTTL		150		157		180	ps
1.5-V LVTTL		210		220		252	ps
GTL		0		0		0	ps
GTL+		220		231		265	ps
3.3-V PCI		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0	ps
Compact PCI		0		0		0	ps
AGP 1×		0		0		0	ps
AGP 2×		0		0		0	ps
CTT		80		84		96	ps
SSTL-3 class I		–30		–32		–37	ps
SSTL-3 class II		–30		–32		–37	ps
SSTL-2 class I		–70		–74		–86	ps
SSTL-2 class II		–70		–74		–86	ps
SSTL-18 class I		180		189		217	ps
SSTL-18 class II		0		0		0	ps
1.5-V HSTL class I		130		136		156	ps

The scaling factors for output pin timing in Table 6–80 are shown in units of time per pF unit of capacitance (ps/pF). Add this delay to the combinational timing path for output or bidirectional pins in addition to the "I/O Adder" delays shown in Tables 6–72 through 6–77 and the "IOE Programmable Delays" in Tables 6–78 and 6–79.

Table 6–80. Output Delay Adder for Loading on LVTTL/LVCMOS Output Buffers

LVTTL/LVCMOS Standards						
Conditions		**Output Pin Adder Delay (ps/pF)**				
Parameter	**Value**	3.3-V LVTTL	2.5-V LVTTL	1.8-V LVTTL	1.5-V LVTTL	LVCMOS
Drive Strength	24 mA	15	–	–	-	8
	16 mA	25	18	–	–	–
	12 mA	30	25	25	–	15
	8 mA	50	35	40	35	20
	4 mA	60	–	–	80	30
	2 mA	–	75	120	160	60
SSTL/HSTL Standards						
Conditions		**Output Pin Adder Delay (ps/pF)**				
		SSTL-3	SSTL-2	SSTL-1.8	1.5-V HSTL	1.8-V HSTL
Class I		25	25	25	25	25
Class II		25	20	25	20	20
GTL+/GTL/CTT/PCI Standards						
Conditions		**Output Pin Adder Delay (ps/pF)**				
Parameter	**Value**	GTL+	GTL	CTT	PCI	AGP
V_{CCIO} voltage level	3.3 V	18	18	25	20	20
	2.5 V	15	18	-	-	-