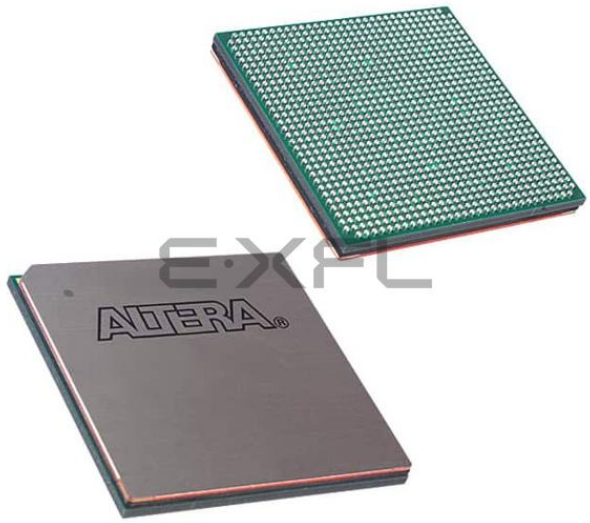

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	624
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1sgx40gf1020i6n

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix GX device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM, FCRAM, ZBT, and QDR SRAM devices.

High-speed serial interface channels support transfers at up to 840 Mbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards.

Figure 1–2 shows an overview of the Stratix GX device.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 shows the code conversion.

Table 2–3. Code Conversion

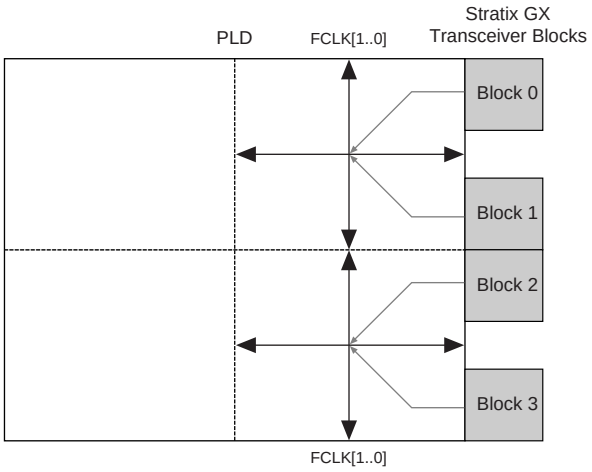
XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, `/K28.0/` (`/R/`) and `/K28.5/` (`/K/`), are automatically randomized based on a PRBS7 pattern with an x^7+x^6+1 polynomial. The `/K28.3/` (`/A/`) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the `/A/`, `/K/`, and `/R/` code groups are done automatically by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8-bit or 10-bit data into a serial stream, transmitting the LSB first. The serialized stream is then fed to the transmit buffer. Figure 2–5 is a diagram of the serializer.

Figure 2–29. EP1SGX25 Receiver PLL Recovered Clock to Fast Regional Clock Connection



In the EP1SGX40 device, the receiver PLL recovered clocks from transceivers 0 and 1 drive `RCLK[1..0]` while transceivers 2, 3, and 4 drive `RCLK[7..6]`. The regional clocks feed logic in their associated regions.

Figure 2–30. EP1SGX40 Receiver PLL Recovered Clock to Regional Clock Connection

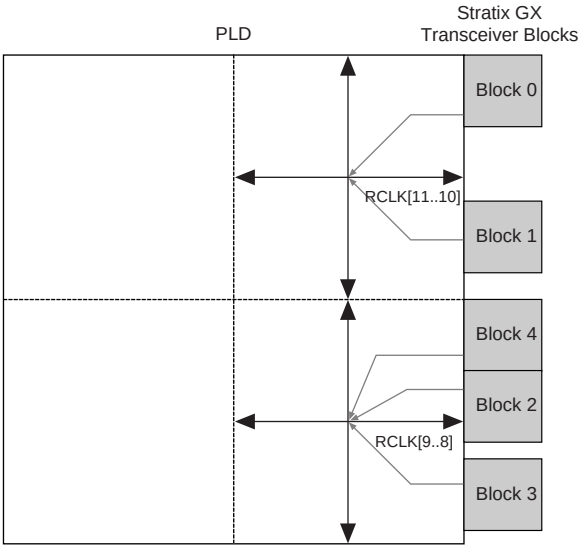


Figure 2–31 shows the possible recovered clock connection to the fast regional clock resource. The fast regional clocks can drive logic in their associated regions.

Figure 2–31. EP1SGX40 Receiver PLL Recovered Clock to Fast Regional Clock Connection

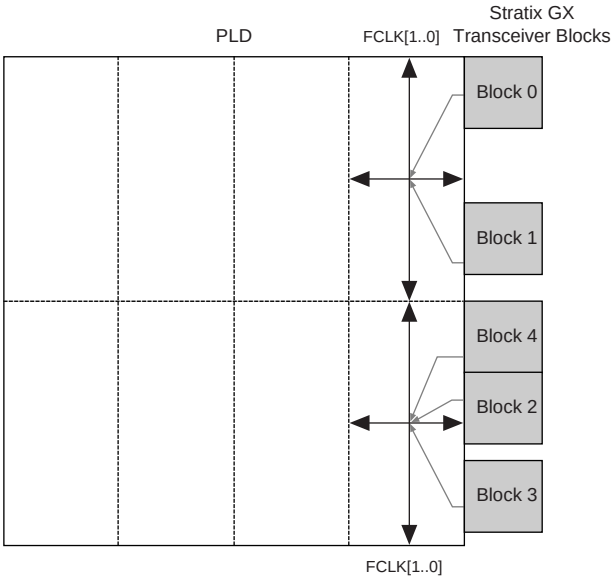


Table 2–10 summarizes the possible clocking connections for the transceivers.

Table 2–10. Possible Clocking Connections for Transceivers (Part 1 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
REFCLKB	✓	✓	✓ *(1)*	✓		✓ *(1)*
Transmitter PLL		✓	✓	✓	✓	
Receiver PLL			✓	✓	✓	
GCLK	✓	✓				
RCLK	✓	✓				
FCLK	✓	✓				

3. Source-Synchronous Signaling With DPA

SGX51003-1.1

Introduction

Expansion in the telecommunications market and growth in Internet use requires systems to move more data faster than ever. To meet this demand, rely on solutions such as differential signaling and emerging high-speed interface standards including RapidIO, POS-PHY 4, SFI-4, or XSBI.

These new protocols support differential data rates up to 1 Gbps and higher. At these high data rates, it becomes more challenging to manage the skew between the clock and data signals. One solution to this challenge is to use CDR to eliminate skew between data channels and clock signals. Another potential solution, DPA, is beginning to be incorporated into some of these protocols.

The source-synchronous high-speed interface in Stratix GX devices is a dedicated circuit embedded into the PLD allowing for high-speed communications. The *High-Speed Source-Synchronous Differential I/O Interfaces in Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2* provides information on the high-speed I/O standard features and functions of the Stratix GX device.

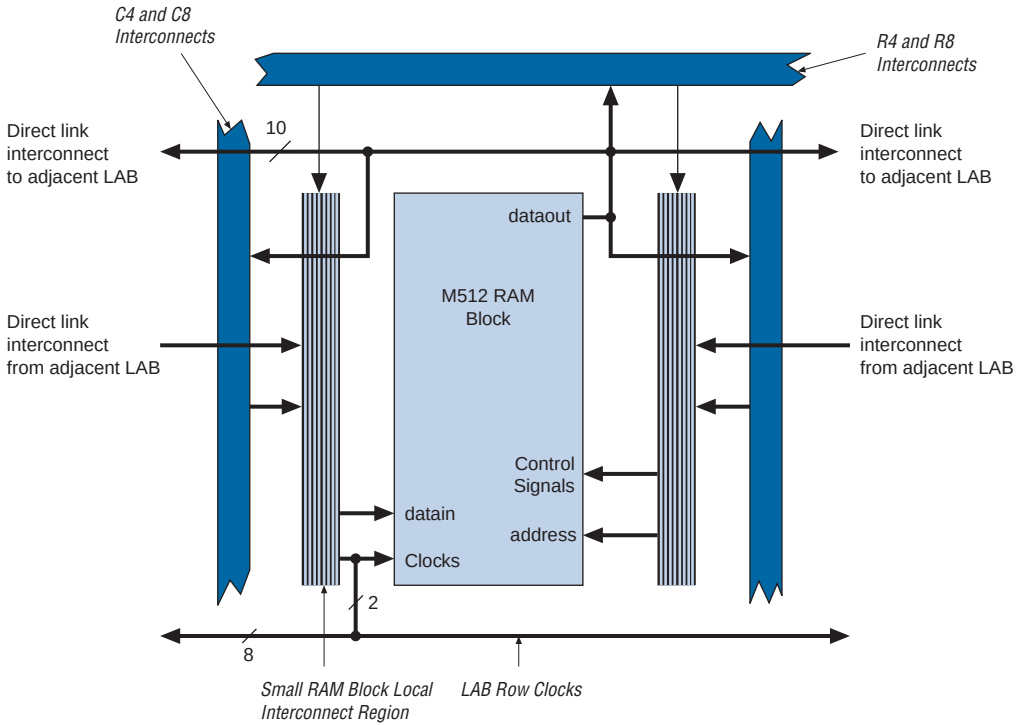
Stratix GX I/O Banks

Stratix GX devices contain 17 I/O banks. I/O banks one and two support high-speed LVDS, LVPECL, and 3.3-V PCML inputs and outputs. These two banks also incorporate an embedded dynamic phase aligner within the source-synchronous interface (see Figure 3–8 on page 3–10). The dynamic phase aligner corrects for the phase difference between the clock and data lines caused by skew. The dynamic phase aligner operates automatically and continuously without requiring a fixed training pattern, and allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-clock skew.

Principles of SERDES Operation

Stratix GX devices support source-synchronous differential signaling up to 1 Gbps in DPA mode, and up to 840 Mbps in non-DPA mode. Serial data is transmitted and received along with a low-frequency clock. The PLL can multiply the incoming low-frequency clock by a factor of 1 to 10. The SERDES factor *J* can be 8 or 10 for the DPA mode, or 4, 7, 8, or 10 for all other modes. The SERDES factor does not have to equal the clock

Figure 4–15. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block implements buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Table 4–10. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2)	
byteena[15..0]	**datain ×144**
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

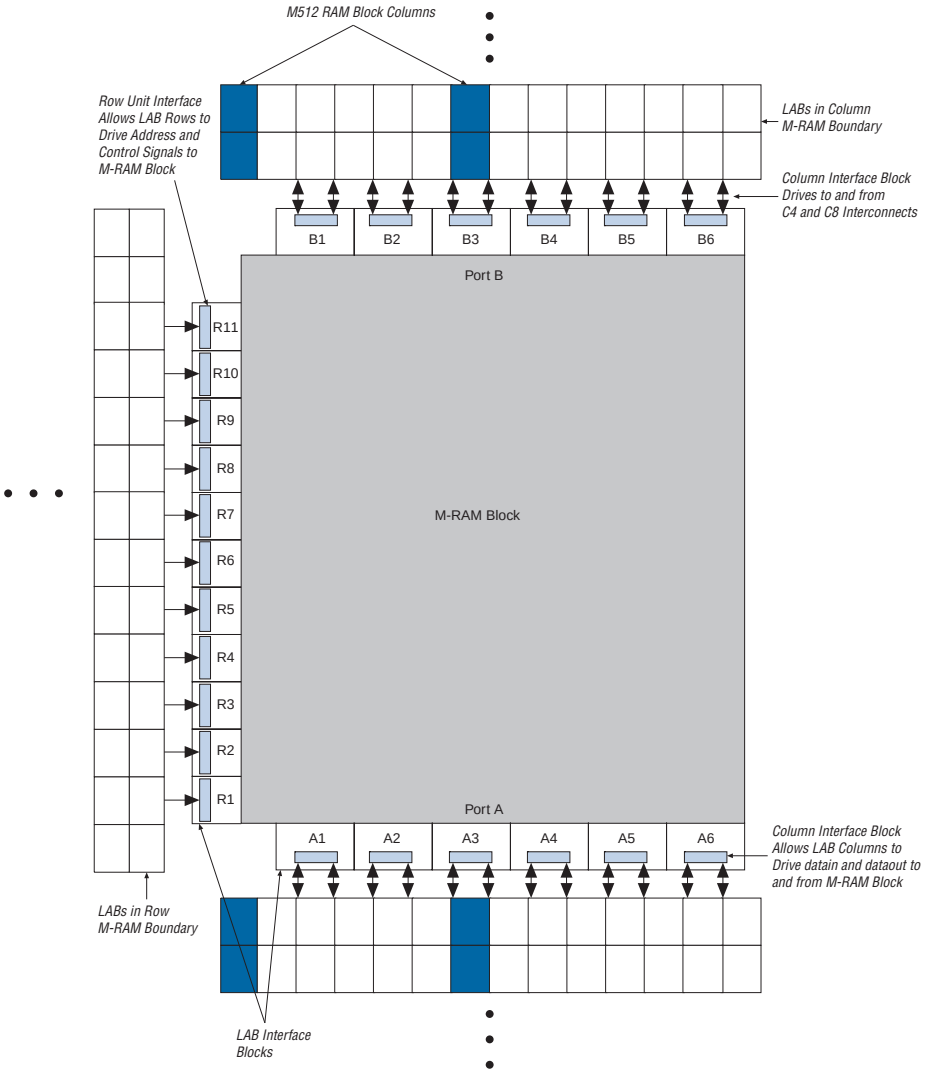
Notes to Tables 4–9 and 4–10:

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, that is, in ×16, ×32, ×64, and ×128 modes.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals as shown in Figure 4–18.

Figure 4–20. Left-Facing M-RAM to Interconnect Interface *Notes (1), (2)*



Notes to Figure 4–20:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Figure 4–43. EP1SGX25 & EP1SGX10 Device Fast Clock Pin Connections to Fast Regional Clocks

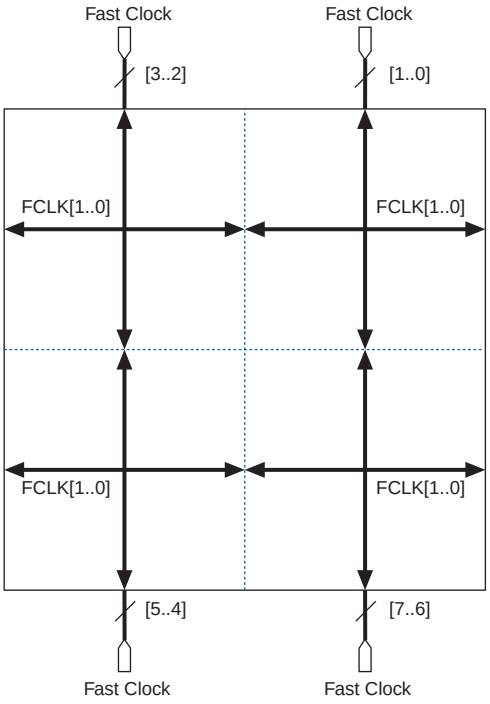
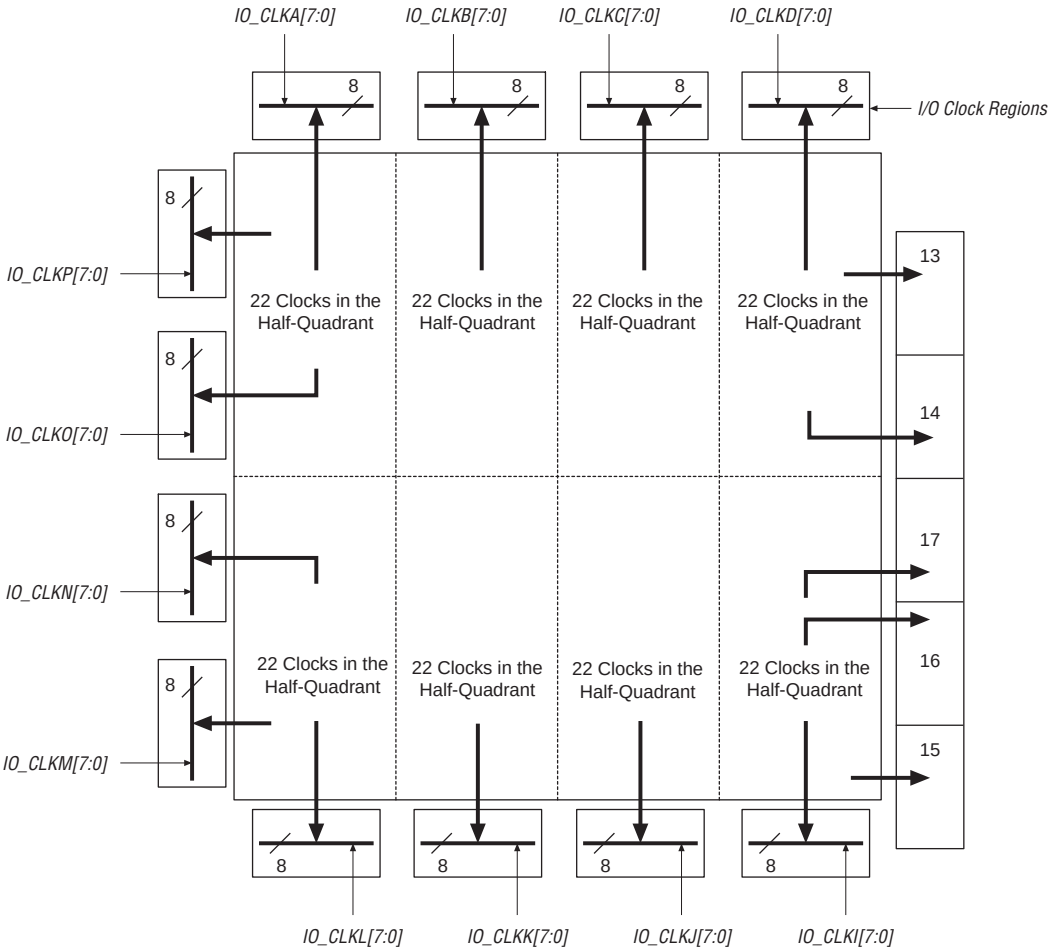


Figure 4–47. EP1SGX40 Device I/O Clock Groups

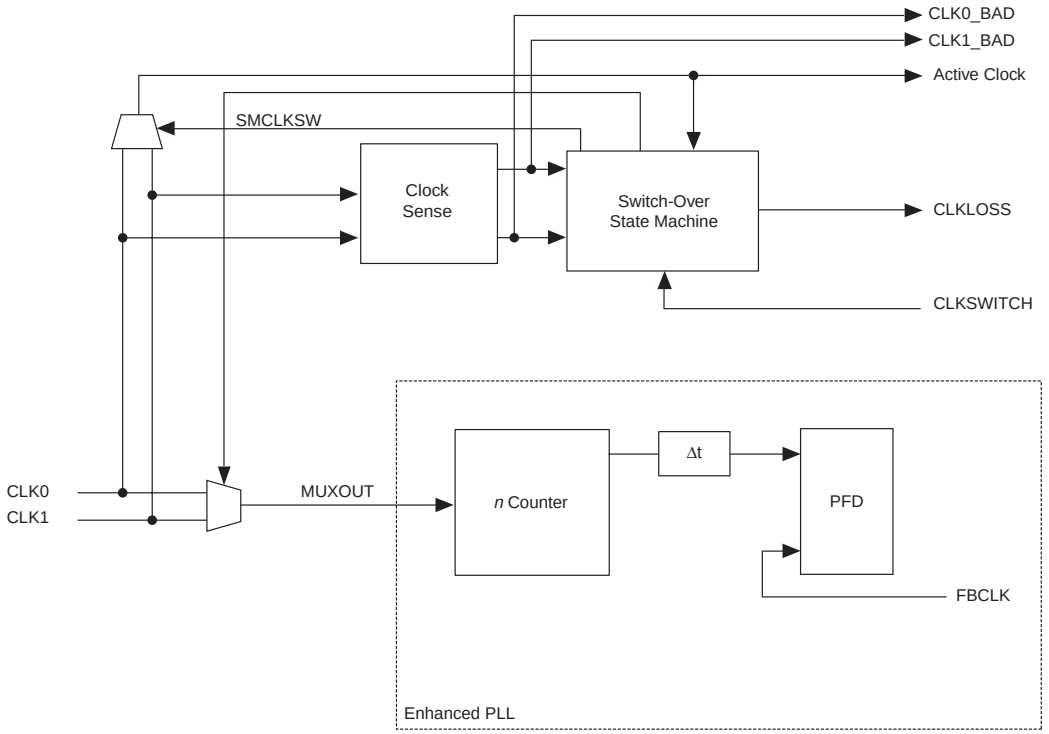


You can use the Quartus II software to control whether a clock input pin is either global, regional, or fast regional. The Quartus II software automatically selects the clocking resources if not specified.

Enhanced & Fast PLLs

Stratix GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum

Figure 4–52. Clock Switchover Circuitry

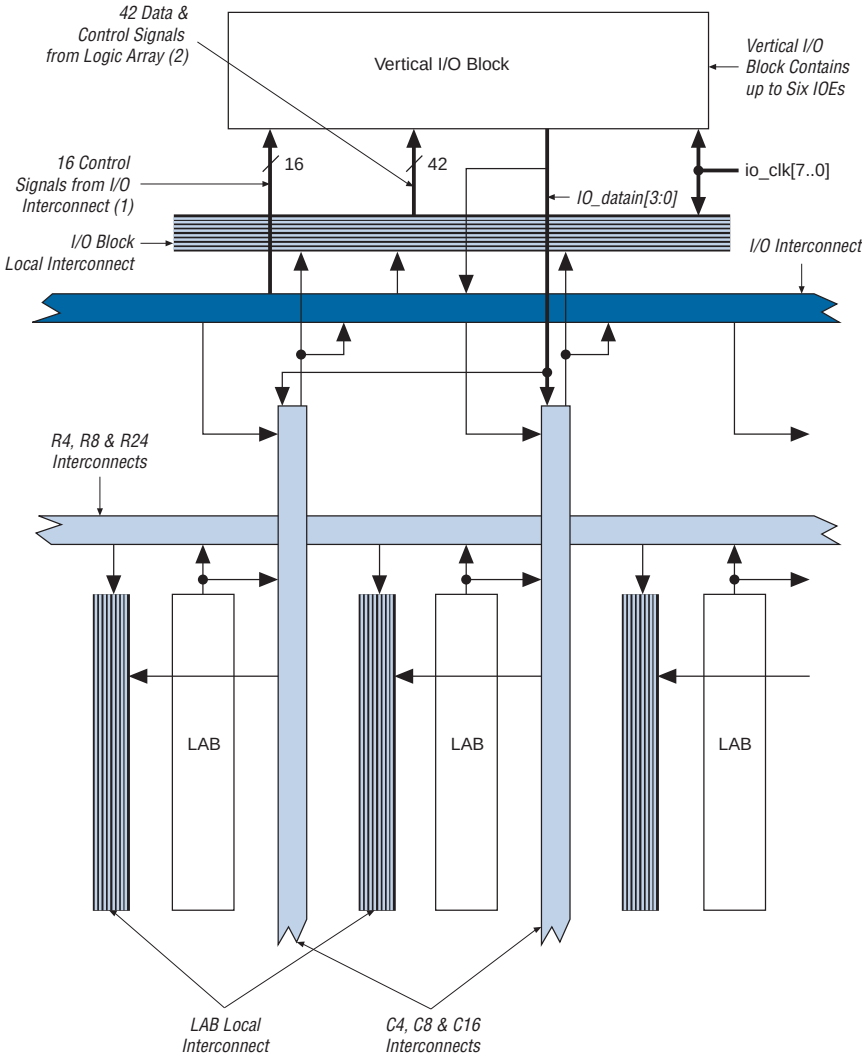


Note to Figure 4–52:
(1) PFD: phase frequency detector.

There are two possible ways to use the clock switchover feature.

- You can use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 4–52. In this case, the secondary clock becomes the reference clock for the PLL.
- You can use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane,

Figure 4–60. Column I/O Block Connection to the Interconnect

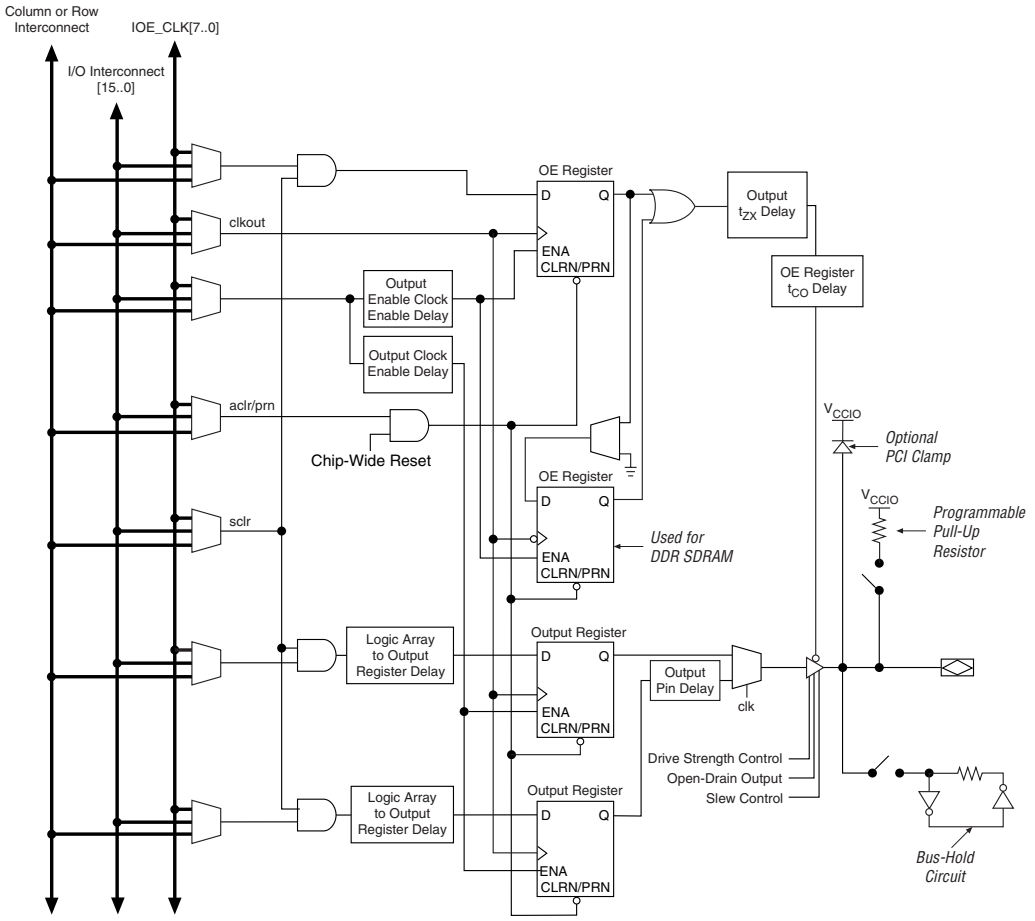


Notes to Figure 4–60:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

Figure 4–66. Stratix GX IOE in DDR Output I/O Configuration *Notes (1), (2)*



Notes to Figure 4–66:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tristate is by default active high. It can, however, be designed to be active low.

2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 4–32 summarizes Stratix GX MultiVolt I/O support.

Table 4–32. Stratix GX MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal *(5)*					Output Signal *(6)*				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*		✓				
1.8	✓ *(2)*	✓	✓ *(2)*	✓ *(2)*		✓ *(3)*	✓			
2.5			✓	✓		✓ *(3)*	✓ *(3)*	✓		
3.3			✓ *(2)*	✓	✓ *(4)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 4–32:

(1) To drive inputs higher than V_{CCIO} but less than 4.1 V, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent V_I from rising above 4.0 V.

(2) The input pin current may be slightly higher than the typical value.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix GX device to drive out, a receiving device powered at a different level can still interface with the Stratix GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix GX devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.

(5) This is the external signal that is driving the Stratix GX device.

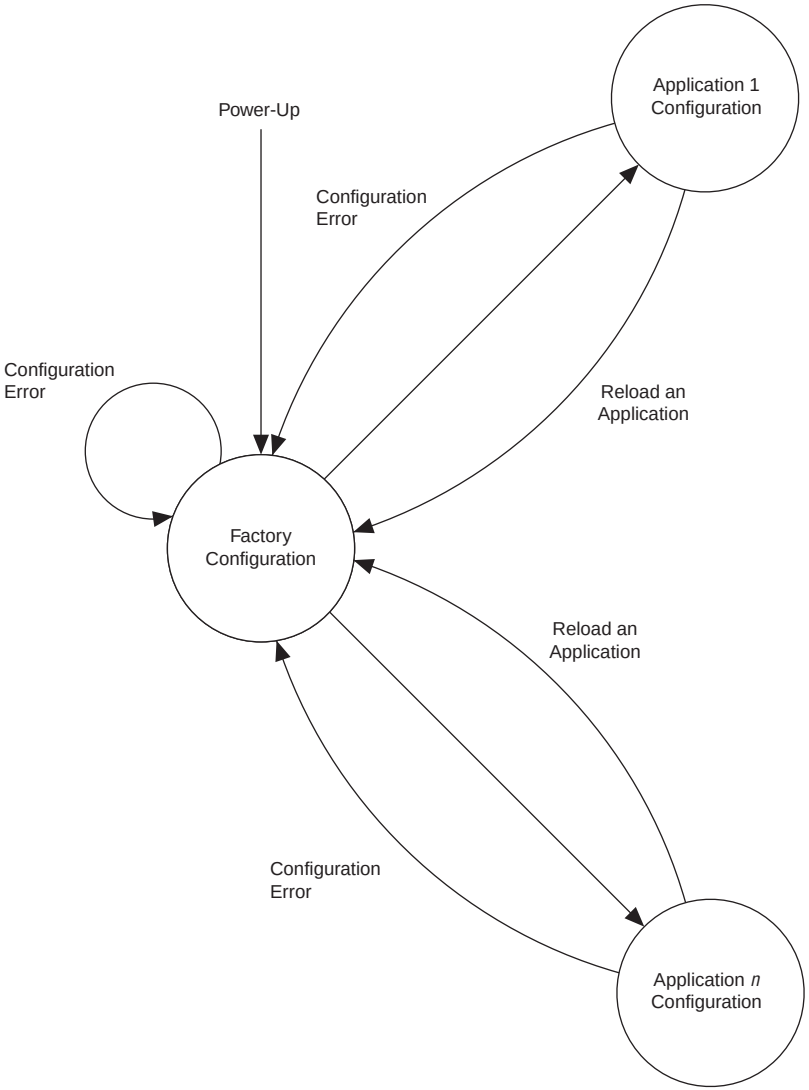
(6) This represents the system voltage that Stratix GX supports when a VCCIO pin is connected to a specific voltage level. For example, when VCCIO is 3.3 V and if the I/O standard is LVTTL/LVCMOS, the output high of the signal coming out from Stratix GX is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Power Sequencing & Hot Socketing

Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the VCCIO and VCCINT power supplies may be powered in any order.

Signals can be driven into Stratix GX devices before and during power up without damaging the device. In addition, Stratix GX devices do not drive out during power up. Once operating conditions are reached and the device is configured, Stratix GX devices operate as specified by the user. For more information, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix GX Device Handbook, Volume 2*.

Figure 5–2. Remote Update Transition Diagram *Notes (1), (2)*



Notes to Figure 5–2:

(1) Remote update of application configuration is controlled by a Nios embedded processor or user logic programmed in the factory or application configurations.

(2) Up to seven pages can be specified allowing up to seven different configuration applications.

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 5 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade (1)			-6 Commercial & Industrial Speed Grade (1)			-7 Commercial & Industrial Speed Grade (1)			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fibre Channel Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.0625 Gbps Pre-emphasis = 0 V_{OD} = 1,200 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.125 Gbps Pre-emphasis= 1 V_{OD} = 1,200 mV			0.16			0.16			0.16	UI
Total jitter				0.33			0.33			0.33	UI
Serial Rapid I/O Short Run Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.25 Gbps Pre-emphasis = 1 V_{OD} = 1,600 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.5 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.15			0.15			0.15	UI
Total jitter				0.32			0.32			0.32	UI
Deterministic jitter	3.125 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.15			0.15			N/A	UI
Total jitter				0.32			0.32			N/A	UI
Serial Rapid I/O Long Run Transmitter Jitter using 8B/10B Encoded CRPAT *Note (9)*											
Deterministic jitter	1.25 Gbps Pre-emphasis = 1 V_{OD} = 1,600 mV			0.09			0.09			0.09	UI
Total jitter				0.17			0.17			0.17	UI
Deterministic jitter	2.5 Gbps Pre-emphasis = 2 V_{OD} = 1,400 mV			0.18			0.18			0.18	UI
Total jitter				0.35			0.35			0.35	UI
Deterministic jitter	3.125 Gbps Pre-emphasis = 2 V_{OD} = 1,400 mV			0.20			0.20			N/A	UI
Total jitter				0.37			0.37			N/A	UI
SONET Transmitter Jitter PRBS23 *Note (9)*											
Total jitter	2.48832 Gbps Pre-emphasis = 1 V_{OD} = 800 mV			0.20			0.20			0.20	UI

Table 6–7. Stratix GX Transceiver Block AC Specification (Part 6 of 7)

Symbol / Description	Conditions	-5 Commercial Speed Grade *(1)*			-6 Commercial & Industrial Speed Grade *(1)*			-7 Commercial & Industrial Speed Grade *(1)*			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
XAUI Transmitter Jitter using 8B/10B Encoded CJPAT *Note (9)*											
Deterministic jitter	3.125 Gbps Pre-emphasis = 0 V_{OD} = 1,200 mV			0.15			0.15			N/A	UI
Total jitter				0.32			0.32			N/A	UI
Jitter transfer bandwidth *(10)*	Low bandwidth setting at 3.125 Gbps		3			3				N/A	MHz
	High bandwidth setting at 3.125 Gbps		4.7			4.7				N/A	MHz
	Low bandwidth setting at 2.5 Gbps		3.2			3.2				3.2	MHz
	High bandwidth setting at 2.5 Gbps		4.3			4.3				4.3	MHz
Output t_{RISE}	20% to 80%	60		130	60		130	60		130	ps
Output t_{FALL}	80% to 20%	60		130	60		130	60		130	ps
Transmit latency *(11)*	Single width	3		8	3		8	3		8	*(3)*
	Double width	3		7	3		7	3		7	*(3)*
Intra differential pair skew				10			10			10	ps
Channel to channel skew	Within a single quadrant			50			50			50	ps

Table 6–52 shows the external I/O timing parameters when using regional clock networks.

Table 6–52. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	C_{LOAD} = 10 pF

Notes to Table 6–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. You should use the Quartus II software to verify the external timing for any pin.

Table 6–53 shows the external I/O timing parameters when using global clock networks.

Table 6–53. Stratix GX Global Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	C_{LOAD} = 10 pF
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	

Table 6–84. Stratix GX Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
1.8 V	250	250	250	MHz
1.5 V	225	200	200	MHz
LVCMOS	350	300	250	MHz
GTL	200	167	125	MHz
GTL+	200	167	125	MHz
SSTL-3 class I	167	150	133	MHz
SSTL-3 class II	167	150	133	MHz
SSTL-2 class I	200	200	167	MHz
SSTL-2 class II	200	200	167	MHz
SSTL-18 class I	150	133	133	MHz
SSTL-18 class II	150	133	133	MHz
1.5-V HSTL class I	250	225	200	MHz
1.5-V HSTL class II	225	200	200	MHz
1.8-V HSTL class I	250	225	200	MHz
1.8-V HSTL class II	225	200	200	MHz
3.3-V PCI	350	300	250	MHz
3.3-V PCI-X 1.0	350	300	250	MHz
Compact PCI	350	300	250	MHz
AGP 1×	350	300	250	MHz
AGP 2×	350	300	250	MHz
CTT	200	200	200	MHz
Differential HSTL	225	200	200	MHz
Differential SSTL-2	200	200	167	MHz
LVDS	500	500	500	MHz
LVPECL	500	500	500	MHz
PCML	350	350	350	MHz
HyperTransport technology	350	350	350	MHz

Table 6–85. Stratix GX Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2] Pins (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Unit
LVTTL	400	350	300	MHz
2.5 V	400	350	300	MHz
1.8 V	400	350	300	MHz