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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (1.375K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f04ka201-i-ss

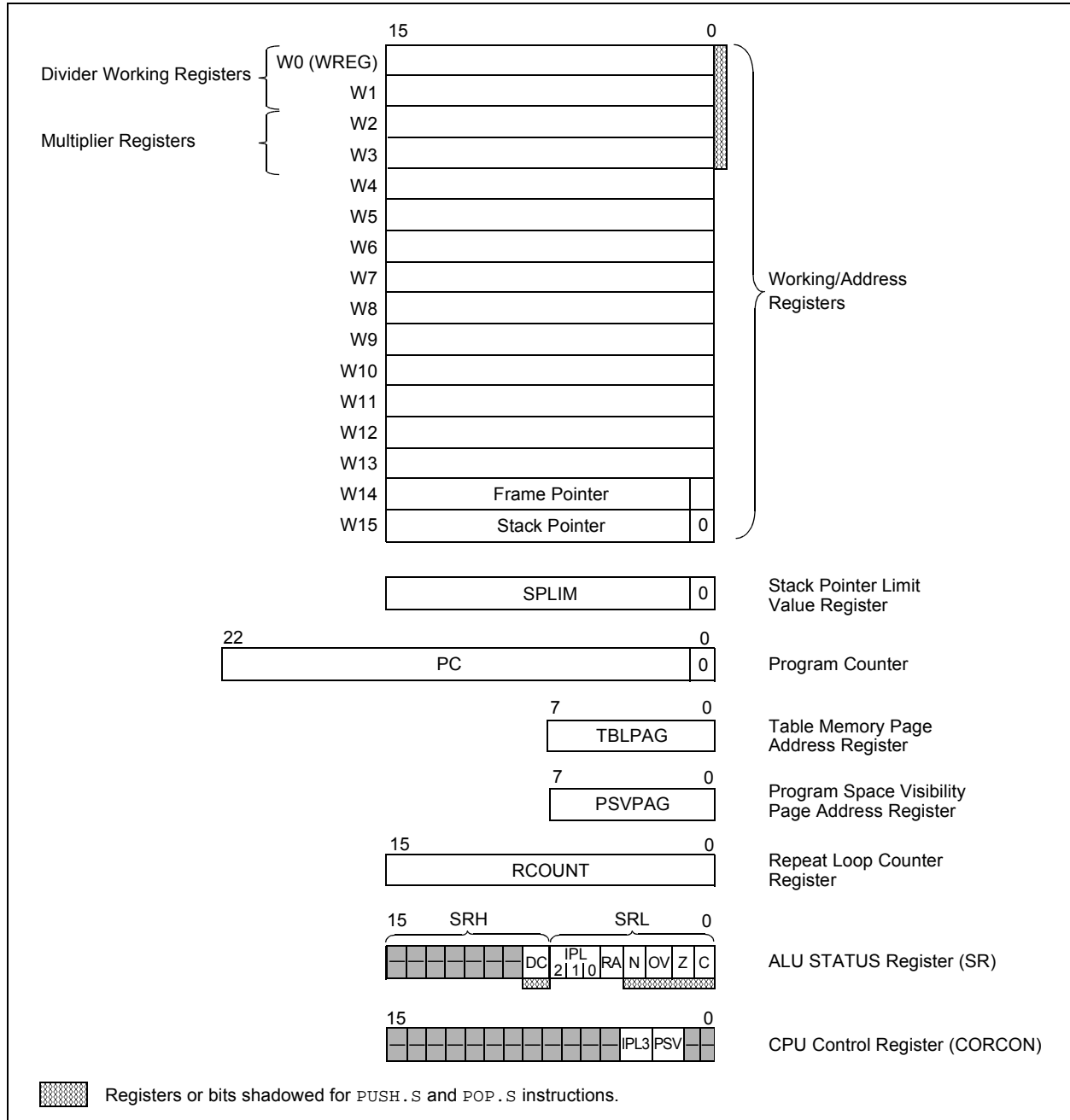
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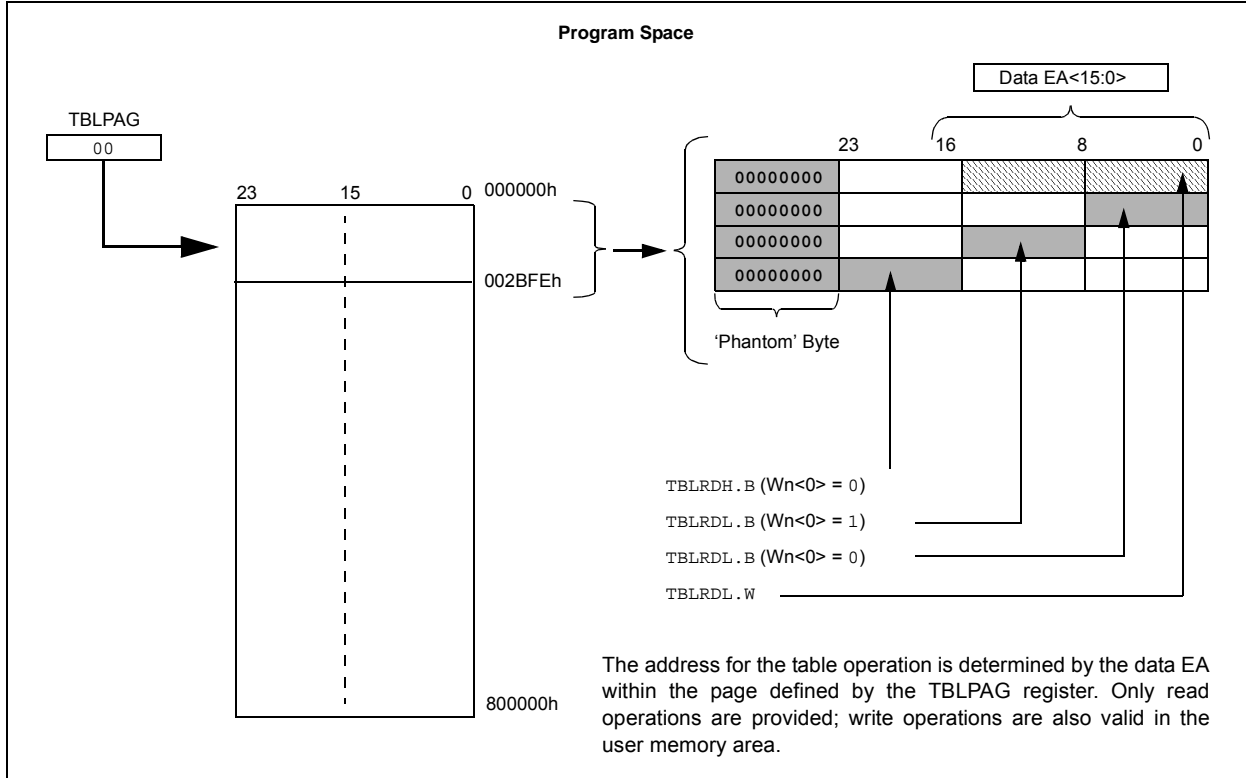
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FIGURE 3-2: PROGRAMMER'S MODEL



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FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



4.3.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into an 8K word page (in PIC24F08KA1XX devices) and a 16K word page (in PIC24F16KA1XX devices) of the program space. This provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the MSb of the data space EA is '1', and PSV is enabled by setting the PSV bit in the CPU Control (CORCON<2>) register. The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page Address register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits.

By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads from this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-7), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space locations used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note: PSV access is temporarily disabled during table reads/writes.

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

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5.5.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time by erasing the programmable row. The general process is:

1. Read a row of program memory (32 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase a row (see Example 5-1):
 - a) Set the NVMOP bits (NVMCON<5:0>) to '011000' to configure for row erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
 - b) Write the starting address of the block to be erased into the TBLPAG and W registers.
 - c) Write 55h to NVMKEY.
 - d) Write AAh to NVMKEY.
 - e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.

4. Write the first 32 instructions from data RAM into the program memory buffers (see Example 5-1).
5. Write the program block to Flash memory:
 - a) Set the NVMOP bits to '011000' to configure for row programming. Clear the ERASE bit and set the WREN bit.
 - b) Write 55h to NVMKEY.
 - c) Write AAh to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS, as displayed in Example 5-5.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY ROW – ASSEMBLY LANGUAGE CODE

```
; Set up NVMCON for row erase operation
MOV    #0x4058, W0                ;
MOV    W0, NVMCON                ; Initialize NVMCON
; Init pointer to row to be ERASED
MOV    #tblpage(PROG_ADDR), W0   ;
MOV    W0, TBLPAG                ; Initialize PM Page Boundary SFR
MOV    #tbloffset(PROG_ADDR), W0 ; Initialize in-page EA[15:0] pointer
TBLWTL W0, [W0]                 ; Set base address of erase block
DISI   #5                        ; Block all interrupts
                                           for next 5 instructions

MOV    #0x55, W0
MOV    W0, NVMKEY                ; Write the 55 key
MOV    #0xAA, W1
MOV    W1, NVMKEY                ; Write the AA key
BSET   NVMCON, #WR               ; Start the erase sequence
NOP                                         ; Insert two NOPS after the erase
NOP                                         ; command is asserted
```

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TABLE 7-1: TRAP VECTOR DETAILS

Vector Number	IVT Address	AIVT Address	Trap Source
0	000004h	000104h	Reserved
1	000006h	000106h	Oscillator Failure
2	000008h	000108h	Address Error
3	00000Ah	00010Ah	Stack Error
4	00000Ch	00010Ch	Math Error
5	00000Eh	00010Eh	Reserved
6	000010h	000110h	Reserved
7	000012h	000112h	Reserved

TABLE 7-2: IMPLEMENTED INTERRUPT VECTORS

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
ADC1 Conversion Done	13	00002Eh	00012Eh	IFS0<13>	IEC0<13>	IPC3<6:4>
Comparator Event	18	000038h	000138h	IFS1<2>	IEC1<2>	IPC4<10:8>
CTMU	77	0000AEh	0001AEh	IFS4<13>	IEC4<13>	IPC19<6:4>
External Interrupt 0	0	000014h	000114h	IFS0<0>	IEC0<0>	IPC0<2:0>
External Interrupt 1	20	00003Ch	00013Ch	IFS1<4>	IEC1<4>	IPC5<2:0>
External Interrupt 2	29	00004Eh	00014Eh	IFS1<13>	IEC1<13>	IPC7<6:4>
I2C1 Master Event	17	000036h	000136h	IFS1<1>	IEC1<1>	IPC4<6:4>
I2C1 Slave Event	16	000034h	000134h	IFS1<0>	IEC1<0>	IPC4<2:0>
Input Capture1	1	000016h	000116h	IFS0<1>	IEC0<1>	IPC0<6:4>
Input Change Notification	19	00003Ah	00013Ah	IFS1<3>	IEC1<3>	IPC4<14:12>
HLVD High/Low-Voltage Detect	72	0000A4h	0001A4h	IFS4<8>	IEC4<8>	IPC17<2:0>
NVM – NVM Write Complete	15	000032h	000132h	IFS0<15>	IEC0<15>	IPC3<14:12>
Output Compare 1	2	000018h	000118h	IFS0<2>	IEC0<2>	IPC0<10:8>
SPI1 Error	9	000026h	000126h	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Event	10	000028h	000128h	IFS0<10>	IEC0<10>	IPC2<10:8>
Timer1	3	00001Ah	00011Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	7	000022h	000122h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	8	000024h	000124h	IFS0<8>	IEC0<8>	IPC2<2:0>
UART1 Error	65	000096h	000196h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	11	00002Ah	00012Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	12	00002Ch	00012Ch	IFS0<12>	IEC0<12>	IPC3<2:0>

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REGISTER 7-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0, HSC	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽²⁾	PSV ⁽¹⁾	—	—
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit⁽²⁾
 1 = CPU interrupt priority level is greater than 7
 0 = CPU interrupt priority level is 7 or less

bit 1-0 **Unimplemented:** Read as '0'

Note 1: See Register 3-1 for the description of this bit, which is not dedicated to interrupt control functions.

Note 2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

Note: Bit 2 is described in Section 3.0 "CPU" .

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8.1 CPU Clocking Scheme

The system clock source can be provided by one of four sources:

- Primary Oscillator (POSC) on the OSC1 and OSC0 pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins

The PIC24F04KA201 family devices consist of two types of secondary oscillator:

- High-Power Secondary Oscillator
- Low-Power Secondary Oscillator

These can be selected by using the SOSCESEL (FOSC<5>) bit.

- Fast Internal RC (FRC) Oscillator
 - 8 MHz FRC Oscillator
 - 500 kHz Lower Power FRC Oscillator
- Low-Power Internal RC (LPRC) Oscillator

The primary oscillator and 8 MHz FRC sources have the option of using the internal 4x PLL. The frequency of the FRC clock source can optionally be reduced by the programmable clock divider. The selected clock source generates the processor and peripheral clock sources.

The processor clock source is divided by two to produce the internal instruction cycle clock, Fcy. In this document, the instruction cycle clock is also denoted by Fosc/2. The internal instruction cycle clock, Fosc/2, can be provided on the OSC0 I/O pin for some operating modes of the primary oscillator.

8.2 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset (POR) event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory (refer to **Section 23.1 “Configuration Bits”** for further details). The Primary Oscillator Configuration bits, POSCMD<1:0> (FOSC<1:0>), and the Initial Oscillator Select Configuration bits, FNOSEC<2:0> (FOSCSEL<2:0>), select the oscillator source that is used at a POR. The FRC primary oscillator with postscaler (FRCDIV) is the default (unprogrammed) selection. The secondary oscillator, or one of the internal oscillators, may be chosen by programming these bit locations. The EC mode frequency range Configuration bits, POSCFREQ<1:0> (FOSC<4:3>), optimize power consumption when running in EC mode. The default configuration is “frequency range is greater than 8 MHz”.

The Configuration bits allow users to choose between the various clock modes, shown in Table 8-1.

8.2.1 CLOCK SWITCHING MODE CONFIGURATION BITS

The FCKSM Configuration bits (FOSC<7:6>) are used jointly to configure device clock switching and the FSCM. Clock switching is enabled only when FCKSM1 is programmed ('0'). The FSCM is enabled only when FCKSM<1:0> are both programmed ('00').

TABLE 8-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSEC<2:0>	Note
8 MHz FRC Oscillator with Postscaler (FRCDIV)	Internal	11	111	1, 2
500 MHz FRC Oscillator with Postscaler (LPFRCDIV)	Internal	11	110	1
Low-Power RC Oscillator (LPRC)	Internal	11	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	00	100	1
Primary Oscillator (HS) with PLL Module (HSPLL)	Primary	10	011	
Primary Oscillator (EC) with PLL Module (ECPLL)	Primary	00	011	
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	
8 MHz FRC Oscillator with PLL Module (FRCPLL)	Internal	11	001	1
8 MHz FRC Oscillator (FRC)	Internal	11	000	1

Note 1: OSC0 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

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14.3 Pulse-Width Modulation (PWM) Mode

The following steps should be taken when configuring the output compare module for PWM operation:

1. Set the PWM period by writing to the selected Timer Period register (PRy).
2. Set the PWM duty cycle by writing to the OC1RS register.
3. Write the OC1R register with the initial duty cycle.
4. Enable interrupts, if required, for the timer and output compare modules. The output compare interrupt is required for PWM Fault pin utilization.
5. Configure the output compare module for one of two PWM Operation modes by writing to the Output Compare Mode bits, OCM<2:0> (OC1CON<2:0>).
6. Set the TMRy prescale value and enable the time base by setting TON (TxCON<15>) = 1.

Note: The OC1R register should be initialized before the output compare module is first enabled. The OC1R register becomes a read-only Duty Cycle register when the module is operated in the PWM modes. The value held in OC1R will become the PWM duty cycle for the first PWM period. The contents of the Output Compare 1 Secondary register, OC1RS, will not be transferred into OC1R until a time base period match occurs.

14.3.1 PWM PERIOD

The PWM period is specified by writing to PRy, the Timer Period register. The PWM period can be calculated using Equation 14-1.

EQUATION 14-1: CALCULATING THE PWM PERIOD⁽¹⁾

$$\text{PWM Period} = [(PRy) + 1] \cdot T_{CY} \cdot (\text{Timer Prescale Value})$$

where:

$$\text{PWM Frequency} = 1/[\text{PWM Period}]$$

Note 1: Based on $T_{CY} = 2 \cdot T_{OSC}$, Doze mode and PLL are disabled.

Note: A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7 written into the PRy register will yield a period consisting of 8 time base cycles.

14.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OC1RS register. The OC1RS register can be written to at any time, but the duty cycle value is not latched into OC1R until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation. In PWM mode, OC1R is a read-only register.

Some important boundary parameters of the PWM duty cycle include:

- If the Output Compare 1 register, OC1R, is loaded with 0000h, the OC1 pin will remain low (0% duty cycle).
- If OC1R is greater than PRy (Timer Period register), the pin will remain high (100% duty cycle).
- If OC1R is equal to PRy, the OC1 pin will be low for one time base count value and high for all other count values.

See Example 14-1 for PWM mode timing details. Table 14-1 provides an example of PWM frequencies and resolutions for a device operating at 10 MIPS.

EQUATION 14-2: CALCULATION FOR MAXIMUM PWM RESOLUTION⁽¹⁾

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{CY}}{F_{PWM} \cdot (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

Note 1: Based on $F_{CY} = F_{OSC}/2$, Doze mode and PLL are disabled.

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REGISTER 15-2: SPI1CON1: SPI CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE ⁽¹⁾	
bit 15								bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **DISSCK:** Disable SCK1 pin bit (SPI Master modes only)
 - 1 = Internal SPI clock is disabled, pin functions as I/O
 - 0 = Internal SPI clock is enabled
- bit 11 **DISSDO:** Disables SDO1 pin bit
 - 1 = SDO1 pin is not used by module; pin functions as I/O
 - 0 = SDO1 pin is controlled by the module
- bit 10 **MODE16:** Word/Byte Communication Select bit
 - 1 = Communication is word-wide (16 bits)
 - 0 = Communication is byte-wide (8 bits)
- bit 9 **SMP:** SPI1 Data Input Sample Phase bit
 - Master mode:
 - 1 = Input data sampled at end of data output time
 - 0 = Input data sampled at middle of data output time
 - Slave mode:
 - SMP must be cleared when SPI1 is used in Slave mode.
- bit 8 **CKE:** SPI1 Clock Edge Select bit⁽¹⁾
 - 1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
 - 0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)
- bit 7 **SSEN:** Slave Select Enable bit (Slave mode)
 - 1 = $\overline{SS1}$ pin used for Slave mode
 - 0 = $\overline{SS1}$ pin not used by module; pin controlled by port function
- bit 6 **CKP:** Clock Polarity Select bit
 - 1 = Idle state for clock is a high level; active state is a low level
 - 0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)
 - 111 = Secondary prescale 1:1
 - 110 = Secondary prescale 2:1
 - .
 - .
 - .
 - 000 = Secondary prescale 8:1

Note 1: The CKE bit is not used in the Framed SPI modes. The user should program this bit to '0' for the Framed SPI modes (FRMEN = 1).

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REGISTER 17-2: U1STA: UART1 STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7						bit 0	

Legend:	C = Clearable bit	HC = Hardware Clearable bit
	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15,13 **UTXISEL<1:0>**: Transmission Interrupt Mode Selection bits
 11 = Reserved; do not use
 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 **UTXINV**: IrDA[®] Encoder Transmit Polarity Inversion bit
 If **IREN** = 0:
 1 = U1TX Idle '0'
 0 = U1TX Idle '1'
 If **IREN** = 1:
 1 = U1TX Idle '1'
 0 = U1TX Idle '0'
- bit 12 **Unimplemented**: Read as '0'
- bit 11 **UTXBRK**: Transmit Break bit
 1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 0 = Sync Break transmission disabled or completed
- bit 10 **UTXEN**: Transmit Enable bit
 1 = Transmit enabled, U1TX pin controlled by UART1
 0 = Transmit disabled, any pending transmission is aborted and buffer is reset. U1TX pin controlled by the PORT register.
- bit 9 **UTXBF**: Transmit Buffer Full Status bit (read-only)
 1 = Transmit buffer is full
 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT**: Transmit Shift Register Empty bit (read-only)
 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 **URXISEL<1:0>**: Receive Interrupt Mode Selection bits
 11 = Interrupt is set on RSR transfer, making the receive buffer full (i.e., has 4 data characters)
 10 = Interrupt is set on RSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 0x = Interrupt is set when any character is received and transferred from the RSR to the receive buffer. Receive buffer has one or more characters.

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REGISTER 18-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
 1 = HLVD enabled
 0 = HLVD disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12-8 **Unimplemented:** Read as '0'
- bit 7 **VDIR:** Voltage Change Direction Select bit
 1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
 0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)
- bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
 1 = Indicates that the band gap voltage is stable
 0 = Indicates that the band gap voltage is unstable
- bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
 1 = Indicates that the internal reference voltage is stable and the high-voltage detect logic generates the interrupt flag at the specified voltage range
 0 = Indicates that the internal reference voltage is unstable and the high-voltage detect logic will not generate the interrupt flag at the specified voltage range, and the HLVD interrupt should not be enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits
 1111 = External analog input is used (input comes from the HLVDIN pin)
 1110 = Trip point 1⁽¹⁾
 1101 = Trip point 2⁽¹⁾
 1100 = Trip point 3⁽¹⁾
 .
 .
 .
 0000 = Trip point 15⁽¹⁾

Note 1: For actual trip point, refer to **Section 26.0 “Electrical Characteristics”**.

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Measurement Unit, refer to the “PIC24F Family Reference Manual”, Section 11. “Charge Time Measurement Unit (CTMU)” (DS39724).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Four edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- Time measurement resolution of one nanosecond
- Accurate current source suitable for capacitive measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance, or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through two registers, CTMUCON and CTMUICON. CTMUCON enables the module, and controls edge source selection, edge source polarity selection, and edge sequencing. The CTMUICON register selects the current range of current source and trims the current.

22.1 Measuring Capacitance

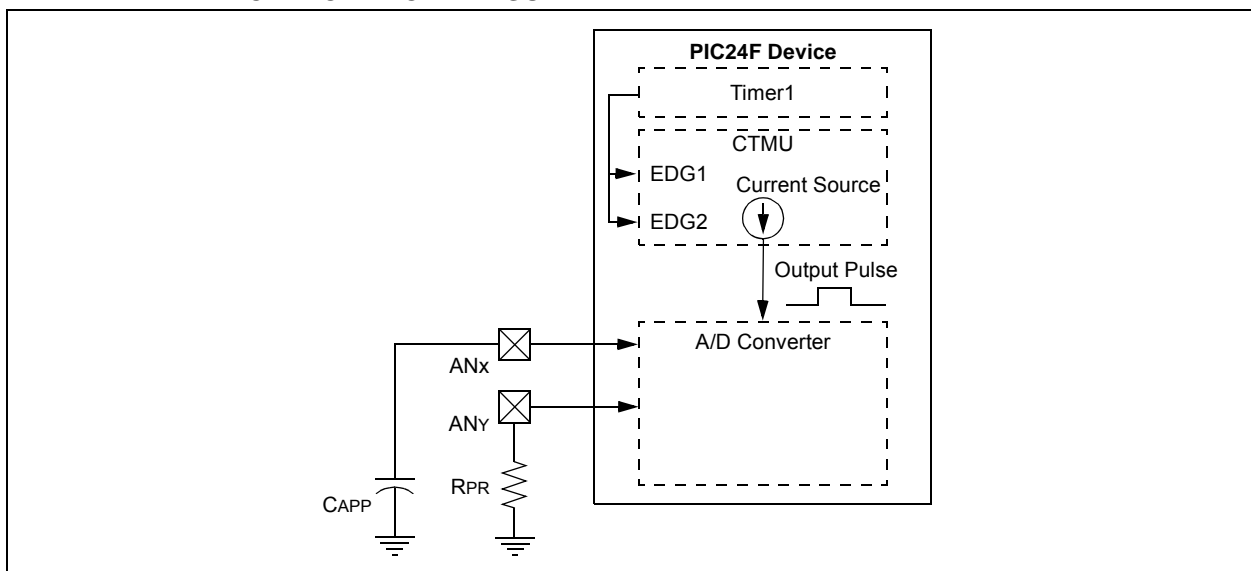
The CTMU module measures capacitance by generating an output pulse with a width equal to the time between edge events on two separate input channels. The pulse edge events to both input channels can be selected from four sources: two internal peripheral modules (OC1 and Timer1) and two external pins (CTEDG1 and CTEDG2). This pulse is used with the module’s precision current source to calculate capacitance according to the relationship:

$$C = I \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an external capacitor (CAPP) on one of its input channels after the CTMU output’s pulse. A precision resistor (RPR) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 22-1 displays the external connections used for capacitance measurements, and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the “PIC24F Family Reference Manual”.

FIGURE 22-1: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR CAPACITANCE MEASUREMENT



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REGISTER 23-7: FDS: DEEP SLEEP CONFIGURATION REGISTER

R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
DSWDTEN	DSLBPOR	—	—	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
 1 = DSWDT enabled
 0 = DSWDT disabled
- bit 6 **DSLBPOR:** Deep Sleep/Low-Power BOR Enable bit (does not affect operation in non Deep Sleep modes)
 1 = Deep Sleep BOR enabled in Deep Sleep
 0 = Deep Sleep BOR disabled in Deep Sleep
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **DSWDTPS<3:0>:** Deep Sleep Watchdog Timer Postscale Select bits
 The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms.
 1111 = 1:2,147,483,648 (25.7 days) nominal
 1110 = 1:536,870,912 (6.4 days) nominal
 1101 = 1:134,217,728 (38.5 hours) nominal
 1100 = 1:33,554,432 (9.6 hours) nominal
 1011 = 1:8,388,608 (2.4 hours) nominal
 1010 = 1:2,097,152 (36 minutes) nominal
 1001 = 1:524,288 (9 minutes) nominal
 1000 = 1:131,072 (135 seconds) nominal
 0111 = 1:32,768 (34 seconds) nominal
 0110 = 1:8,192 (8.5 seconds) nominal
 0101 = 1:2,048 (2.1 seconds) nominal
 0100 = 1:512 (528 ms) nominal
 0011 = 1:128 (132 ms) nominal
 0010 = 1:32 (33 ms) nominal
 0001 = 1:8 (8.3 ms) nominal
 0000 = 1:2 (2.1 ms) nominal

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23.2 Watchdog Timer (WDT)

For the PIC24F04KA201 family of devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

The nominal WDT clock source from LPRC is 31 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the FWPSA Configuration bit. With a 31 kHz input, the prescaler yields a nominal WDT time-out period (T_{WDT}) of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the Configuration bits, $WDTPS<3:0>$ ($FWDT<3:0>$), which allow the selection of a total of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a `PWRSVAV` instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a `CLRWDT` instruction during normal execution

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake the device and code execution will continue from where the `PWRSVAV` instruction was

executed. The corresponding SLEEP or IDLE bits ($RCON<3:2>$) will need to be cleared in software after the device wakes up.

The WDT Flag bit, $WDTO$ ($RCON<4>$), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note: The `CLRWDT` and `PWRSVAV` instructions clear the prescaler and postscaler counts when executed.

23.2.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, `CLRWDT` instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A `CLRWDT` instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

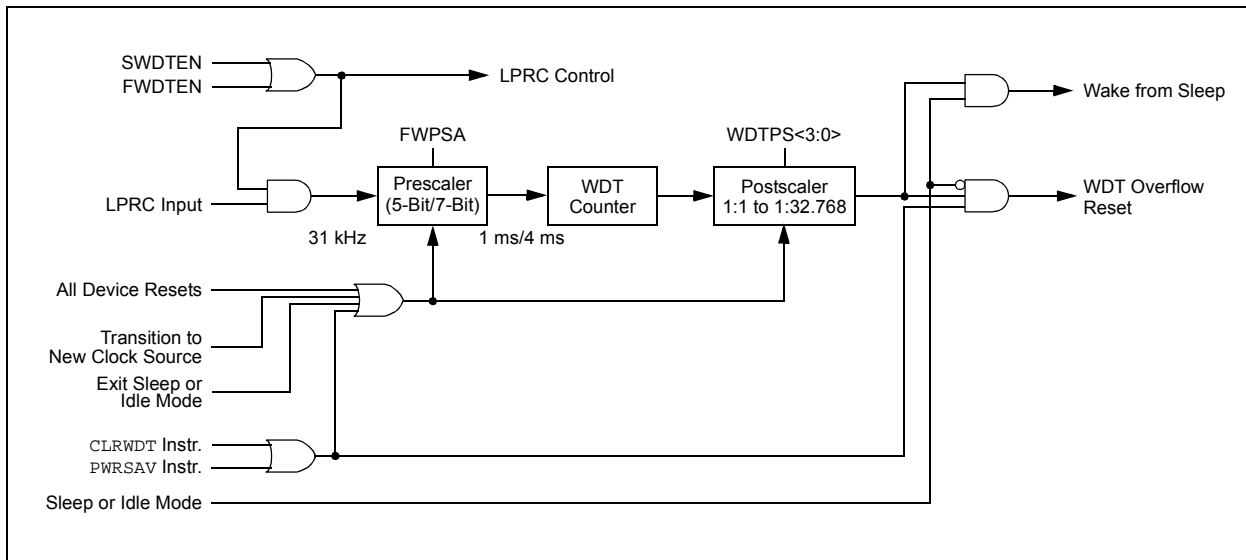
Windowed WDT mode is enabled by programming the Configuration bit, $WINDIS$ ($FWDT<6>$), to '0'.

23.2.2 CONTROL REGISTER

The WDT is enabled or disabled by the $FWDTEN$ Configuration bit. When the $FWDTEN$ Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the $FWDTEN$ Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the $SWDTEN$ control bit ($RCON<5>$). The $SWDTEN$ control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

FIGURE 23-1: WDT BLOCK DIAGRAM



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26.1 DC Characteristics

FIGURE 26-1: PIC24F04KA201 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

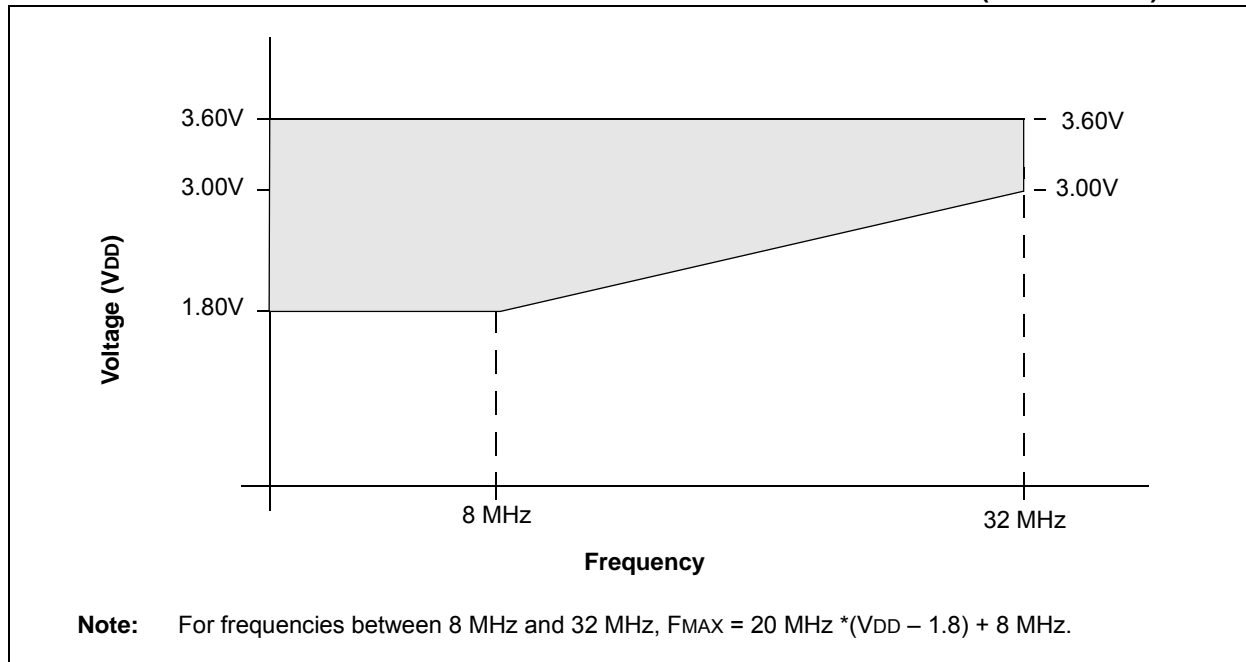


TABLE 26-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Operating Junction Temperature Range	T _J	-40	—	+125	°C
Operating Ambient Temperature Range	T _A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	PD	P _{INT} + P _{I/O}			W
Maximum Allowed Power Dissipation	PD _{MAX}	$(T_J - T_A) / \theta_{JA}$			W

TABLE 26-2: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 14-Pin PDIP	θ _{JA}	62.4	—	°C/W	1
Package Thermal Resistance, 20-Pin PDIP	θ _{JA}	60	—	°C/W	1
Package Thermal Resistance, 14-Pin SSOP	θ _{JA}	108	—	°C/W	1
Package Thermal Resistance, 20-Pin SSOP	θ _{JA}	71	—	°C/W	1
Package Thermal Resistance, 14-Pin SOIC	θ _{JA}	75	—	°C/W	1
Package Thermal Resistance, 20-Pin SOIC	θ _{JA}	80.2	—	°C/W	1
Package Thermal Resistance, 14-Pin QFN	θ _{JA}	43	—	°C/W	1
Package Thermal Resistance, 20-Pin QFN	θ _{JA}	32	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

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TABLE 26-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Parameter No.	Typical ⁽¹⁾	Max	Units	Conditions		
IDD Current						
DC31	8	28	μA	-40°C	1.8V	LPRC (31 kHz)
DC31a		28		$+25^{\circ}\text{C}$		
DC31b		28		$+60^{\circ}\text{C}$		
DC31c		28		$+85^{\circ}\text{C}$		
DC31d	15	55	μA	-40°C	3.3V	
DC31e		55		$+25^{\circ}\text{C}$		
DC31f		55		$+60^{\circ}\text{C}$		
DC31g		55		$+85^{\circ}\text{C}$		

Note 1: Data in "Typical" column is at 3.3V, $+25^{\circ}\text{C}$ unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:

- EC mode with clock input driven with a square wave rail-to-rail
- I/O configured as outputs driven low
- $\overline{\text{MCLR}} - V_{\text{DD}}$
- WDT FSCM disabled
- SRAM, program and data memory active
- All PMD bits set except for modules being measured

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param No.	Typical ⁽¹⁾	Max	Units	Conditions		
Idle Current (I_{IDLE}): Core Off, Clock On Base Current, PMD Bits are Set⁽²⁾						
DC40	48	100	μA	-40°C	1.8V	0.5 MIPS, Fosc = 1 MHz
DC40a		100		$+25^{\circ}\text{C}$		
DC40b		100		$+60^{\circ}\text{C}$		
DC40c		100		$+85^{\circ}\text{C}$		
DC40d	106	215	μA	-40°C	3.3V	
DC40e		215		$+25^{\circ}\text{C}$		
DC40f		215		$+60^{\circ}\text{C}$		
DC40g		215		$+85^{\circ}\text{C}$		

Note 1: Data in "Typical" column is at 3.3V, $+25^{\circ}\text{C}$ unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:

- Core off
- EC mode with clock input driven with a square wave rail-to-rail
- I/O configured as outputs driven low
- $\overline{\text{MCLR}} - V_{\text{DD}}$
- WDT FSCM disabled
- SRAM, program and data memory active
- All PMD bits set except for modules being measured

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FIGURE 26-3: EXTERNAL CLOCK TIMING

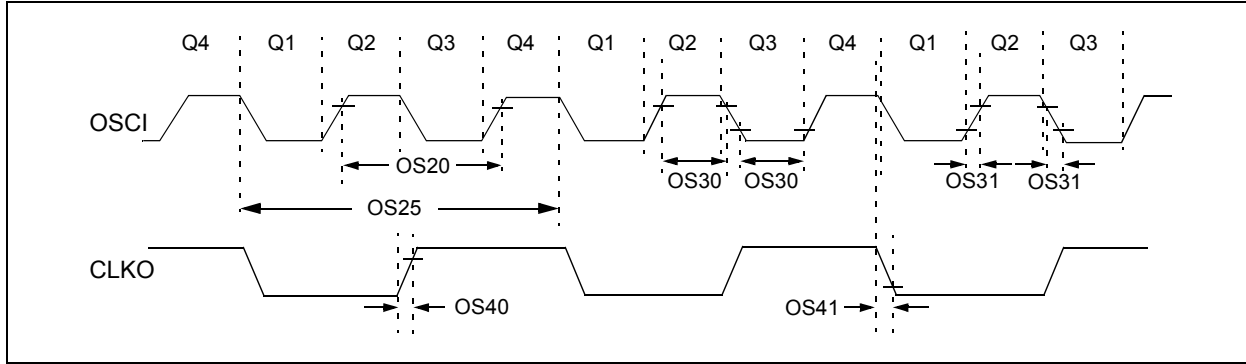


TABLE 26-19: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8 to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC mode)	DC 4	— —	32 8	MHz MHz	EC ECPLL
		Oscillator Frequency	0.2 4 4 31	— — — —	4 25 8 33	MHz MHz MHz kHz	XT HS HSPLL SOSC
OS20	Tosc	$T_{osc} = 1/F_{osc}$	—	—	—	—	See Parameter OS10 for Fosc value
OS25	Tcy	Instruction Cycle Time ⁽²⁾	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x TOSC	—	—	ns	EC
		External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ⁽³⁾	—	6	10	ns	
OS41	TckF	CLKO Fall Time ⁽³⁾	—	6	10	ns	

- Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.
- 3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 Tcy) and high for the Q3-Q4 period (1/2 Tcy).

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TABLE 26-20: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 1.8V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Sym	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range	4	—	8	MHz	ECPLL, HSPLL modes
OS51	FSYS	PLL Output Frequency Range	16	—	32	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	
OS53	DCLK	CLKO Stability (Jitter)	-2	1	2	%	Measured over 100 ms period

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 26-21: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F20	Internal FRC Accuracy @ 8 MHz ⁽¹⁾					
	FRC	-2	—	2	%	+25°C
		-5	—	5	%	-40°C ≤ TA ≤ +85°C
						3.0V ≤ V _{DD} ≤ 3.6V

Note 1: Frequency calibrated at +25°C and 3.3V. OSCTUN bits can be used to compensate for temperature drift.

TABLE 26-22: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F21	LPRC @ 31 kHz ⁽¹⁾					
		-15	—	15	%	+25°C
		-15	—	15	%	-40°C ≤ TA ≤ +85°C
						3.0V ≤ V _{DD} ≤ 3.6V

Note 1: Change of LPRC frequency as V_{DD} changes.

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