What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (1.375K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24f04ka201t-i-ss

NOTES:

PIC24F04KA201 FAMILY

3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HSC
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0, HSC[1]	R/W-0, HSC[1]	R/W-0, HSC[1]	R-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC
IPL2[2]	IPL1[2]	IPL0[2]	RA	N	OV	Z	C
bit 7							bit 0

Legend:		HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9   **Unimplemented:** Read as '0'

bit 8   **DC:** ALU Half Carry/Borrow bit
             1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
             0 = No carry-out from the 4th or 8th low-order bit of the result has occurred

bit 7-5   **IPL<2:0>:** CPU Interrupt Priority Level Status bits[1,2]
             111 = CPU interrupt priority level is 7 (15); user interrupts disabled
             110 = CPU interrupt priority level is 6 (14)
             101 = CPU Interrupt priority Level is 5 (13)
             100 = CPU interrupt priority level is 4 (12)
             011 = CPU interrupt priority level is 3 (11)
             010 = CPU interrupt priority level is 2 (10)
             001 = CPU interrupt priority level is 1 (9)
             000 = CPU interrupt priority level is 0 (8)

bit 4   **RA:** REPEAT Loop Active bit
             1 = REPEAT loop in progress
             0 = REPEAT loop not in progress

bit 3   **N:** ALU Negative bit
             1 = Result was negative
             0 = Result was non-negative (zero or positive)

bit 2   **OV:** ALU Overflow bit
             1 = Overflow occurred for signed (2's complement) arithmetic in this arithmetic operation
             0 = No overflow has occurred

bit 1   **Z:** ALU Zero bit
             1 = An operation, which effects the Z bit, has set it at some time in the past
             0 = The most recent operation, which effects the Z bit, has cleared it (i.e., a non-zero result)

bit 0   **C:** ALU Carry/Borrow bit
             1 = A carry-out from the Most Significant bit (MSb) of the result occurred
             0 = No carry-out from the Most Significant bit (MSb) of the result occurred

Note 1: The IPL Status bits are read-only when NSTDIS (INTCON1<15>) = 1.
   2: The IPL Status bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

REGISTER 3-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0, HSC	R/W-0	U-0	U-0
—	—	—	—	IPL3[1]	PSV	—	—
bit 7							bit 0

Legend:		HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit[1]

1 = CPU interrupt priority level is greater than 7
0 = CPU interrupt priority level is 7 or less

bit 2 **PSV:** Program Space Visibility in Data Space Enable bit

1 = Program space visible in data space
0 = Program space not visible in data space

bit 1-0 **Unimplemented:** Read as '0'

Note 1: User interrupts are disabled when IPL3 = 1.

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware division for 16-bit divisor.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

PIC24F04KA201 FAMILY

TABLE 4-9: I²C™ REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	I2C1 Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK9	AMSK8	AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: UART REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									0000
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: SPI REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	SPIFPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit/Receive Buffer																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.3.2 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the program memory without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a program space word as data.

The PC is incremented by 2 for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word-wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the least significant data word, and TBLRDH and TBLWTH access the space which contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from program space. Both function as either byte or word operations.

1. TBLRDL (Table Read Low): In Word mode, it maps the lower word of the program space location (P<15:0>) to a data address (D<15:0>).

    In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when byte select is '1'; the lower byte is selected when it is '0'.

2. TBLRDH (Table Read High): In Word mode, it maps the entire upper word of a program address (P<23:16>) to a data address. Note that D<15:8>, the 'phantom' byte, will always be '0'.

    In Byte mode, it maps the upper or lower byte of the program word to D<7:0> of the data address, as above. Note that the data will always be '0' when the upper 'phantom' byte is selected (byte select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a program space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Memory Page Address register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

Note:	Only table read operations will execute in the configuration memory space, and only then, in implemented areas such as the Device ID. Table write operations are not allowed.

FIGURE 4-6: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS
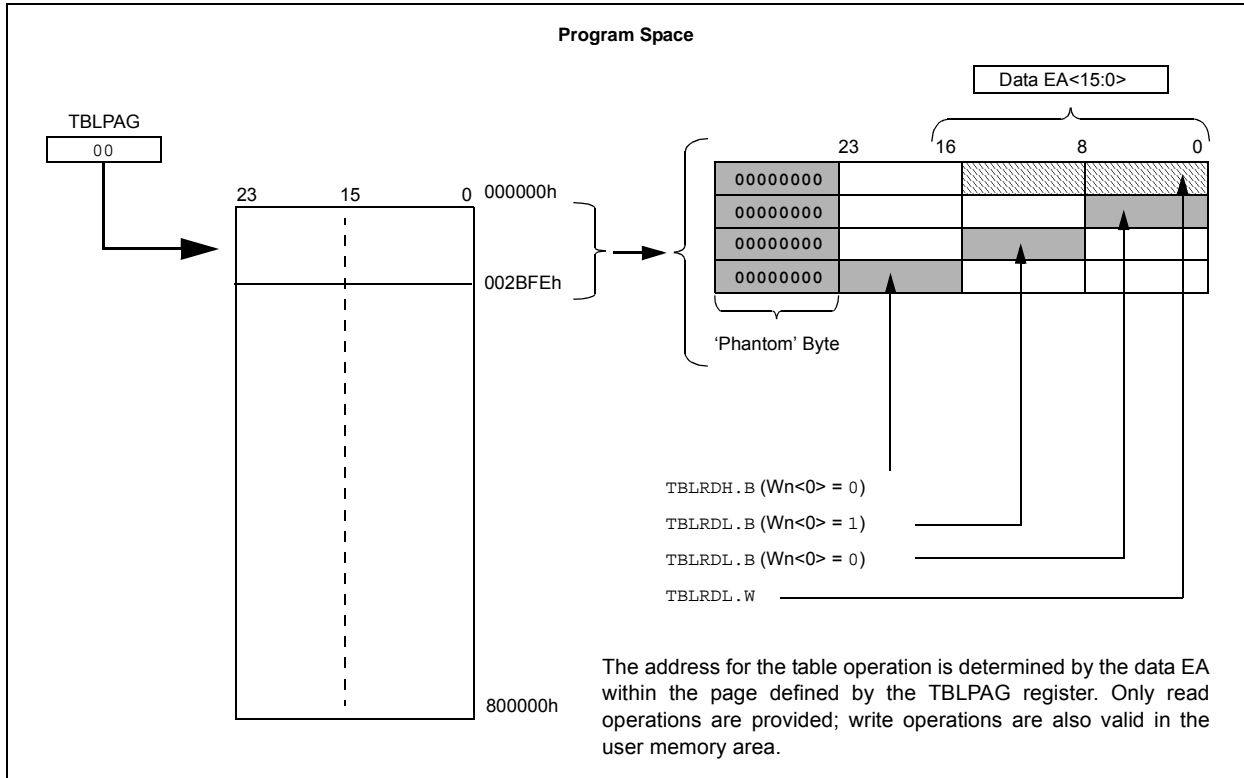
4.3.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into an 8K word page (in PIC24F08KA1XX devices) and a 16K word page (in PIC24F16KA1XX devices) of the program space. This provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the MSb of the data space EA is '1', and PSV is enabled by setting the PSV bit in the CPU Control (CORCON<2>) register. The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page Address register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits.

By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads from this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-7), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space locations used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

> **Note:** PSV access is temporarily disabled during table reads/writes.

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

8.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

> **Note:** The primary oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMDx Configuration bits. While an application can switch to and from primary oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

8.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to '0'. (Refer to **Section 23.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and FSCM function are disabled. This is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSCx bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

8.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSCx bits (OSCCON<14:12>), to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM with LPRC as a clock source is enabled) or SOSC (if SOSCEN remains enabled).

> **Note 1:** The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
>
> **2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

9.2.4.5 Deep Sleep WDT

To enable the DSWDT in Deep Sleep mode, program the Configuration bit, DSWDTEN (FDS<7>). The device Watchdog Timer (WDT) need not be enabled for the DSWDT to function. Entry into Deep Sleep mode automatically resets the DSWDT.

The DSWDT clock source is selected by the DSWDTOSC Configuration bit (FDS<4>). The postscaler options are programmed by the DSWDTPS<3:0> Configuration bits (FDS<3:0>). The minimum time-out period that can be achieved is 2.1 ms and the maximum is 25.7 days. For more details on the FDS Configuration register and DSWDT configuration options, refer to **Section 23.0 "Special Features"**.

9.2.4.6 Switching Clocks in Deep Sleep Mode

The DSWDT may run from either SOSC or the LPRC clock source. This allows the DSWDT to run without requiring both the LPRC and SOSC to be enabled together, reducing power consumption.

Under certain circumstances, it is possible for the DSWDT clock source to be off when entering Deep Sleep mode. In this case, the clock source is turned on automatically (if DSWDT is enabled), without the need for software intervention. However, this can cause a delay in the start of the DSWDT counters. In order to avoid this delay when using SOSC as a clock source, the application can activate SOSC prior to entering Deep Sleep mode.

9.2.4.7 Checking and Clearing the Status of Deep Sleep

Upon entry into Deep Sleep mode, the status bit, DPSLP (RCON<10>), becomes set and must be cleared by the software.

On power-up, the software should read this status bit to determine if the Reset was due to an exit from Deep Sleep mode and clear the bit if it is set. Of the four possible combinations of DPSLP and POR bit states, three cases can be considered:

• Both the DPSLP and POR bits are cleared. In this case, the Reset was due to some event other than a Deep Sleep mode exit.

• The DPSLP bit is clear, but the POR bit is set. This is a normal POR.

• Both the DPSLP and POR bits are set. This means that Deep Sleep mode was entered, the device was powered down and Deep Sleep mode was exited.

9.2.4.8 Power-on Resets (PORs)

V_{DD} voltage is monitored to produce PORs. Since exiting from Deep Sleep functionally looks like a POR, the technique described in **Section 9.2.4.7 "Checking and Clearing the Status of Deep Sleep"** should be used to distinguish between Deep Sleep and a true POR event.

When a true POR occurs, the entire device including all Deep Sleep logic, (Deep Sleep registers, DSWDT, etc.) is reset.

9.2.4.9 Summary of Deep Sleep Sequence

To review, these are the necessary steps involved in invoking and exiting Deep Sleep mode:

1. Device exits Reset and begins to execute its application code.
2. If DSWDT functionality is required, program the appropriate Configuration bit.
3. Select the appropriate clock(s) for the DSWDT (optional).
4. Enable and configure the DSWDT (optional).
5. Write context data to the DSGPRx registers (optional).
6. Enable the INT0 interrupt (optional).
7. Set the DSEN bit in the DSCON register.
8. Enter Deep Sleep by issuing a `PWRSV #SLEEP_MODE` command.
9. Device exits Deep Sleep when a wake-up event occurs.
10. The DSEN bit is automatically cleared.
11. Read and clear the DPSLP status bit in RCON, and the DSWAKE status bits.
12. Read the DSGPRx registers (optional).
13. Once all state related configurations are complete, clear the RELEASE bit.
14. Application resumes normal operation.

10.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum V$_{IH}$ specification.

10.2 Configuring Analog Port Pins

The use of the AD1PCFG and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V$_{OH}$ or V$_{OL}$) will be converted.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

10.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

10.3 Input Change Notification

The input change notification function of the I/O ports allows the PIC24F04KA201 family of devices to generate interrupt requests to the processor in response to a change of state on selected input pins. This feature is capable of detecting input change of states even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 17 external signals (11 on 14-pin devices) that may be selected (enabled) for generating an interrupt request on a change of state.

There are six control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up/pull-down connected to it. The pull-ups act as a current source that is connected to the pin and the pull-downs act as a current sink to eliminate the need for external resistors when push button or keypad devices are connected.

On any pin, only the pull-up resistor or the pull-down resistor should be enabled, but not both of them. If the push button or the keypad is connected to V$_{DD}$, enable the pull-down, or if they are connected to V$_{SS}$, enable the pull-up resistors. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins.

Setting any of the control bits enables the weak pull-ups for the corresponding pins. The pull-downs are enabled separately using the CNPD1 and CNPD2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-downs for the corresponding pins.

When the internal pull-up is selected, the pin uses V$_{DD}$ as the pull-up source voltage. When the internal pull-down is selected, the pins are pulled down to V$_{SS}$ by an internal resistor. Make sure that there is no external pull-up source/pull-down sink when the internal pull-ups/pull-downs are enabled.

> **Note:** Pull-ups and pull-downs on change notification pins should always be disabled whenever the port pin is configured as a digital output.

EXAMPLE 10-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0;         //Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
MOV    W0, TRISBB;
NOP;                       //Delay 1 cycle
BTSS   PORTB, #13;         //Next Instruction


Equivalent 'C' Code
TRISB = 0xFF00;            //Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
NOP();                     //Delay 1 cycle
if(PORTBbits.RB13 == 1)    // execute following code if PORTB pin 13 is set.
{
}
```

REGISTER 14-2:   PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	—	—	SMBUSDEL[2]	OC1TRIS[1]	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5   **Unimplemented:** Read as '0'

bit 3   **OC1TRIS:** OC1 Output Tri-State Select bit[1]

            1 = OC1 output will not be active on the pin; OCPWM1 can still be used for internal triggers
            0 = OC1 output will be active on the pin based on the OCPWM1 module settings

bit 2-0   **Unimplemented:** Read as '0'

Note 1:   To enable the actual OC1 output, the OCPWM1 module has to be enabled.

      2:   Bit 4 is described in **Section 16.0 "Inter-Integrated Circuit (I2C™)"**.

16.0   INTER-INTEGRATED CIRCUIT (I^2C™)

> **Note:**   This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Inter-Integrated Circuit, refer to the *"PIC24F Family Reference Manual"*, **Section 24. "Inter-Integrated Circuit (I^2C™)"** (DS39702).

The Inter-Integrated Circuit (I^2C™) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial data EEPROMs, display drivers, A/D Converters, etc.

The I^2C module supports these features:

• Independent master and slave logic
• 7-bit and 10-bit device addresses
• General call address, as defined in the I^2C protocol
• Clock stretching to provide delays for the processor to respond to a slave data request
• Both 100 kHz and 400 kHz bus specifications
• Configurable address masking
• Multi-Master modes to prevent loss of messages in arbitration
• Bus Repeater mode, allowing the acceptance of all messages as a slave regardless of the address
• Automatic SCL

Figure 16-1 illustrates a block diagram of the module.

16.1   Pin Remapping Options

The I^2C module is tied to a fixed pin. To allow flexibility with peripheral multiplexing, the I2C1 module in 20-pin devices can be reassigned to the alternate pins, designated as SCL1 and SDA1 during device configuration.

Pin assignment is controlled by the I2C1SEL Configuration bit. Programming this bit (= 0) multiplexes the module to the SCL1 and SDA1 pins.

16.2   Communicating as a Master in a Single Master Environment

The details of sending a message in Master mode depends on the communications protocol for the device being communicated with. Typically, the sequence of events is as follows:

1. Assert a Start condition on SDA1 and SCL1.
2. Send the I^2C device address byte to the slave with a write indication.
3. Wait for and verify an Acknowledge from the slave.
4. Send the first data byte (sometimes known as the command) to the slave.
5. Wait for and verify an Acknowledge from the slave.
6. Send the serial memory address low byte to the slave.
7. Repeat steps 4 and 5 until all data bytes are sent.
8. Assert a Repeated Start condition on SDA1 and SCL1.
9. Send the device address byte to the slave with a read indication.
10. Wait for and verify an Acknowledge from the slave.
11. Enable master reception to receive serial memory data.
12. Generate an ACK or NACK condition at the end of a received byte of data.
13. Generate a Stop condition on SDA1 and SCL1.

REGISTER 16-1: I2C1CON: I2C1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2C1 Enable bit

1 = Enables the I2C1 module and configures the SDA1 and SCL1 pins as serial port pins
0 = Disables the I2C1 module; all I^{2}C™ pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** Stop in Idle Mode bit

1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCL1 Release Control bit (when operating as I^{2}C slave)

1 = Releases SCL1 clock
0 = Holds SCL1 clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software may write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software may only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit

1 = IPMI Support mode is enabled; all addresses Acknowledged
0 = IPMI Support mode is disabled

bit 10 **A10M:** 10-Bit Slave Addressing bit

1 = I2C1ADD is a 10-bit slave address
0 = I2C1ADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit

1 = Slew rate control disabled
0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit

1 = Enables I/O pin thresholds compliant with the SMBus specification
0 = Disables the SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^{2}C slave)

1 = Enables interrupt when a general call address is received in the I2C1RSR (module is enabled for reception)
0 = General call address disabled

bit 6 **STREN:** SCL1 Clock Stretch Enable bit (when operating as I^{2}C slave)

Used in conjunction with the SCLREL bit.
1 = Enables software or receive clock stretching
0 = Disables software or receive clock stretching

17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Universal Asynchronous Receiver Transmitter, refer to the *"PIC24F Family Reference Manual"*, **Section 21. "UART"** (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in this PIC24F device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. This module also supports a hardware flow control option with the U1CTS and U1RTS pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

• Full-Duplex, 8-Bit or 9-Bit Data Transmission through the U1TX and U1RX pins
• Even, Odd or No Parity Options (for 8-bit data)
• One or Two Stop bits
• Hardware Flow Control Option with U1CTS and U1RTS pins

• Fully Integrated Baud Rate Generator (IBRG) with 16-Bit Prescaler
• Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
• 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
• 4-Deep FIFO Receive Data Buffer
• Parity, Framing and Buffer Overrun Error Detection
• Support for 9-Bit mode with Address Detect (9th bit = 1)
• Transmit and Receive Interrupts
• Loopback mode for Diagnostic Support
• Support for Sync and Break Characters
• Supports Automatic Baud Rate Detection
• IrDA Encoder and Decoder Logic
• 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UART is displayed in Figure 17-1. The UART module consists of these important hardware elements:

• Baud Rate Generator
• Asynchronous Transmitter
• Asynchronous Receiver

FIGURE 17-1: UART SIMPLIFIED BLOCK DIAGRAM
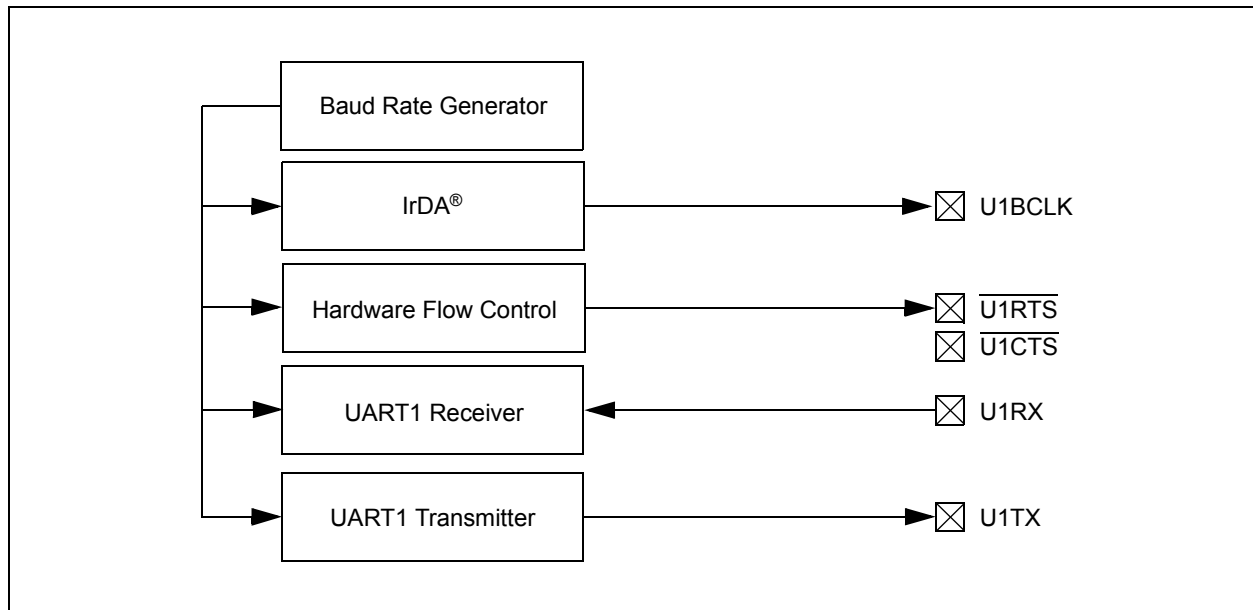
23.0 SPECIAL FEATURES

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Watchdog Timer, High-Level Device Integration and Programming Diagnostics, refer to the individual sections of the *"PIC24F Family Reference Manual"* provided below:
>
> • **Section 9. "Watchdog Timer (WDT)"** (DS39697)
> • **Section 36. "High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
> • **Section 33. "Programming and Diagnostics"** (DS39716)

PIC24F04KA201 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

• Flexible Configuration
• Watchdog Timer (WDT)
• Code Protection
• In-Circuit Serial Programming™ (ICSP™)
• In-Circuit Emulation

23.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location, F80000h. A complete list is provided in Table 23-1. A detailed explanation of the various bit functions is provided in Register 23-1 through Register 23-7.

The address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using table reads and table writes.

TABLE 23-1:   CONFIGURATION REGISTERS LOCATIONS

Configuration Register	Address
FGS	F80004
FOSCSEL	F80006
FOSC	F80008
FWDT	F8000A
FPOR	F8000C
FICD	F8000E
FDS	F80010

REGISTER 23-1:   FGS: GENERAL SEGMENT CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/C-1	R/C-1
—	—	—	—	—	—	GSS0	GWRP
bit 7							bit 0

Legend:		
R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2   **Unimplemented:** Read as '0'

bit 1   **GSS0:** General Segment Code Flash Code Protection bit

1 = No protection
0 = Standard security enabled

bit 0   **GWRP**: General Segment Code Flash Write Protection bit

1 = General segment may be written
0 = General segment is write-protected

TABLE 26-5: BOR TRIP POINTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial							
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC19		BOR Voltage on VDD Transition	BOR = 00	1.55	2	2.00	V	Valid for LPBOR and DSBOR
			BOR = 01	2.92	3	3.25	V	
			BOR = 10	2.63	2.7	2.92	V	
			BOR = 11	1.75	1.78	2.01	V	

TABLE 26-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Parameter No.	Typical[1]	Max	Units	Conditions	
IDD Current					
DC20	195	330	μA	-40°C	1.8V	0.5 MIPS, FOSC = 1 MHz
DS20a		330		+25°C		
DC20b		330		+60°C		
DC20c		330		+85°C		
DC20d	365	590	μA	-40°C	3.3V	
DC20e		590		+25°C		
DC20f		645		+60°C		
DC20g		720		+85°C		
DC22	363	600	μA	-40°C	1.8V	1 MIPS, FOSC = 2 MHz
DC22a		600		+25°C		
DC22b		600		+60°C		
DC22c		600		+85°C		
DC22d	695	1100	μA	-40°C	3.3V	
DC22e		1100		+25°C		
DC22f		1100		+60°C		
DC22g		1100		+85°C		
DC23	11	18	mA	-40°C	3.3V	16 MIPS, FOSC = 32 MHz
DC23a		18		+25°C		
DC23b		18		+60°C		
DC23c		18		+85°C		
DC27	2.25	3.40	mA	-40°C	2.5V	FRC (4 MIPS), FOSC = 8 MHz
DC27a		3.40		+25°C		
DC27b		3.40		+60°C		
DC27c		3.40		+85°C		
DC27d	3.05	4.60	mA	-40°C	3.3V	
DC27e		4.60		+25°C		
DC27f		4.60		+60°C		
DC27g		4.60		+85°C		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:
- EC mode with clock input driven with a square wave rail-to-rail
- I/O configured as outputs driven low
- $\overline{MCLR}$ – VDD
- WDT FSCM disabled
- SRAM, program and data memory active
- All PMD bits set except for modules being measured

TABLE 26-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS				Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Parameter No.	Typical[1]	Max	Units	Conditions		
Power-Down Current (I_{PD}): PMD Bits are Set, PMSLP Bit is '0'[2]						
DC70	0.045	0.200	µA	-40°C	1.8V	LPBOR[3,4]
DC70a		0.200		+25°C		
DC70b		0.200		+60°C		
DC70c		0.200		+85°C		
DC70d	0.095	0.200	µA	-40°C	3.3V	
DC70e		0.200		+25°C		
DC70f		0.200		+60°C		
DC70g		0.200		+85°C		
DC71	0.35	0.55	µA	-40°C	1.8V	Deep Sleep Watchdog Timer: DSWDT (SOSC – LP)[5]
DC71a		0.55		+25°C		
DC71b		0.55		+60°C		
DC71c		0.55		+85°C		
DC71d	0.55	0.75	µA	-40°C	3.3V	
DC71e		0.75		+25°C		
DC71f		0.75		+60°C		
DC71g		0.75		+85°C		
DC72	0.005	0.200	µA	-40°C	1.8V	Deep Sleep BOR: DSBOR[3,5]
DC72a		0.200		+25°C		
DC72b		0.200		+60°C		
DC72c		0.200		+85°C		
DC72d	0.010	0.200	µA	-40°C	3.3V	
DC72e		0.200		+25°C		
DC72f		0.200		+60°C		
DC72g		0.200		+85°C		

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base I_{PD} is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled high. WDT, etc., are all switched off.

3: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Current applies to Sleep only.

5: Current applies to Deep Sleep only.

PIC24F04KA201 FAMILY

TABLE 26-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
	V_{IL}	**Input Low Voltage**[4]	—	—	—	—	
DI10		I/O Pins	V_{SS}	—	0.2 V_{DD}	V	
DI15		$\overline{MCLR}$	V_{SS}	—	0.2 V_{DD}	V	
DI16		OSCI (XT mode)	V_{SS}	—	0.2 V_{DD}	V	
DI17		OSCI (HS mode)	V_{SS}	—	0.2 V_{DD}	V	
DI18		I/O Pins with I²C™ Buffer	V_{SS}	—	0.3 V_{DD}	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	V_{SS}	—	0.8	V	SMBus enabled
	V_{IH}	**Input High Voltage**[4]	—	—	—	—	
DI20		I/O Pins:					
		with Analog Functions	0.8 V_{DD}	—	V_{DD}	V	
		Digital Only	0.8 V_{DD}	—	V_{DD}	V	
DI25		$\overline{MCLR}$	0.8 V_{DD}	—	V_{DD}	V	
DI26		OSCI (XT mode)	0.7 V_{DD}	—	V_{DD}	V	
DI27		OSCI (HS mode)	0.7 V_{DD}	—	V_{DD}	V	
DI28		I/O Pins with I²C Buffer:					
		with Analog Functions	0.7 V_{DD}	—	V_{DD}	V	
		Digital Only	0.7 V_{DD}	—	V_{DD}	V	
DI29		I/O Pins with SMBus	2.1	—	V_{DD}	V	2.5V ≤ V_{PIN} ≤ V_{DD}
DI30	I_{CNPU}	**CNx Pull-up Current**	50	250	500	μA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
	I_{IL}	**Input Leakage Current**[2,3]					
DI50		I/O Ports	—	0.050	±0.100	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance
DI51		$V_{REF}+$, $V_{REF}-$, AN0, AN1	—	0.300	±0.500	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±5.0	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
DI56		OSCI	—	—	±5.0	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, XT and HS modes

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
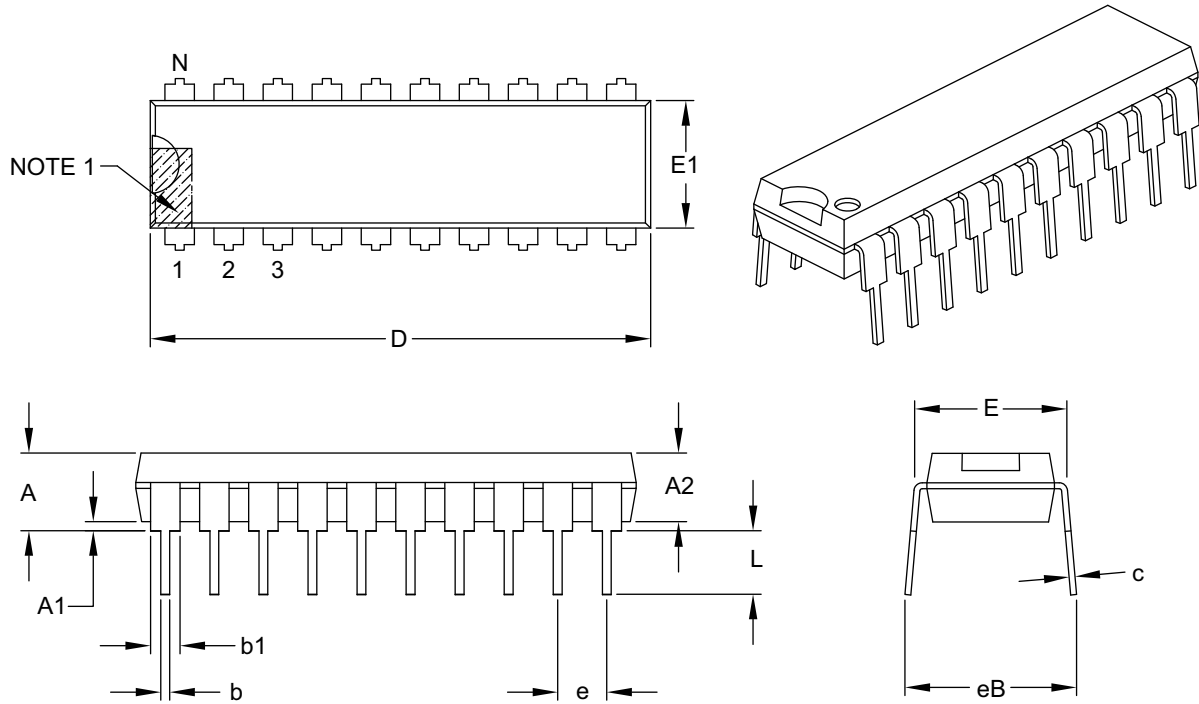
3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-2 for I/O pin buffer types.

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

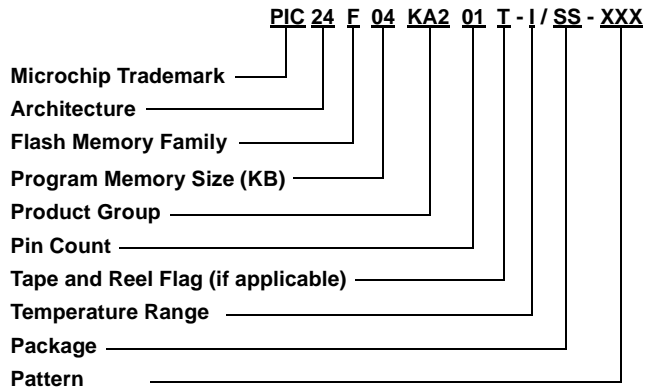4. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC 24 F 04 KA2 01 T - I / SS - XXX

Microchip Trademark
Architecture
Flash Memory Family
Program Memory Size (KB)
Product Group
Pin Count
Tape and Reel Flag (if applicable)
Temperature Range
Package
Pattern

Examples:

a) PIC24F04KA201-I/MQ: General purpose, 16-Kbyte program memory, 20-pin, Industrial temp., QFN package.

Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	F	= Flash program memory
Product Group	KA2	= General purpose microcontrollers
Pin Count	00	= 14-pin
	01	= 20-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
Package	P	= PDIP
	SL	= SOIC, Narrow
	SO	= SOIC
	SS	= SSOP
	MQ	= QFN
	ST	= TSSOP
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	ES	= Engineering Sample

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