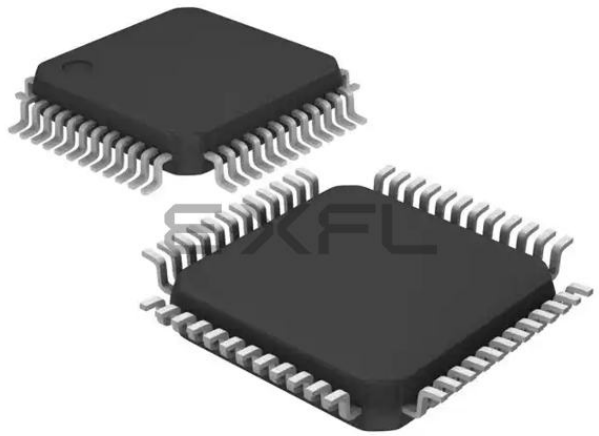

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ll16clf

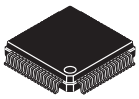
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LL16
Rev. 7, 1/2013

An Energy Efficient Solution by Freescale

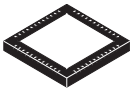
MC9S08LL16 Series

Covers: MC9S08LL16 and MC9S08LL8



64-LQFP
Case 840F

48-LQFP
Case 932



48-QFN
1314

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20-MHz CPU at 3.6V to 1.8V across temperature range of -40°C to 85°C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual Array FLASH read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and FLASH contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents.
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6 usec typical wake up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1MHz to 10 MHz.
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-Voltage Warning with interrupt
  - Low-Voltage Detection with reset or interrupt
  - Illegal opcode and illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — 4x28 or 8x24 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control.
  - **ADC** — 8-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
  - **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
  - **SPI**— Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
  - **IIC** — IIC with up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
  - **TPMx** — Two 2-channel (TPM1 and TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
  - **TOD**— (Time Of Day) 8-bit quarter second counter with match register; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components.
- Input/Output
  - 38 GPIOs, 2 output-only pins
  - 8 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.
- Package Options
  - 64-LQFP, 48-LQFP and 48-QFN

1 Devices in the MC9S08LL16 Series

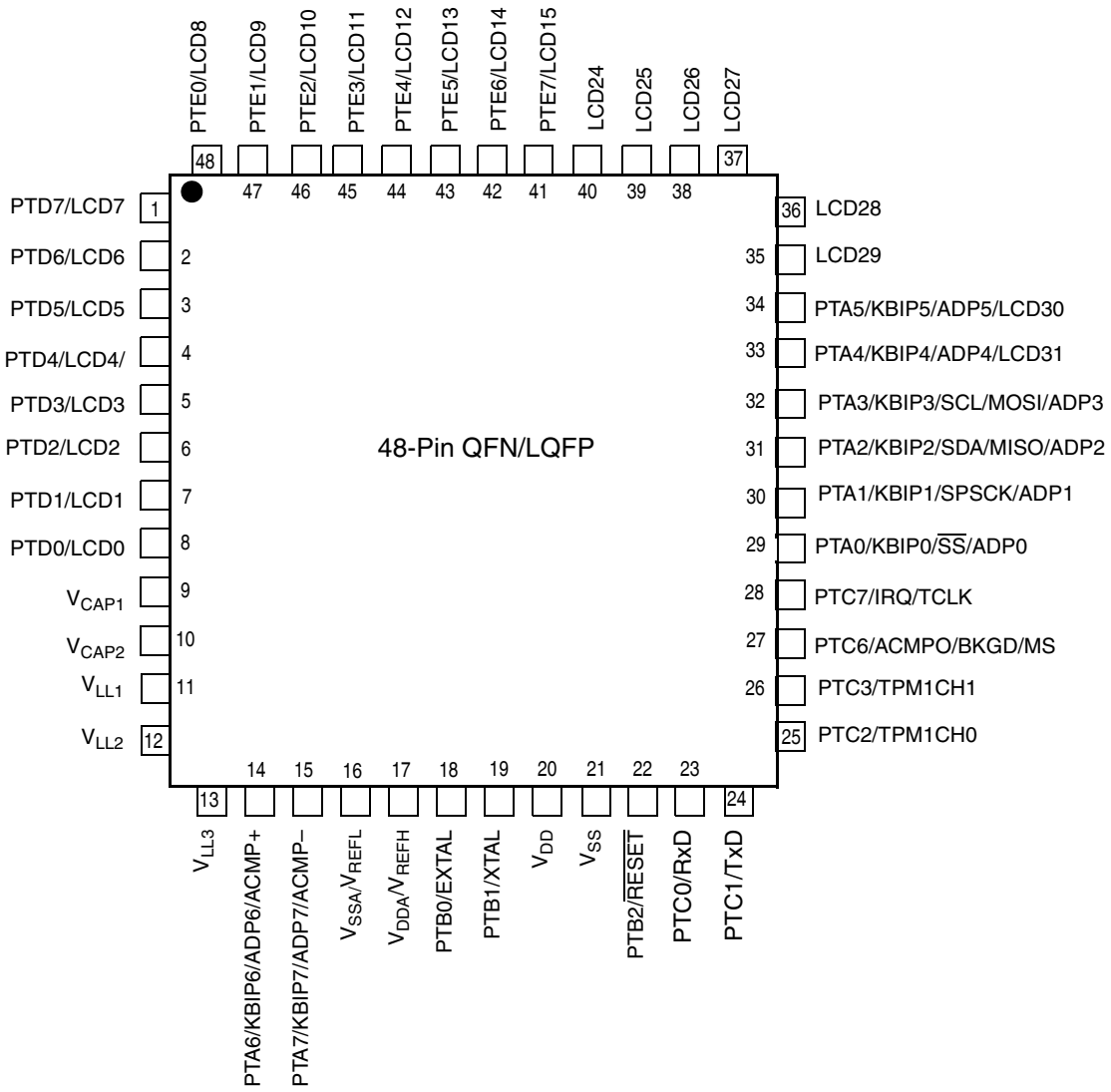
Table 1 summarizes the feature set available in the MC9S08LL16 series of MCUs.

Table 1. MC9S08LL16 Series Features by MCU and Package

Feature	MC9S08LL16		MC9S08LL8
Package	64-pin LQFP	48-pin QFN/LQFP	48-pin QFN/LQFP
FLASH	16,384 (Dual 8K Arrays)		10,240 (8K and 2K arrays)
RAM	2080	2080	2080
ACMP	yes	yes	yes
ADC	8-ch	8-ch	8-ch
IIC	yes	yes	yes
IRQ	yes	yes	yes
KBI	8	8	8
SCI	yes	yes	yes
SPI	yes	yes	yes
TPM1	2-ch	2-ch	2-ch
TPM2	2-ch	-	-
TOD	Yes	Yes	Yes
LCD	8x24 4x28	8x16 4x20	8x16 4x20
I/O pins[1]	38	31	31

1 I/O does not include two output-only port pins.

The block diagram in Figure 1 shows the structure of the MC9S08LL16 series MCU.



Note: V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}

Figure 3. MC9S08LL16 Series in 48-Pin QFN/LQFP Packages

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest **Priority** --> Highest				
64	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	47	PTE1	LCD9			
2	48	PTE0	LCD8			
3	1	PTD7	LCD7			
4	2	PTD6	LCD6			
5	3	PTD5	LCD5			
6	4	PTD4	LCD4			
7	5	PTD3	LCD3			
8	6	PTD2	LCD2			
9	7	PTD1	LCD1			
10	8	PTD0	LCD0			
11	9		V_{cap1}			
12	10		V_{cap2}			
13	11		V_{LL1}			
14	12		V_{LL2}			
15	13		V_{LL3}			
16	—		V_{LCD}			
17	14	PTA6	KBIP6	ADP6	ACMP+	
18	15	PTA7	KBIP7	ADP7	ACMP–	
19	16				V_{SSA}	
					V_{REFL}	
20	17				V_{REFH}	
					V_{DDA}	
21	18	PTB0		EXTAL		
22	19	PTB1		XTAL		
23	20				V_{DD}	
24	21				V_{SS}	
25	22	PTB2	$\overline{\text{RESET}}$			
26	—	PTB3				
27	—	PTB4	—	MISO	SDA	
28	—	PTB5	—	MOSI	SCL	
29	—	PTB6	—	SPSCK		
30	—	PTB7	—	$\overline{\text{SS}}$		
31	23	PTC0		RxD		
32	24	PTC1		TxD		
33	25	PTC2		TPM1CH0		
34	26	PTC3		TPM1CH1		
35	—	PTC4		TPM2CH0		
36	—	PTC5		TPM2CH1		
37	27	PTC6	ACMPO	BKGD	MS	
38	28	PTC7		IRQ	TCLK	
39	29	PTA0	KBIP0	—	$\overline{\text{SS}}$	ADP0

Table 2. Pin Availability by Package Pin-Count (continued)

		<-- Lowest **Priority** --> Highest				
64	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
40	30	PTA1	KBIP1	—	SPSCK	ADP1
41	31	PTA2	KBIP2	SDA	MISO	ADP2
42	32	PTA3	KBIP3	SCL	MOSI	ADP3
43	33	PTA4	KBIP4	ADP4	LCD31	
44	34	PTA5	KBIP5	ADP5	LCD30	
45	35		LCD29			
46	36		LCD28			
47	37		LCD27			
48	38		LCD26			
49	39		LCD25			
50	40		LCD24			
51	—		LCD23			
52	—		LCD22			
53	—		LCD21			
54	—		LCD20			
55			LCD19			
56			LCD18			
57			LCD17			
58			LCD16			
59	41	PTE7	LCD15			
60	42	PTE6	LCD14			
61	43	PTE5	LCD13			
62	44	PTE4	LCD12			
63	45	PTE3	LCD11			
64	46	PTE2	LCD10			

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LL16 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1		Operating voltage			1.8		3.6	V
2	C	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], low-drive strength	V_{OH}	V_{DD} >1.8 V, I_{Load} = –0.6 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7][2], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	C	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –0.5 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
	C			V_{DD} > 1.8 V, I_{Load} = –1 mA	V_{DD} – 0.5	—	—	
4	D	Output high current — Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
5	C	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V_{OL}	V_{DD} >1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P	Output low voltage — PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
6	C	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.5 mA	—	—	0.5	V
	P	Output low voltage — PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
	C			V_{DD} > 1.8 V, I_{Load} = 1 mA	—	—	0.5	
7	D	Output low current — Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
8	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 × V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 × V_{DD}	—	—	
9	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} > 1.8 V	—	—	0.30 x V_{DD}	
10	C	Input hysteresis — all digital inputs	V_{hys}		0.06 × V_{DD}	—	—	mV

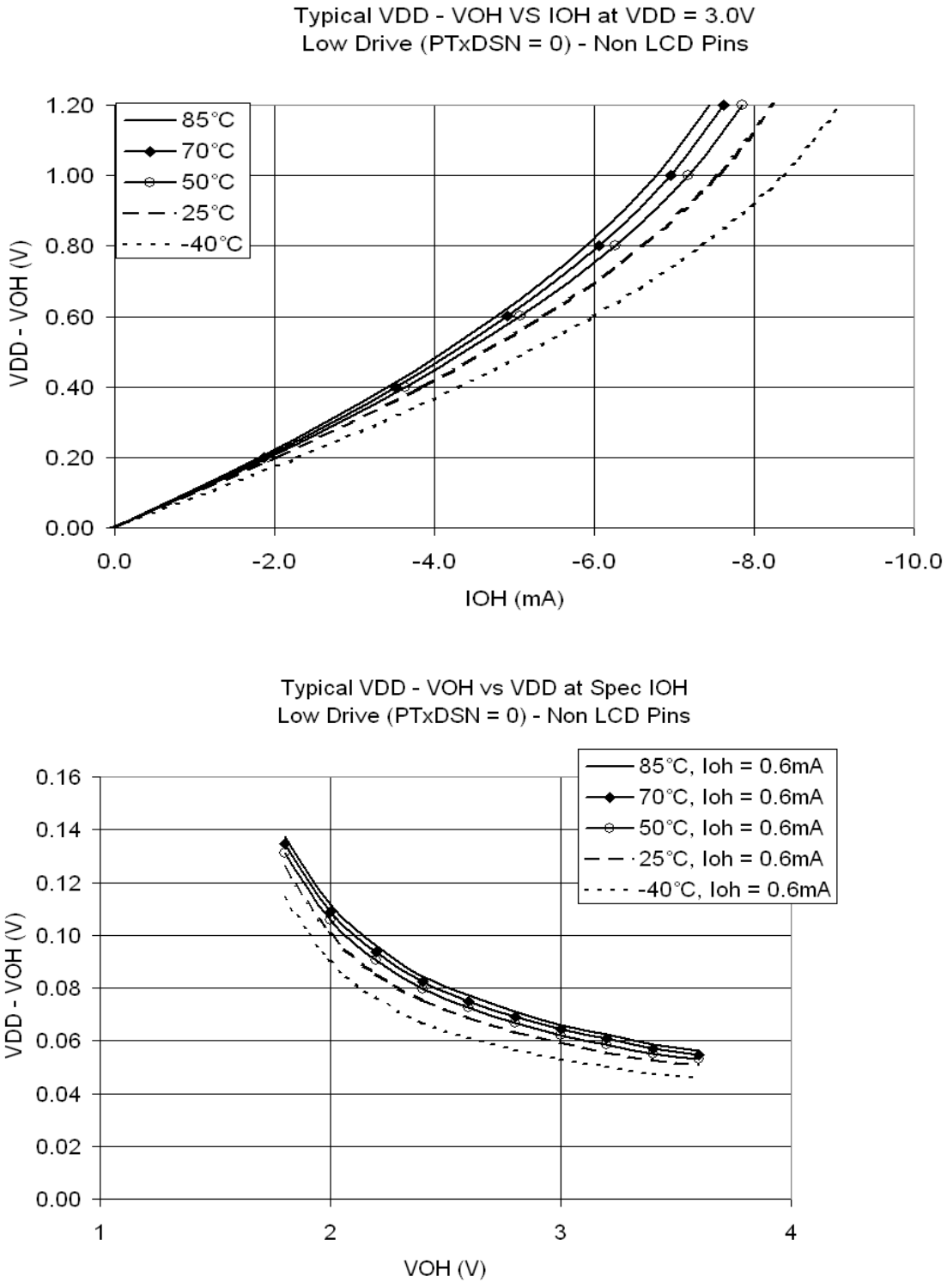


Figure 8. Typical High-Side (Source) Characteristics (Non-LCD Pins) — Low Drive (PTxDSn = 0)

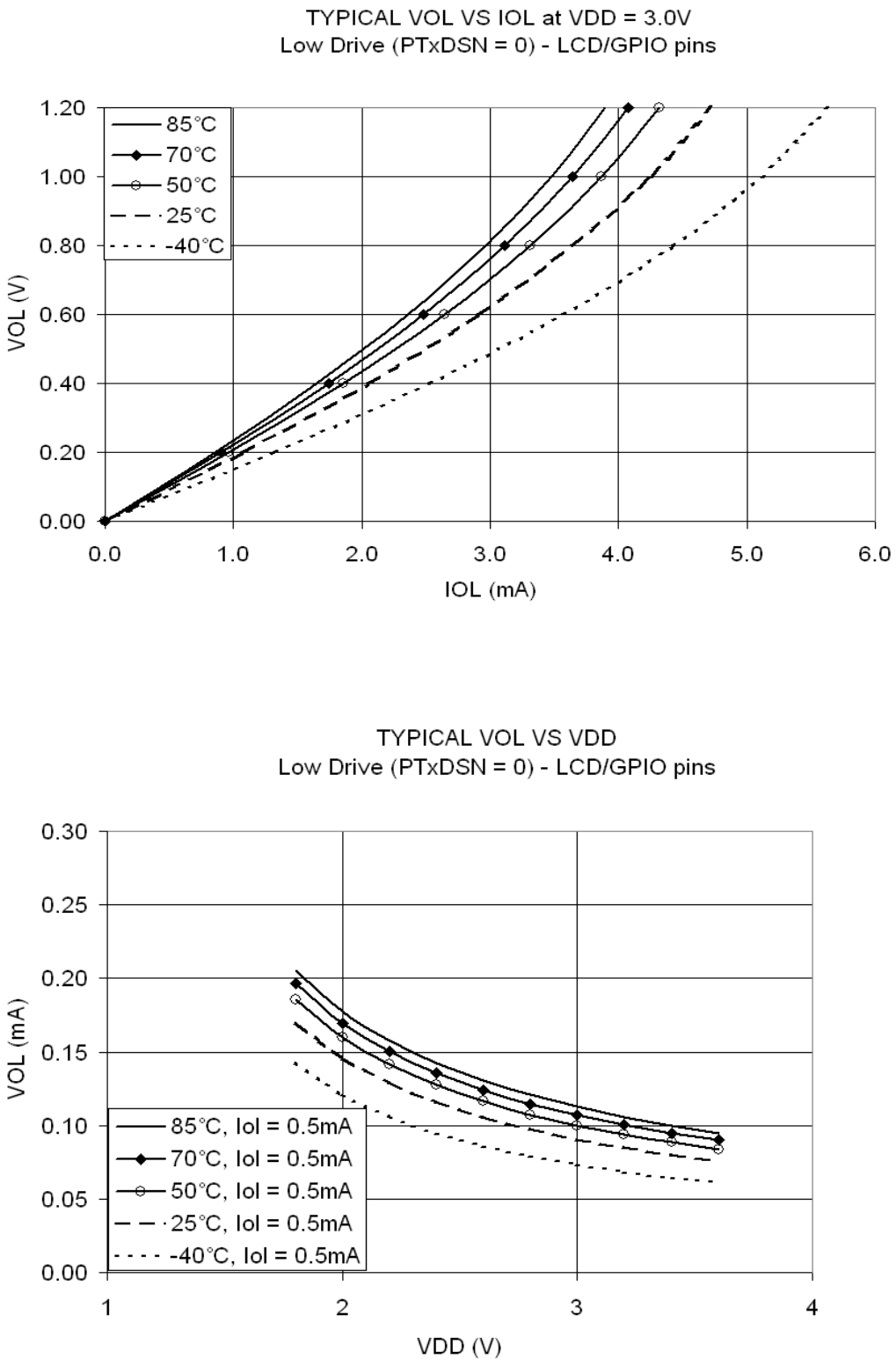
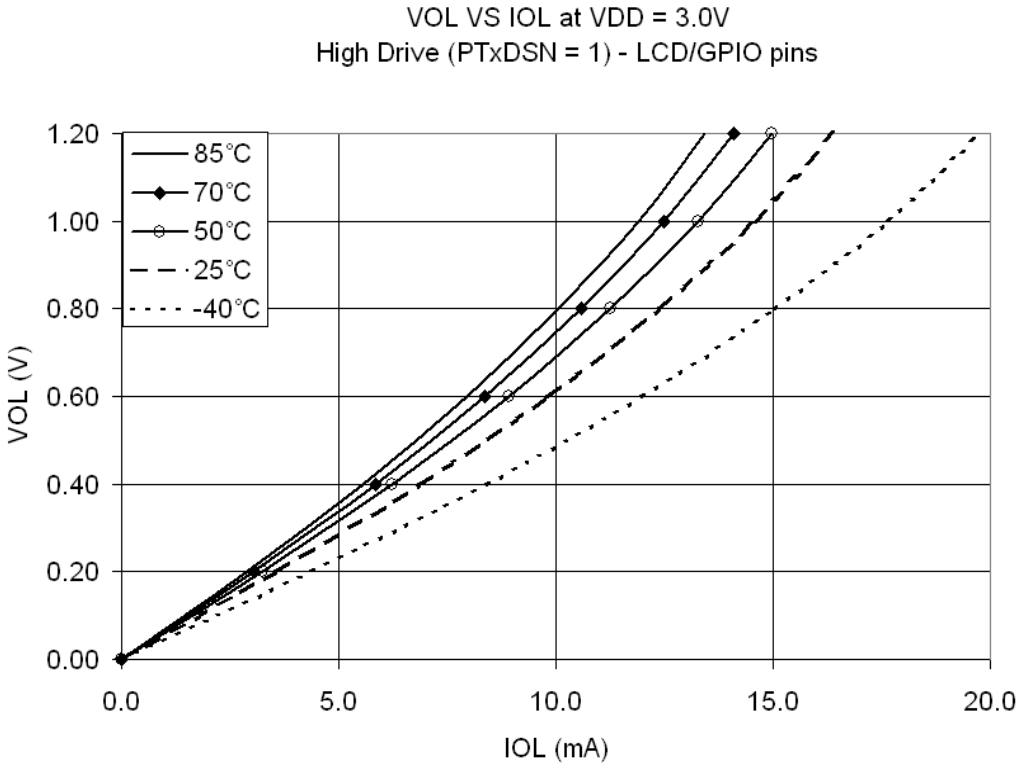


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)



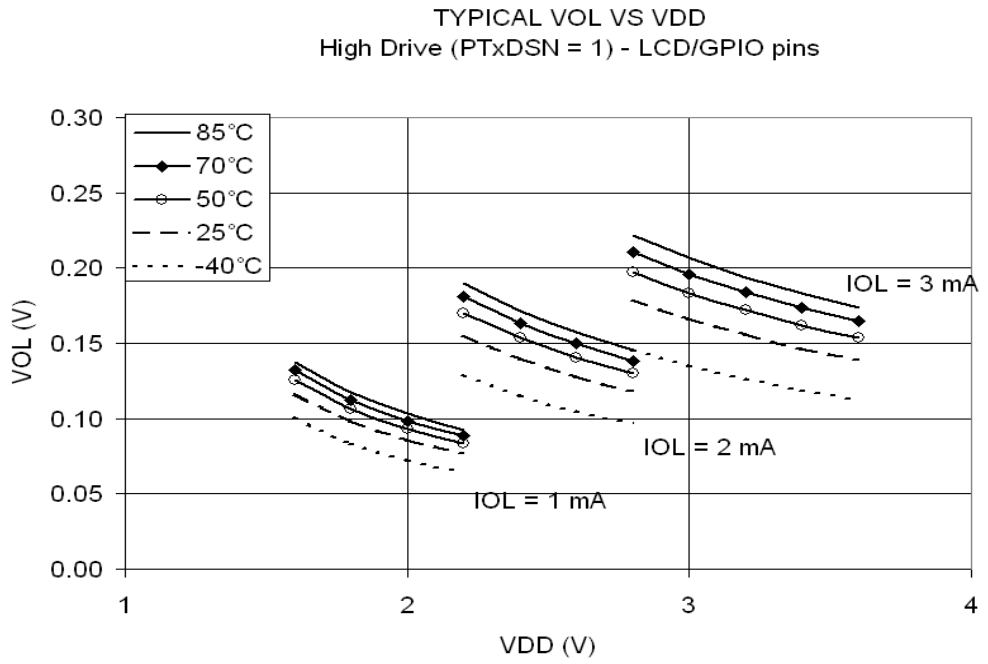


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO Pins) — High Drive (PTxDSn = 1)

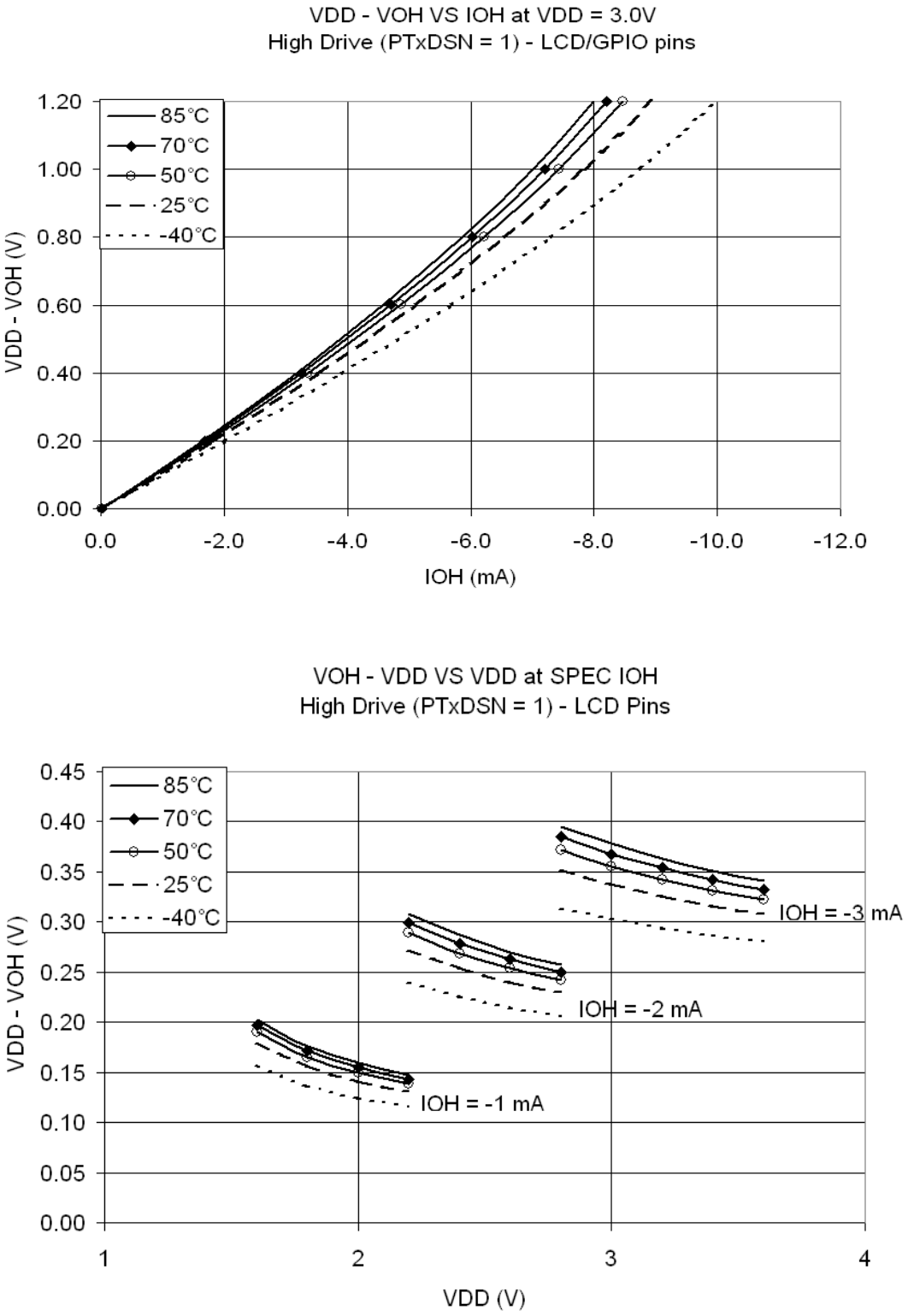


Figure 13. Typical High-Side (Source) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	8 MHz	3	4.2	5.7	mA	–40 to 85 °C
	T			1 MHz		1	1.52		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85 °C
	T			1 MHz		0.50	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	µA	–40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off; running from Flash	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		21	—		
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	P	Wait mode supply current FEI mode, all modules off	WI_{DD}	8 MHz	3	1.4	3.5	mA	–40 to 85 °C
	C			1 MHz		0.8	1.15		
7	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBELP	3	1.3	—	µA	–40 to 85 °C
8	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	350	930	nA	–40 to 25 °C
						1000	—		50 °C
						2500	4000		70 °C
						5100	—		85 °C
	C			n/a	2	250	—		–40 to 25 °C
						2000	—		70 °C
						4000	—		85 °C
9	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	400	1030	nA	–40 to 25 °C
						1300	—		50 °C
						4000	6000		70 °C
						8000	—		85 °C
	C			n/a	2	350	—		–40 to 25 °C
						3000	—		70 °C
						6000	—		85 °C

3.8 External Oscillator (XOSCVLP) Characteristics

Refer to Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

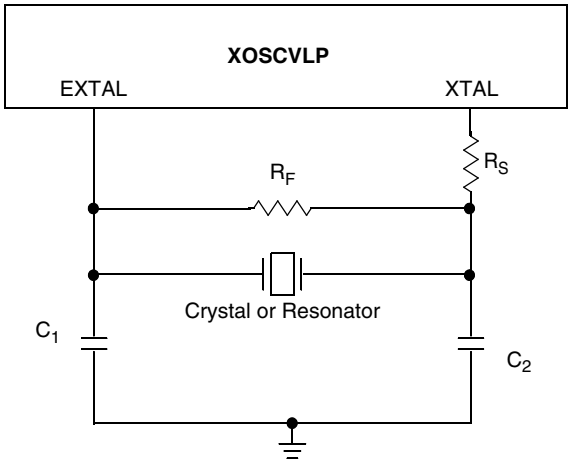


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

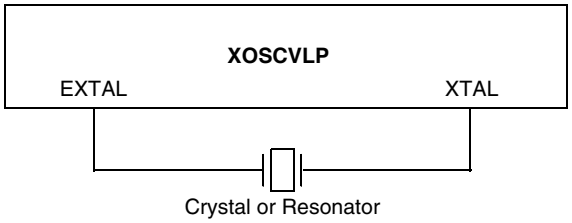


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	µs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 –1.0	±2	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

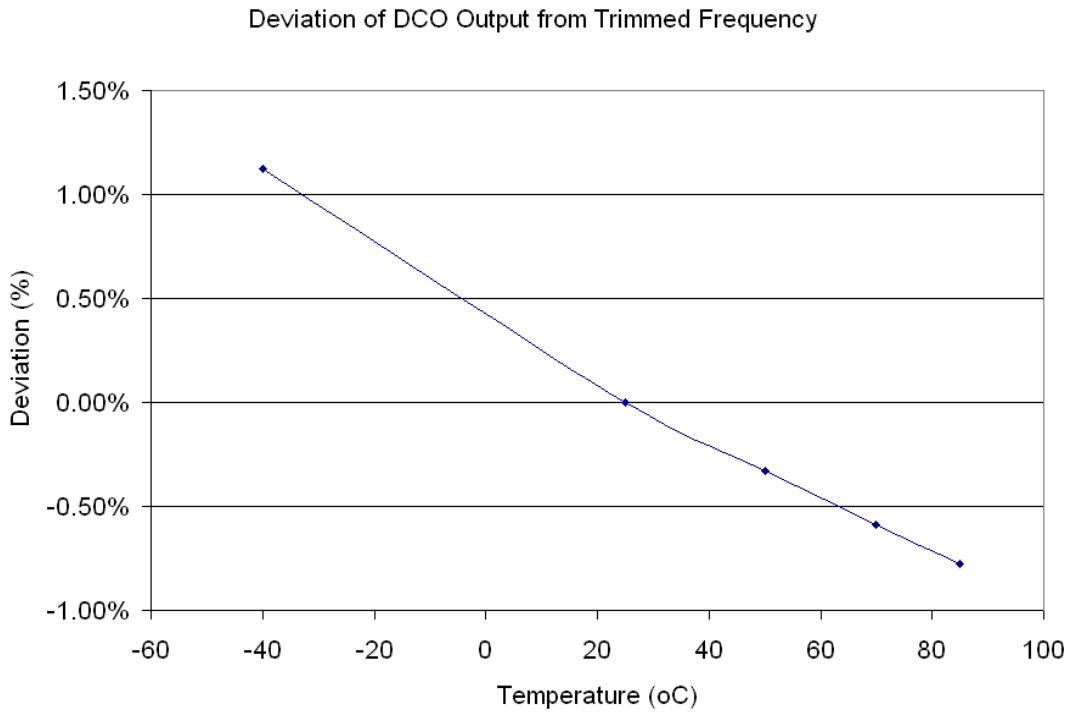


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

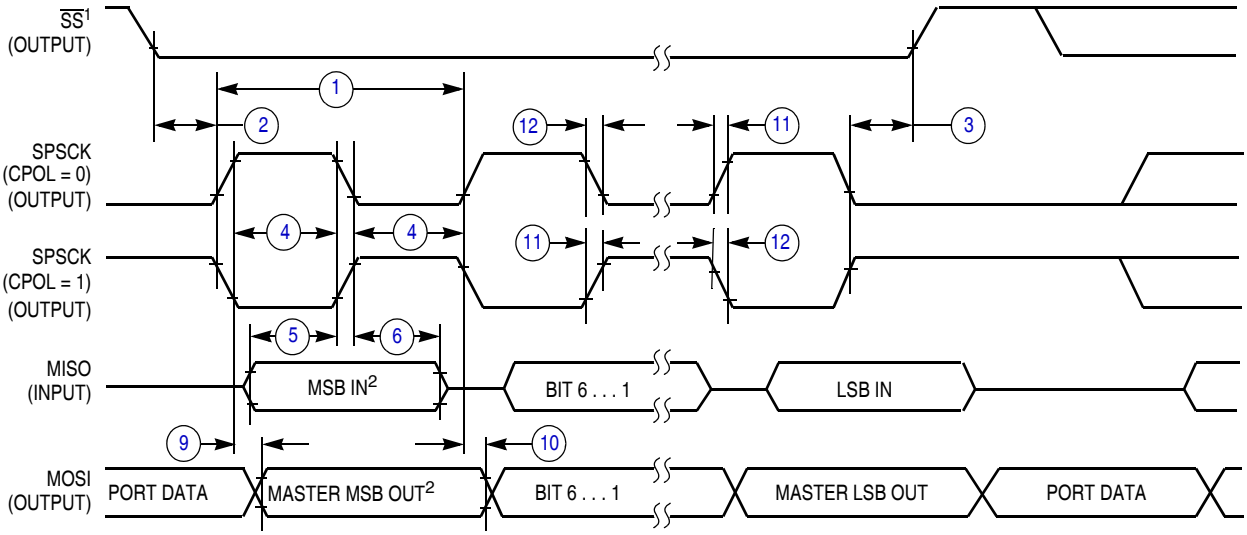
2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

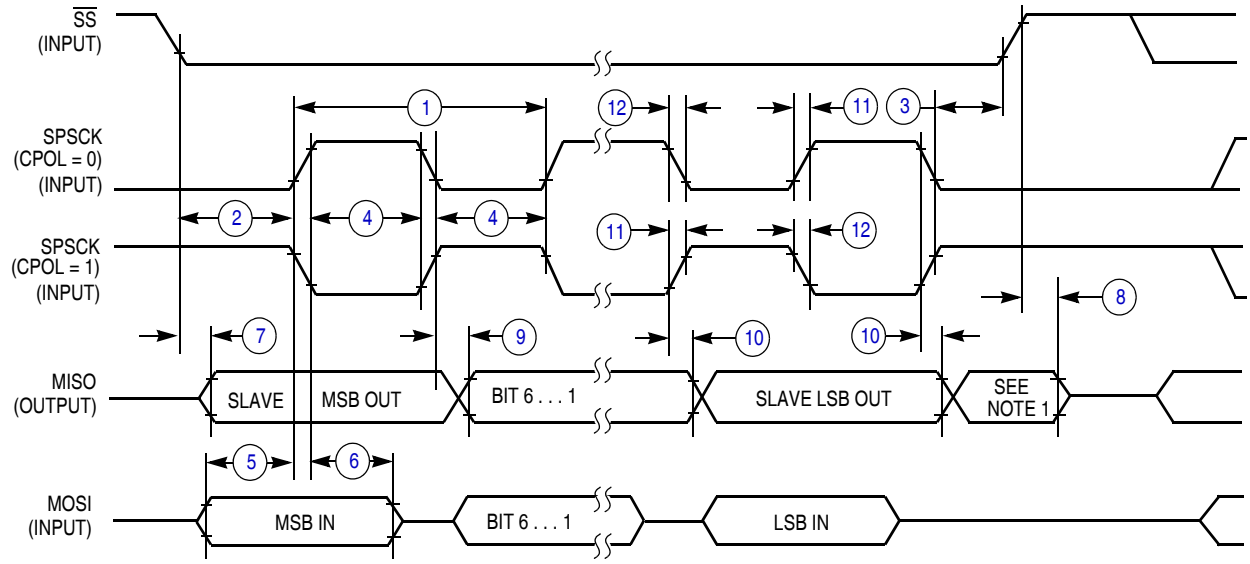
5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

6 Except for LCD pins in Open Drain mode.



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 22. SPI Master Timing (CPHA =1)



NOTE:
1. Not defined but normally MSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 0)

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	120	—	μA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	200	—	μA	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	290	—	μA	
P	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.53	1	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
C		Low Power (ADLPC=1)		1.25	2	3.3		
P	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the LL16 Reference Manual for conversion time variances
C		Long Sample (ADLSMP=1)		—	40	—		
P	Sample Time	Short Sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
C		Long Sample (ADLSMP=1)		—	23.5	—		
T	Total Unadjusted Error	12-bit mode, 3.6>VDDA>2.7V	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
		12-bit mode, 2.7>VDDA>1.8V		—	–1 to 3	–3.0 to 6.0		
P		10-bit mode		—	±1	±2.5		
T		8-bit mode		—	±0.5	±1.0		
T	Differential Non-Linearity	12-bit mode	DNL	—	±1	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
T		8-bit mode[3]		—	±0.3	±0.5		
T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	–2.5 to 1.0	LSB[2]	
P		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		

3.13 LCD Specifications

Table 19. LCD Electricals, 3 V Glass

C	Characteristic		Symbol	Min	Typ	Max	Unit
D	LCD Supply Voltage		V_{LCD}	0.9	1.5	1.8	V
D	LCD Frame Frequency		f_{Frame}	28	30	58	Hz
D	LCD Charge Pump Capacitance		C_{LCD}		100	100	nF
D	LCD Bypass Capacitance		C_{BYLCD}		100	100	nF
D	LCD Glass Capacitance		C_{glass}		2000	8000	pF
D	V_{IREG}	HRefSel = 0 HRefSel = 1	V_{IREG}	.89 1.49	1.00 1.67	1.15 1.85[1]	V
D	V_{IREG} TRIM Resolution		Δ_{RTRIM}	1.5			% V_{IREG}
D	V_{IREG} Ripple	HRefSel = 0 HRefSel = 1				0.1 0.15	V
D	V_{LCD} Buffered Adder[2]		I_{Buff}		1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V

2 VSUPPLY = 10, BYPASS = 0

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 21. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 3.3 V T_A = 25 °C package type 64-pin LQFP	0.15 – 50 MHz	32 kHz crystal 10 MHz bus	–7	dBμV
			50 – 150 MHz		–9	
			150 – 500 MHz		–6	
			500 – 1000 MHz		–6	
			IEC Level		N	—
			SAE Level		1	—

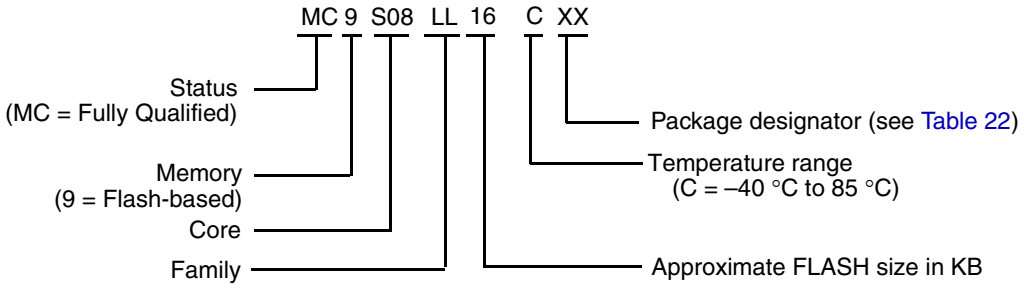
1 Data based on qualification test results.

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08LL16 Series.

4.1 Device Numbering System

Example of the device numbering system:



5 Package Information and Mechanical Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LL16 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.