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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08ll16clhr

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

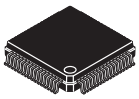
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LL16
Rev. 7, 1/2013

An Energy Efficient Solution by Freescale

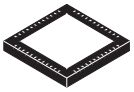
MC9S08LL16 Series

Covers: MC9S08LL16 and MC9S08LL8



64-LQFP
Case 840F

48-LQFP
Case 932



48-QFN
1314

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20-MHz CPU at 3.6V to 1.8V across temperature range of -40°C to 85°C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual Array FLASH read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and FLASH contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents.
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6 usec typical wake up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1MHz to 10 MHz.
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-Voltage Warning with interrupt
  - Low-Voltage Detection with reset or interrupt
  - Illegal opcode and illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — 4x28 or 8x24 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control.
  - **ADC** — 8-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
  - **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
  - **SPI**— Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
  - **IIC** — IIC with up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
  - **TPMx** — Two 2-channel (TPM1 and TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
  - **TOD**— (Time Of Day) 8-bit quarter second counter with match register; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components.
- Input/Output
  - 38 GPIOs, 2 output-only pins
  - 8 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.
- Package Options
  - 64-LQFP, 48-LQFP and 48-QFN

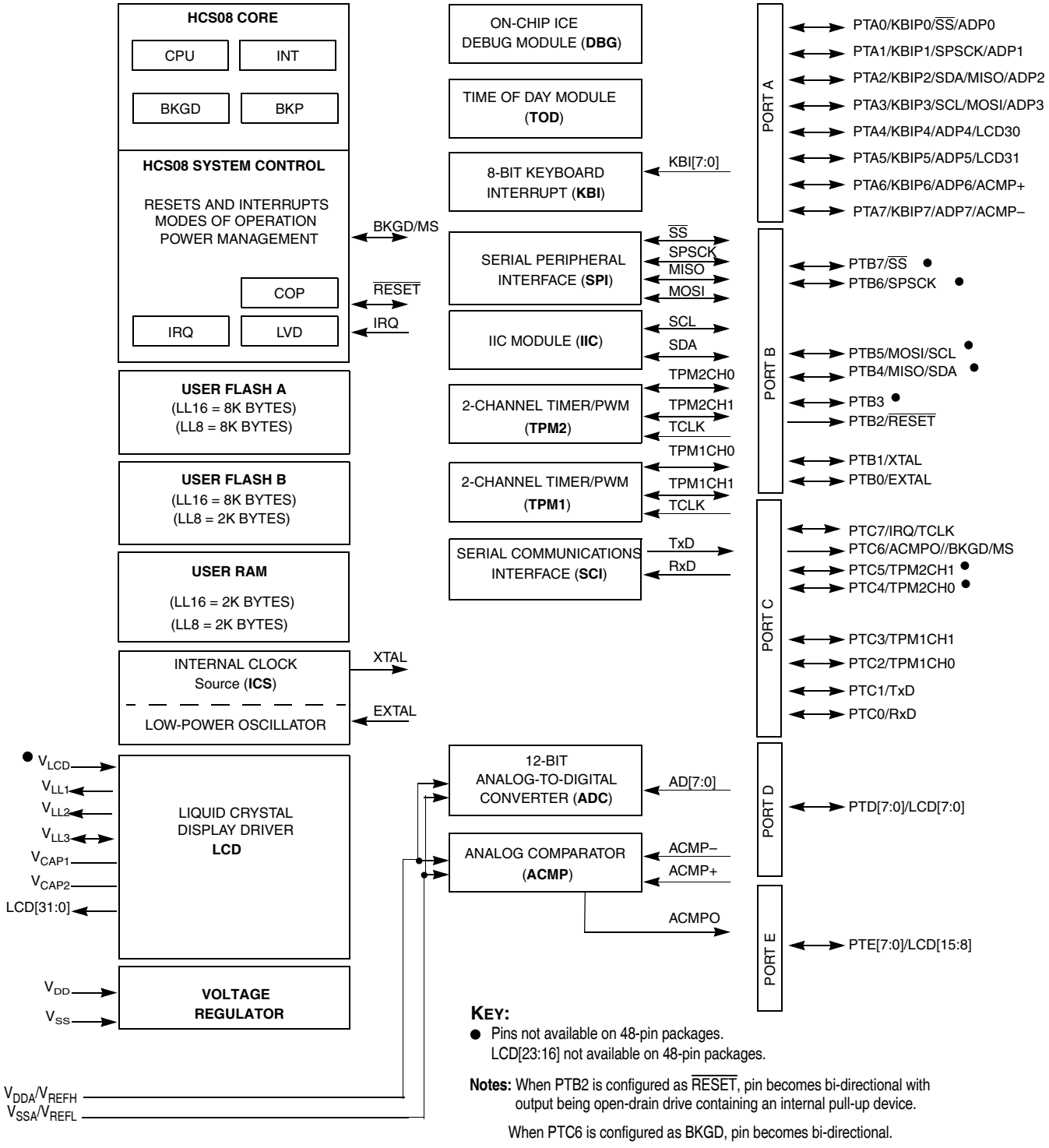
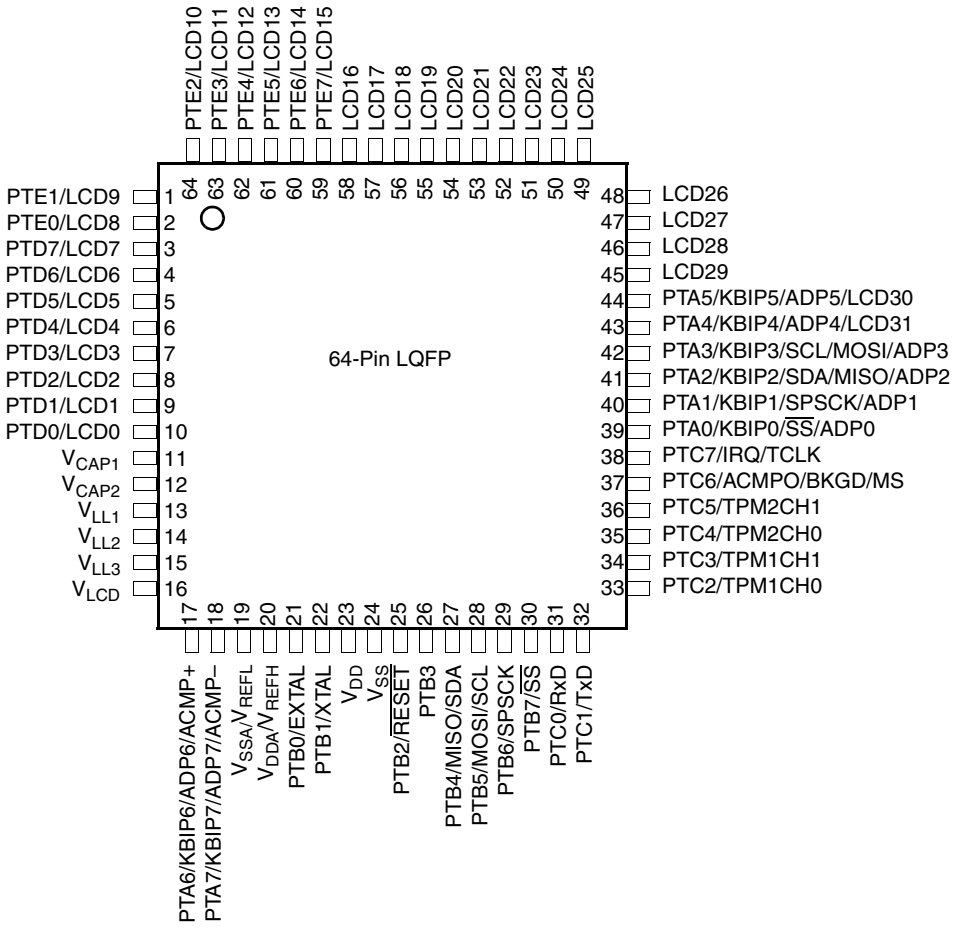


Figure 1. MC9S08LL16 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08LL16 series devices.



Note: V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Figure 2. MC9S08LL16 Series in 64-pin LQFP Package

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest **Priority** --> Highest				
64	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt3**	**Alt4**
1	47	PTE1	LCD9			
2	48	PTE0	LCD8			
3	1	PTD7	LCD7			
4	2	PTD6	LCD6			
5	3	PTD5	LCD5			
6	4	PTD4	LCD4			
7	5	PTD3	LCD3			
8	6	PTD2	LCD2			
9	7	PTD1	LCD1			
10	8	PTD0	LCD0			
11	9		V_{cap1}			
12	10		V_{cap2}			
13	11		V_{LL1}			
14	12		V_{LL2}			
15	13		V_{LL3}			
16	—		V_{LCD}			
17	14	PTA6	KBIP6	ADP6	ACMP+	
18	15	PTA7	KBIP7	ADP7	ACMP–	
19	16				V_{SSA}	
					V_{REFL}	
20	17				V_{REFH}	
					V_{DDA}	
21	18	PTB0		EXTAL		
22	19	PTB1		XTAL		
23	20				V_{DD}	
24	21				V_{SS}	
25	22	PTB2	$\overline{\text{RESET}}$			
26	—	PTB3				
27	—	PTB4	—	MISO	SDA	
28	—	PTB5	—	MOSI	SCL	
29	—	PTB6	—	SPSCK		
30	—	PTB7	—	$\overline{\text{SS}}$		
31	23	PTC0		RxD		
32	24	PTC1		TxD		
33	25	PTC2		TPM1CH0		
34	26	PTC3		TPM1CH1		
35	—	PTC4		TPM2CH0		
36	—	PTC5		TPM2CH1		
37	27	PTC6	ACMPO	BKGD	MS	
38	28	PTC7		IRQ	TCLK	
39	29	PTA0	KBIP0	—	$\overline{\text{SS}}$	ADP0

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
11	P	Input leakage current	all input only pins except for LCD only pins (LCD 16-29)	$\|I_{In}\|$	$V_{In} = V_{DD}$	—	0.025	1	μA
					$V_{In} = V_{SS}$	—	0.025	1	μA
			LCD only pins (LCD 16-29)		$V_{In} = V_{DD}$	—	100	150	μA
					$V_{In} = V_{SS}$	—	0.025	1	μA
12	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	0.025	1	μA
13	P	Total leakage current[3]	Total leakage current for all pins	$\|I_{InT}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
14	P	Pullup, pulldown resistors when enabled	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7]	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
	P		PTA[4:5], PTD[0:7], PTE[0:7]					69.5	
15	D	DC injection current [4, 5, 6]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
16	C	Input capacitance, all pins		C_{In}		—	—	8	pF
17	C	RAM retention voltage		V_{RAM}		—	0.6	1.0	V
18	C	POR re-arm voltage[7]		V_{POR}		0.9	1.4	2.0	V
19	D	POR re-arm time		t_{POR}		10	—	—	μs
20	P	Low-voltage detection threshold		V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V
21	P	Low-voltage warning threshold		V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.2	V
22	P	Low-voltage inhibit reset/recover hysteresis		V_{hys}		—	80	—	mV
23	P	Bandgap voltage reference[8]		V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 All I/O pins except for LCD pins in open drain mode.

3 Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

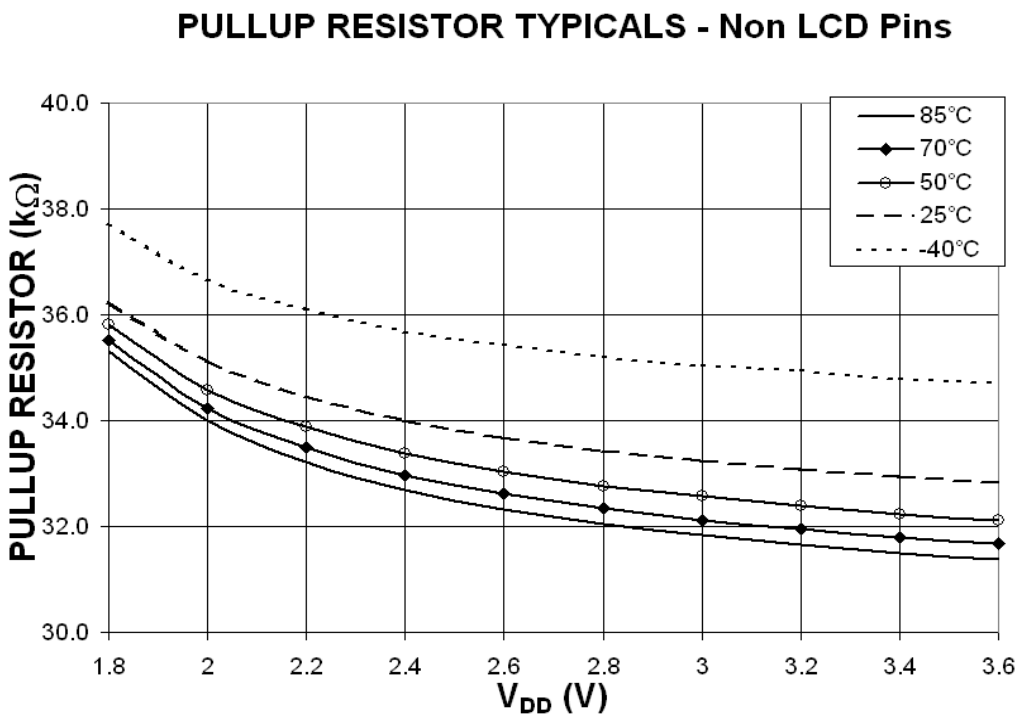
4 All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 POR will occur below the minimum voltage.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C.



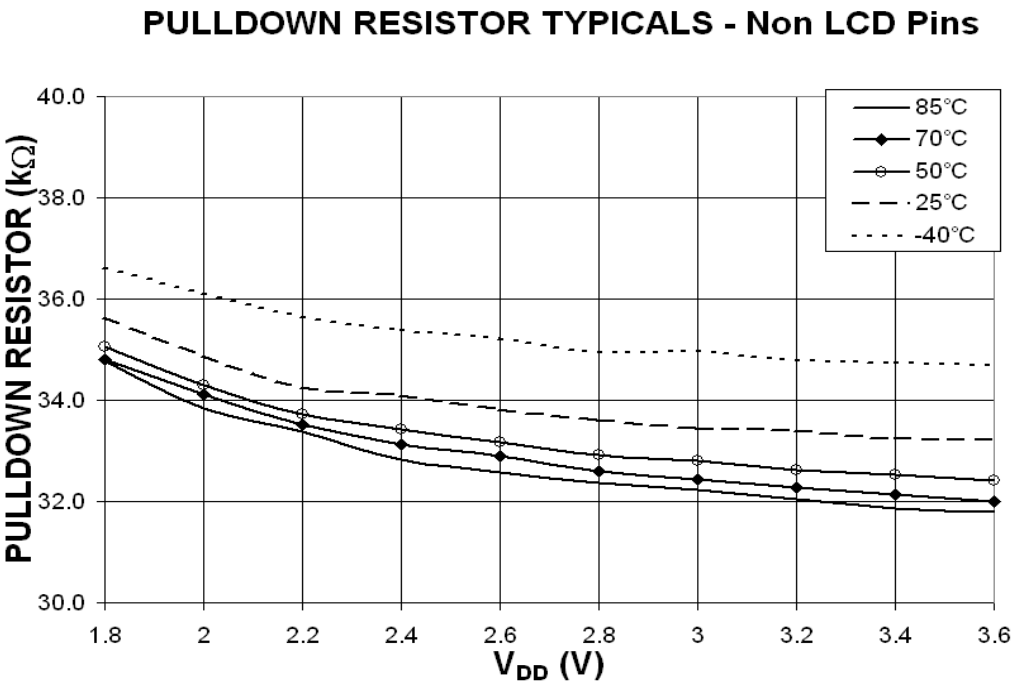


Figure 4. Non-LCD pins I/O Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

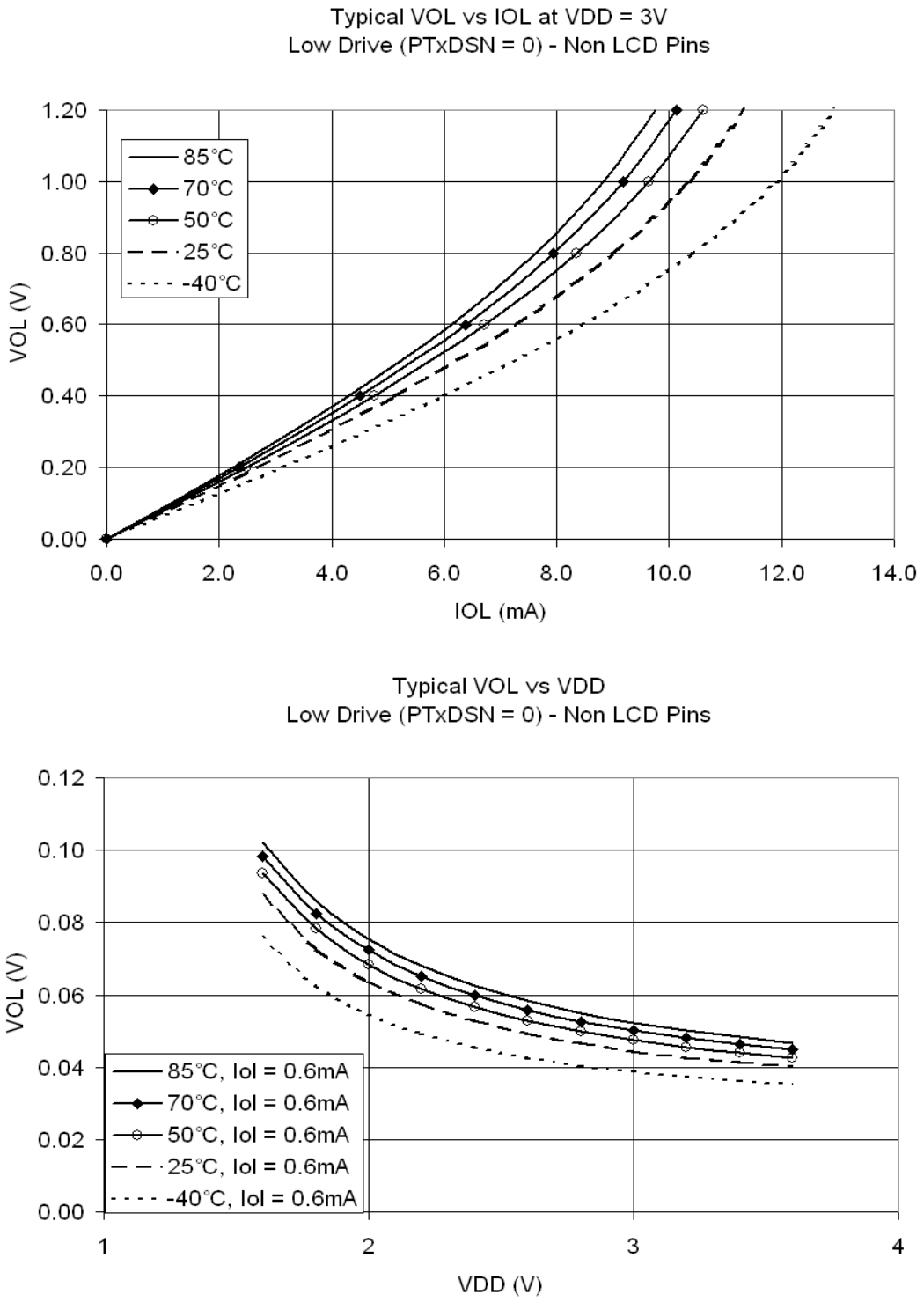
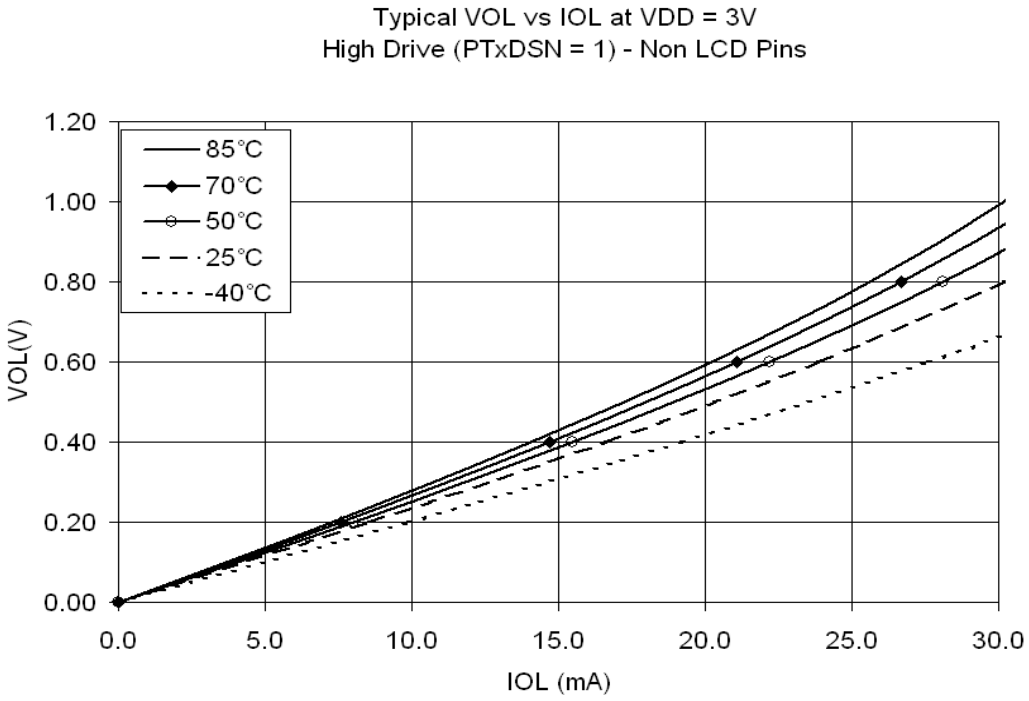


Figure 6. Typical Low-Side Driver (Sink) Characteristics (Non-LCD pins) — Low Drive (PTxDSn = 0)



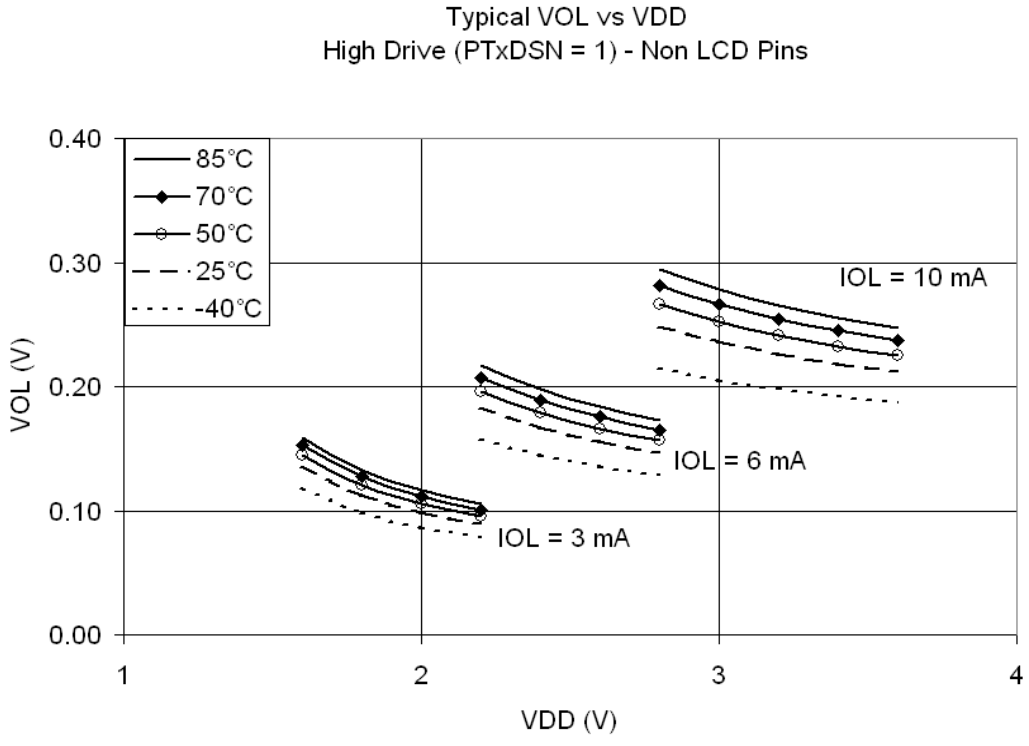


Figure 7. Typical Low-Side Driver (Sink) Characteristics(Non-LCD pins) — High Drive (PTxDSn = 1)

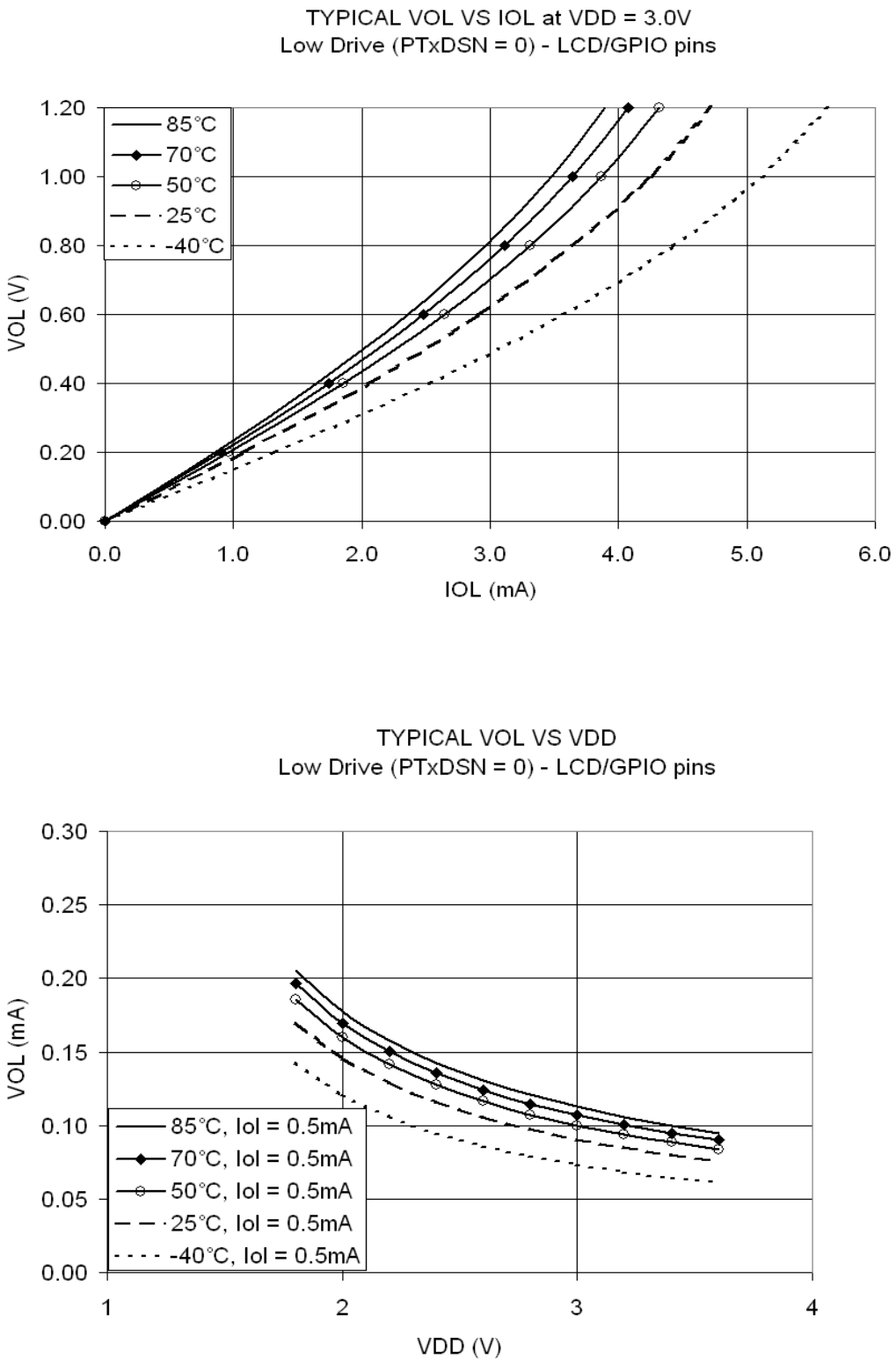
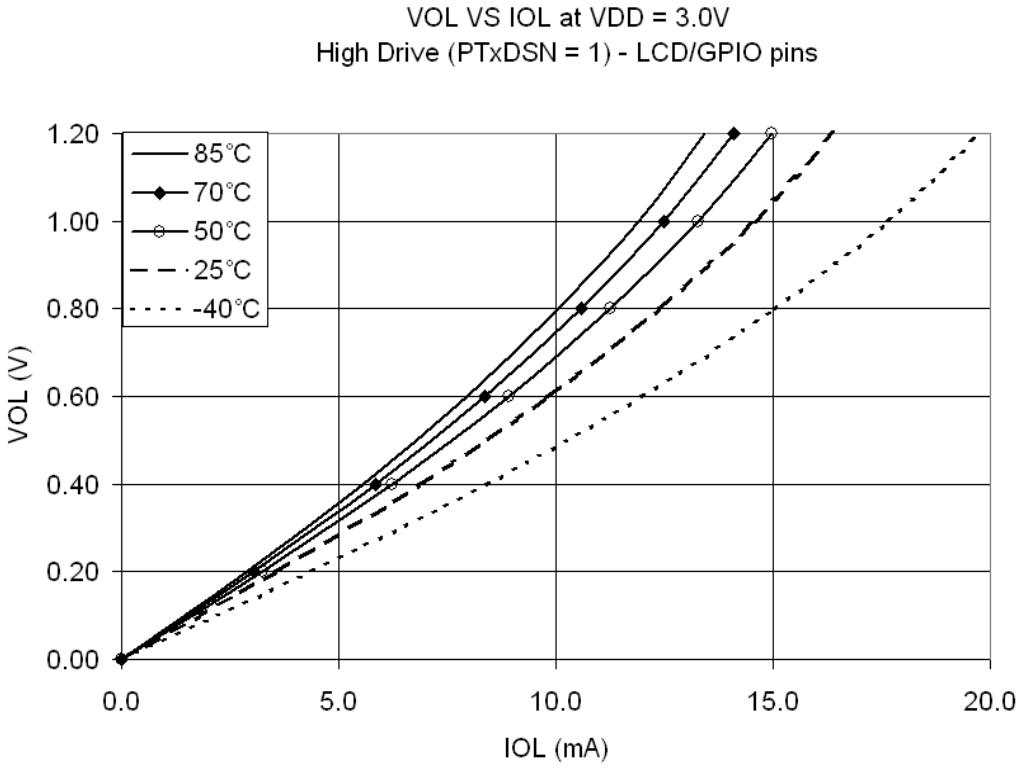


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)



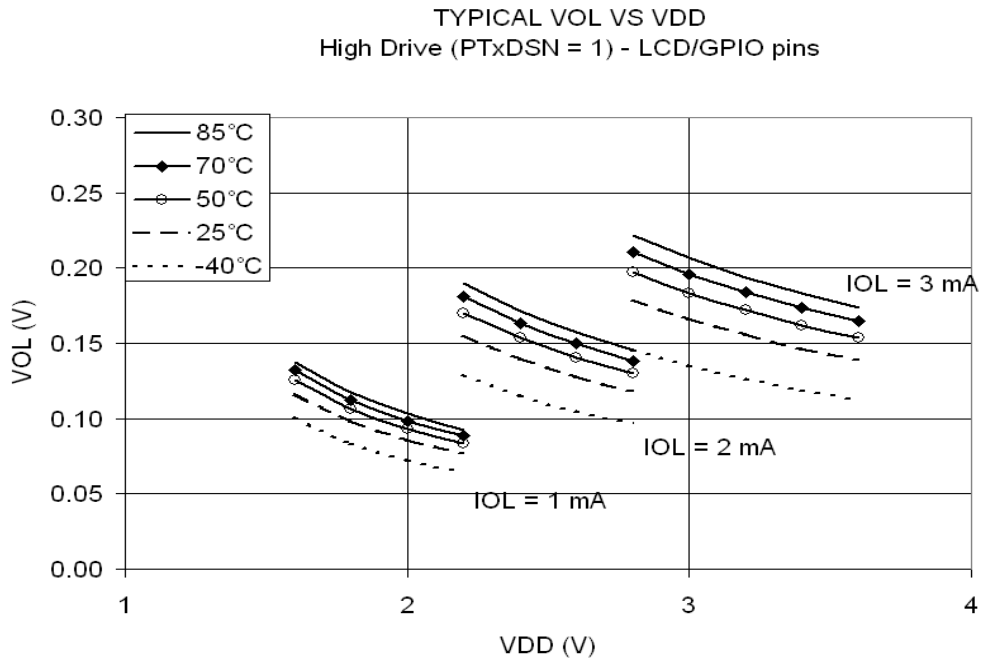
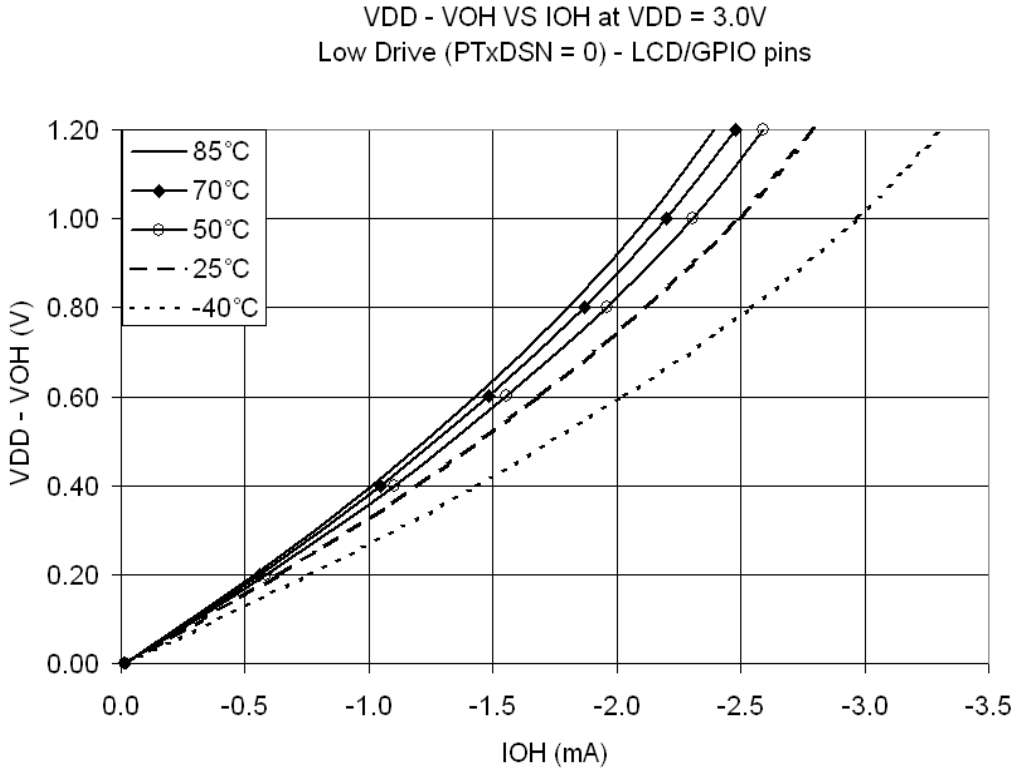


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO Pins) — High Drive (PTxDSn = 1)



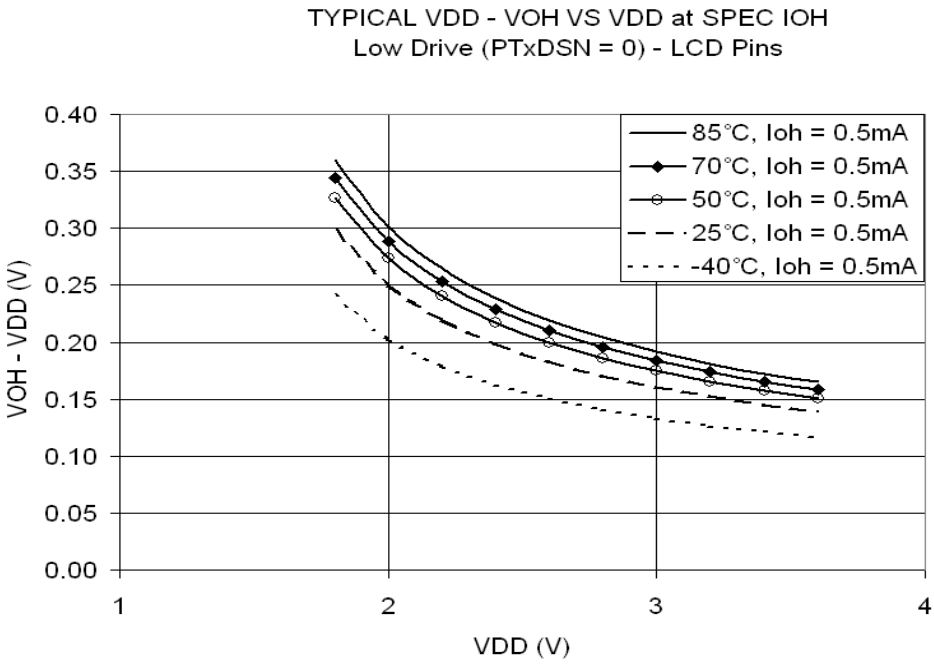


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	8 MHz	3	4.2	5.7	mA	–40 to 85 °C
	T			1 MHz		1	1.52		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85 °C
	T			1 MHz		0.50	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	µA	–40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off; running from Flash	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		21	—		
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	P	Wait mode supply current FEI mode, all modules off	WI_{DD}	8 MHz	3	1.4	3.5	mA	–40 to 85 °C
	C			1 MHz		0.8	1.15		
7	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBELP	3	1.3	—	µA	–40 to 85 °C
8	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	350	930	nA	–40 to 25 °C
						1000	—		50 °C
						2500	4000		70 °C
						5100	—		85 °C
	C			n/a	2	250	—		–40 to 25 °C
						2000	—		70 °C
						4000	—		85 °C
9	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	400	1030	nA	–40 to 25 °C
						1300	—		50 °C
						4000	6000		70 °C
						8000	—		85 °C
	C			n/a	2	350	—		–40 to 25 °C
						3000	—		70 °C
						6000	—		85 °C

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

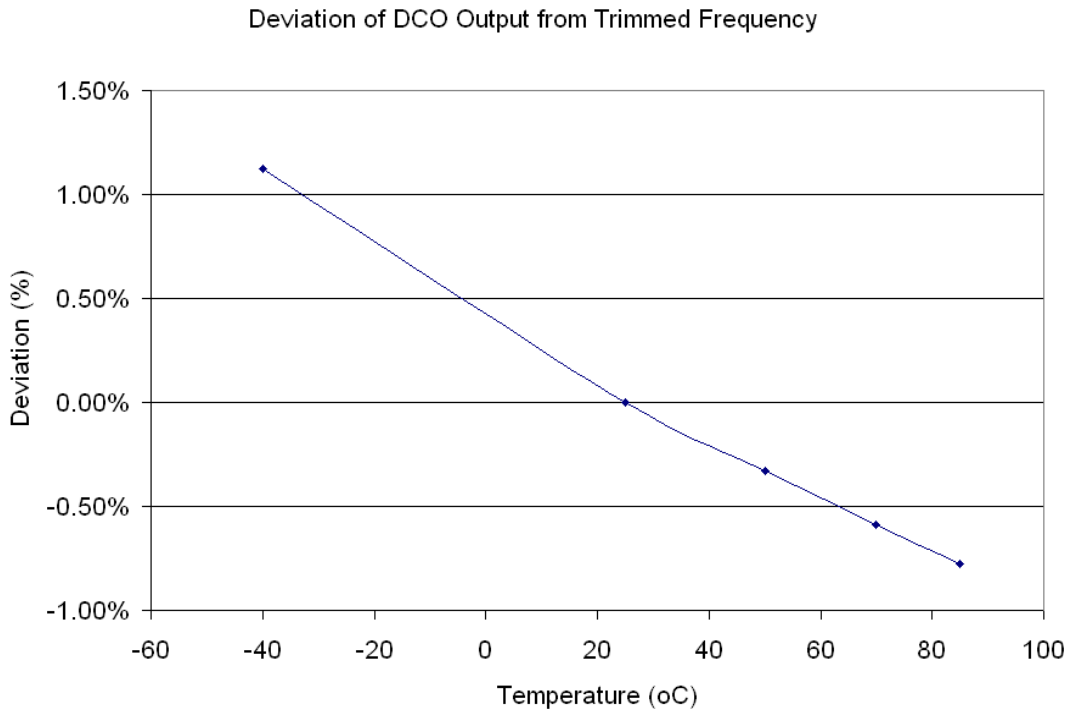


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

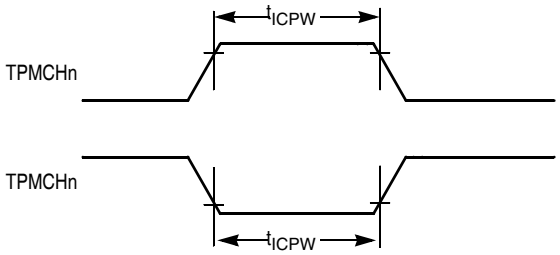


Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

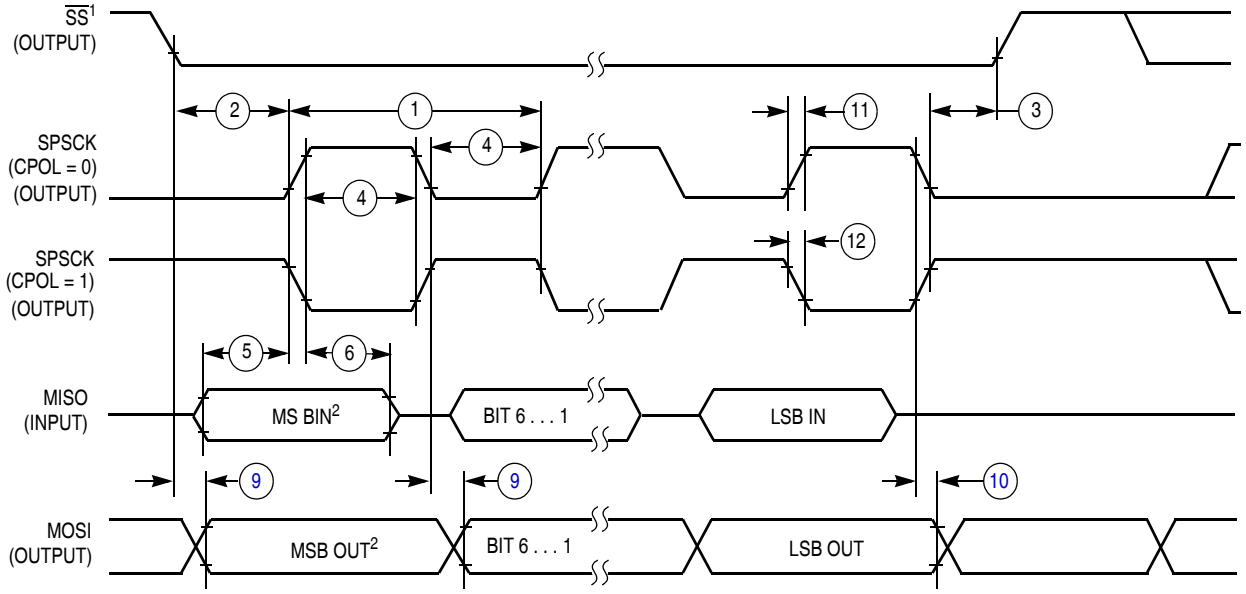
Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns

Table 15. SPI Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 t_{cyc} – 25 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 t_{cyc} – 25 25	 ns ns



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	120	—	μA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	200	—	μA	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	290	—	μA	
P	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.53	1	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
C		Low Power (ADLPC=1)		1.25	2	3.3		
P	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the LL16 Reference Manual for conversion time variances
C		Long Sample (ADLSMP=1)		—	40	—		
P	Sample Time	Short Sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
C		Long Sample (ADLSMP=1)		—	23.5	—		
T	Total Unadjusted Error	12-bit mode, 3.6>VDDA>2.7V	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
		12-bit mode, 2.7>VDDA>1.8V		—	–1 to 3	–3.0 to 6.0		
P		10-bit mode		—	±1	±2.5		
T		8-bit mode		—	±0.5	±1.0		
T	Differential Non-Linearity	12-bit mode	DNL	—	±1	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
T		8-bit mode[3]		—	±0.3	±0.5		
T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	–2.5 to 1.0	LSB[2]	
P		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		

3.13 LCD Specifications

Table 19. LCD Electricals, 3 V Glass

C	Characteristic		Symbol	Min	Typ	Max	Unit
D	LCD Supply Voltage		V_{LCD}	0.9	1.5	1.8	V
D	LCD Frame Frequency		f_{Frame}	28	30	58	Hz
D	LCD Charge Pump Capacitance		C_{LCD}		100	100	nF
D	LCD Bypass Capacitance		C_{BYLCD}		100	100	nF
D	LCD Glass Capacitance		C_{glass}		2000	8000	pF
D	V_{IREG}	HRefSel = 0 HRefSel = 1	V_{IREG}	.89 1.49	1.00 1.67	1.15 1.85[1]	V
D	V_{IREG} TRIM Resolution		Δ_{RTRIM}	1.5			% V_{IREG}
D	V_{IREG} Ripple	HRefSel = 0 HRefSel = 1				0.1 0.15	V
D	V_{LCD} Buffered Adder[2]		I_{Buff}		1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V

2 VSUPPLY = 10, BYPASS = 0

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

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