Infineon Technologies - MB96F613ABPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f613abpmc-gse1

Contents

1. Product Lineup

Features		CY96610	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
32.5KB + 32KB	4KB	CY96F612R, CY96F612A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB	10KB	CY96F613R, CY96F613A	
128.5KB + 32KB	10KB	CY96F615R, CY96F615A	
Package		LQFP-48 LQA048	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO	No	
8/10-bit A/D Converter		16ch	AN 0/1/3/4/6 to 10/ 12/14/16/24/25/30/31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	No	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 0 to 3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		7ch (3 channels for LIN-USART)	ICU 0/1/4 to 6/9/10 (ICU 6/9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)		5ch	OCU 0/1/4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INT)		11ch	INT 0/2/3/4/7 to 13
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		35 (Dual clock mode) 37 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

5. Pin Circuit Type

Pin No.	I/O Circuit Type*	Pin Name
1	Supply	AVss
2	G	AVRH
3	K	P06_3 / AN3 / PPG3
4	K	P06_4 / AN4 / PPG4
5	K	P06_6 / AN6 / PPG6
6	K	P06_7 / AN7 / PPG7
7	I	P05_0 / AN8 / SIN2 / INT3_R1
8	K	P05_1 / AN9 / SOT2
9	I	P05_2 / AN10 / SCK2
10	K	P05_4 / AN12 / TOT3 / INT2_R
11	K	P05_6 / AN14 / INT4_R
12	K	P07_0 / AN16 / INT0 / NMI
13	B	P04_0 / X0A
14	B	P04_1 / X1A
15	C	MD
16	H	P17_0
17	O	DEBUG I/F
18	M	P00_0 / INT8 / SCK7_R / PPG0_B
19	H	P00_1 / INT9 / SOT7_R / PPG1_B
20	M	P00_2 / INT10 / SIN7_R
21	H	P00_4 / INT12 / SOT8_R / PPG12_B
22	M	P00_5 / INT13 / SIN8_R / PPG14_B
23	M	P00_3 / INT11 / SCK8_R / PPG3_B
24	H	P01_0 / TIN1 / CKOT1 / OUT0_R
25	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
26	H	P01_4 / PPG4_B
27	M	P01_5 / SIN2_R / INT7_R
28	H	P01_6 / SOT2_R / PPG6_B
29	M	P01_7 / SCK2_R / PPG7_B
30	H	P02_0 / PPG12 / CKOT1_R
31	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
32	H	P02_4 / AIN0 / IN0 / TTG0

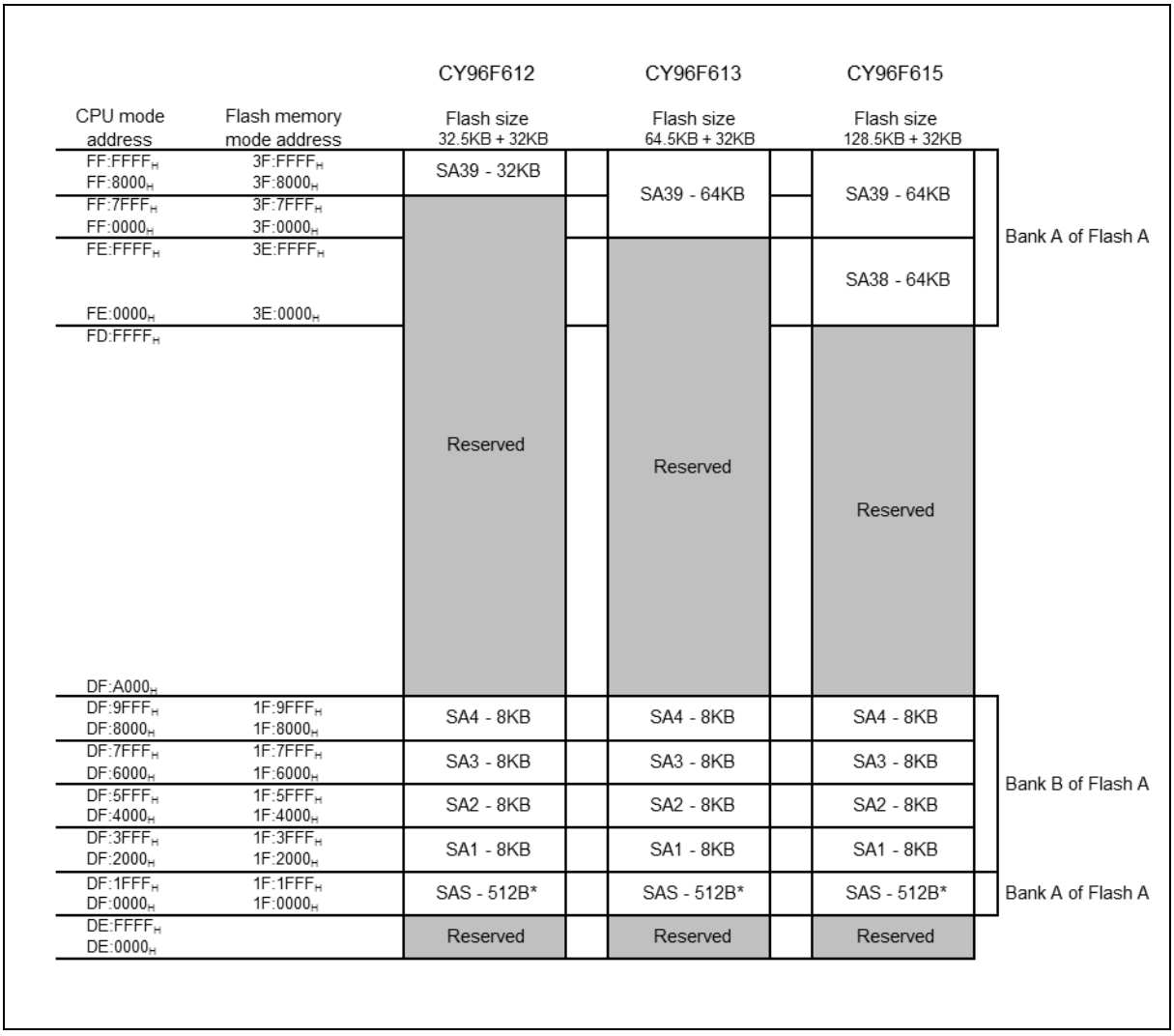
Pin No.	I/O Circuit Type*	Pin Name
33	C	RSTX
34	A	X1
35	A	X0
36	Supply	Vss
37	Supply	Vcc
38	F	C
39	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
40	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
41	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
42	M	P03_2 / INT10_R / RX2
43	H	P03_3 / TX2
44	K	P03_6 / ZIN1 / OUT6 / AN30
45	K	P03_7 / OUT7 / AN31
46	K	P06_0 / AN0 / PPG0
47	K	P06_1 / AN1 / PPG1
48	Supply	AVcc

*: See I/O Circuit Type" for details on the I/O circuit types.

8. RAMstart Addresses

Devices	Bank 0 RAM Size	RAMSTART0
CY96F612	4KB	$00:7200_H$
CY96F613, CY96F615	10KB	$00:5A00_H$

9. User ROM Memory Map for Flash Devices



*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96610		
Pin Number	**USART Number**	**Normal Function**
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable)

13.8 Pin Handling when Not Using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V_{CC} AV_{SS} = AVRH = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.12 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[1]	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
				-	-	14	mA	T_A = +125°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T_A = +25°C
				-	-	4	mA	T_A = +105°C
				-	-	5	mA	T_A = +125°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
				-	-	4.5	mA	T_A = +125°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T_A = +25°C
				-	-	2.7	mA	T_A = +105°C
				-	-	3.7	mA	T_A = +125°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.5	mA	T_A = +105°C
				-	-	3.5	mA	T_A = +125°C

14.3.2 *Pin Characteristics*

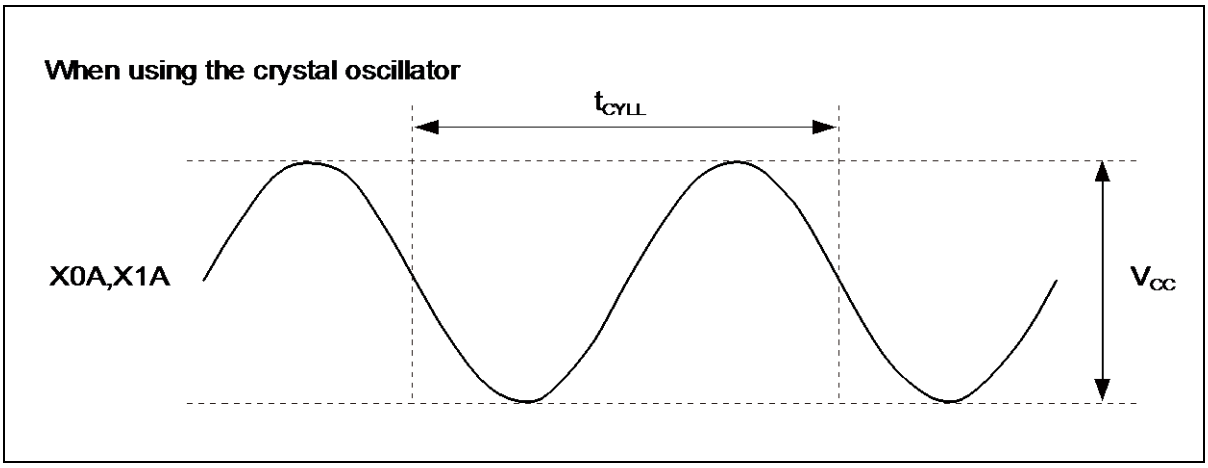
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

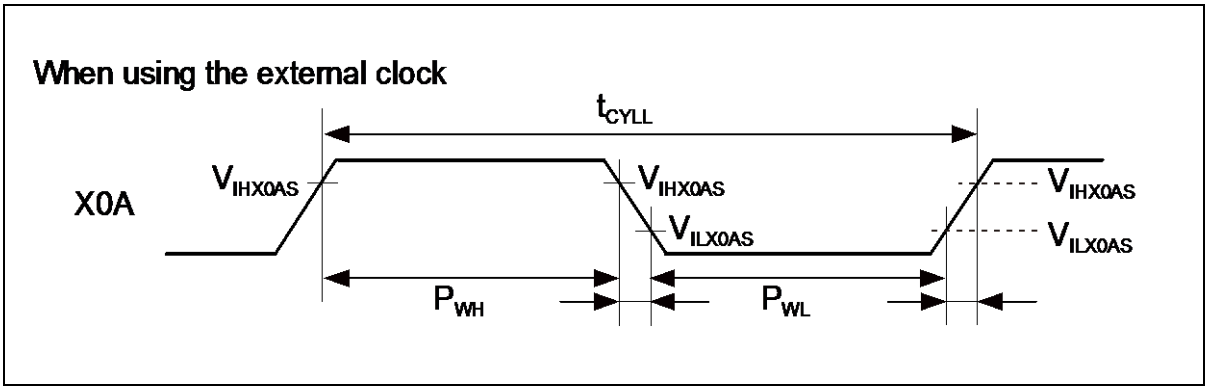
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC}×0.7	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
			-	V_{CC}×0.8	-	V_{CC}+ 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD×0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC}×0.8	-	V_{CC}+ 0.3	V	
	V_{IHR}	RSTX	-	V_{CC}×0.8	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC}- 0.3	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC}+ 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS}- 0.3	-	V_{CC}×0.3	V	CMOS Hysteresis input
			-	V_{SS}- 0.3	-	V_{CC}×0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD×0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS}- 0.3	-	V_{CC}×0.2	V	
	V_{ILR}	RSTX	-	V_{SS}- 0.3	-	V_{CC}×0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS}- 0.3	-	V_{SS}+ 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS}- 0.3	-	0.8	V	TTL Input
"H" level output voltage	V_{OH4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -4mA	V_{CC}- 0.5	-	V_{CC}	V	
			2.7V ≤ V_{CC} < 4.5V I_{OH} = -1.5mA					
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ V_{CC} < 4.5V I_{OL} = +1.7mA					
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS} < V_I <AV_{CC}, AVRH	- 1	-	+ 1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	

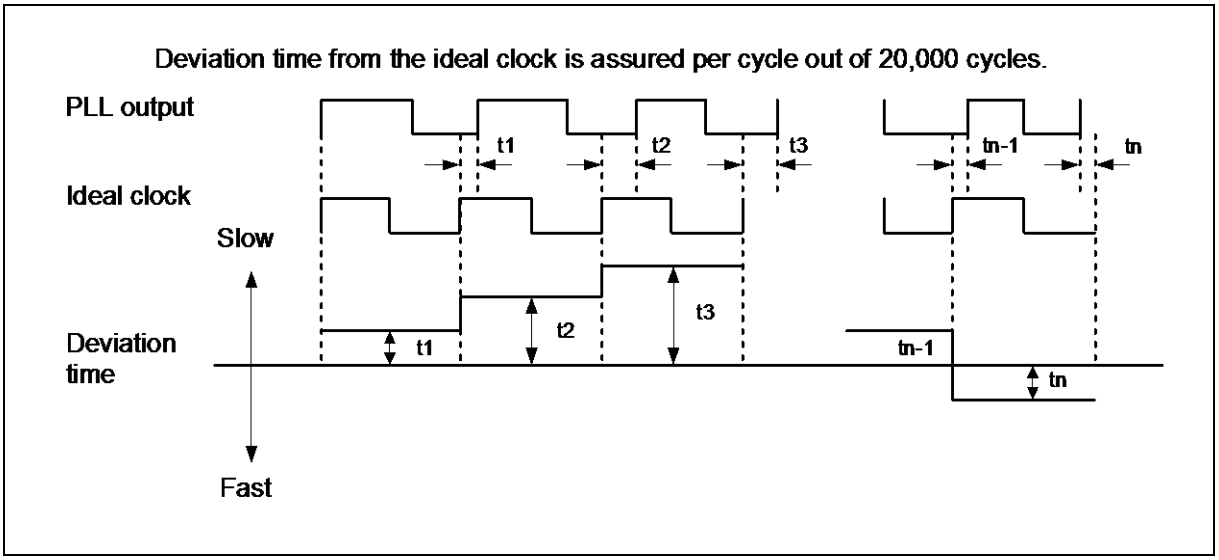




14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

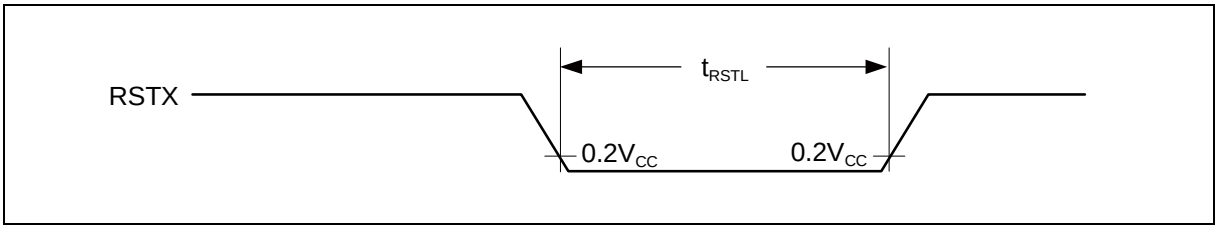
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz

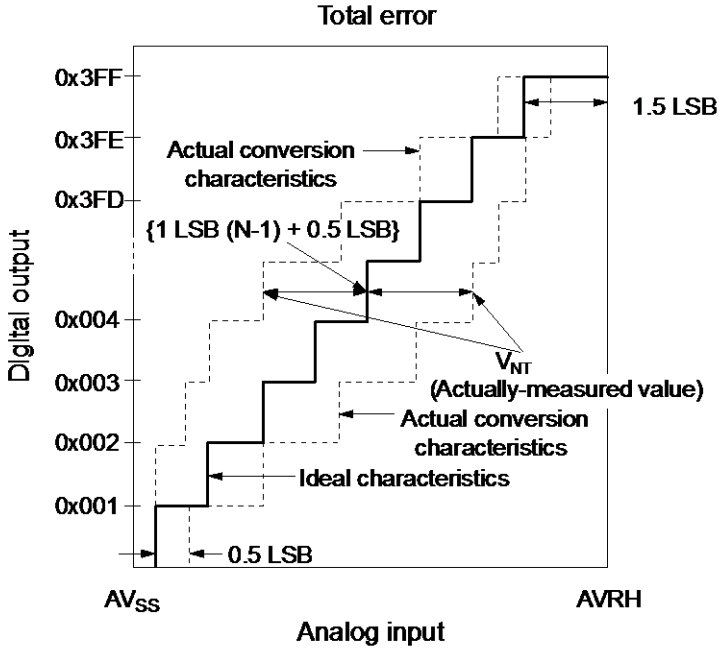


14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs





$$1LSB\ (Ideal\ value) = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT} (Ideal value) = AV_{SS} + 0.5LSB[V]
V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

16. Ordering Information

MCU with CAN Controller

Part Number	Flash Memory	Package*
CY96F612RBPMC-GS-UJE1	Flash A (64.5KB)	48-pin plastic LQFP (LQA048)
CY96F612RBPMC-GS-UJE2		
CY96F613RBPMC-GS-UJE1	Flash A (96.5KB)	48-pin plastic LQFP (LQA048)
CY96F613RBPMC-GS-UJE2		
CY96F613RBPMC-GS-UJERE2		
CY96F615RBPMC-GS-UJE1	Flash A (160.5KB)	48-pin plastic LQFP (LQA048)
CY96F615RBPMC-GS-UJE2		
CY96F615RBPMC-GS-UJERE2		

*: For details about package, see "Package Dimension".

MCU without CAN Controller

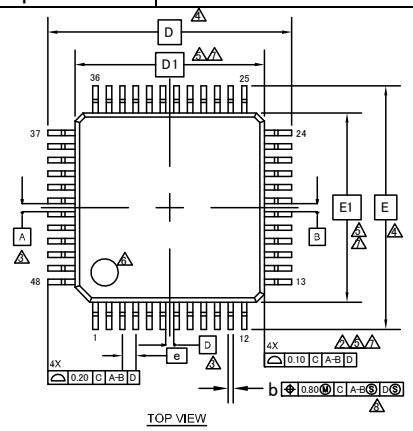
Part Number	Flash Memory	Package*
CY96F612ABPMC-GS-UJE1	Flash A (64.5KB)	48-pin plastic LQFP (LQA048)
CY96F612ABPMC-GS-UJE2		
CY96F613ABPMC-GS-UJE1	Flash A (96.5KB)	48-pin plastic LQFP (LQA048)
CY96F613ABPMC-GS-UJE2		
CY96F615ABPMC-GS-UJE1	Flash A (160.5KB)	48-pin plastic LQFP (LQA048)

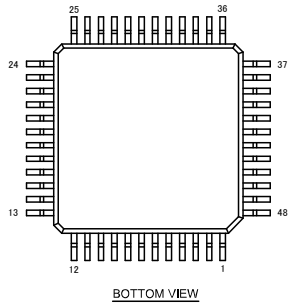
*: For details about package, see "Package Dimension".

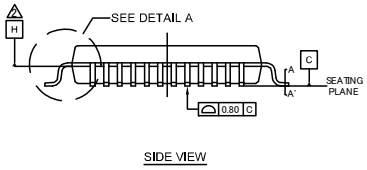
17. Package Dimension

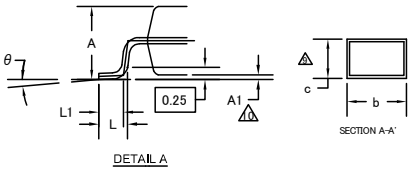
LQA048, 48 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 48pin	LQA048









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

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PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

18. Major Changes

Spansion Publication Number: MB96610_DS704-00007

Page	Section	Change Results
Revision 3.0		
4	■FEATURES	Changed the description of “External Interrupts” Interrupt mask and pending bit per channel Interrupt mask bit per channel
23 to 26	■HANDLING PRECAUTIONS	Added a section
34	■ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,
		Changed the Conditions for I_{CCSRCL} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz CLKS1/2 = CLKP1/2 = CLKRC = 100kHz
35		Changed the Conditions for I_{CCTPLL} PLL Timer mode with CLKP1 = 32MHz PLL Timer mode with CLKPLL = 32MHz
		Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2480µA → 1800µA (T_A = +25°C) Max: 2710µA → 2245µA (T_A = +25°C) Max: 3985µA → 3165µA (T_A = +105°C) Max: 4830µA → 3975µA (T_A = +125°C)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)
36		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. The current for "On Chip Debugger" part is not included.
47	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
52	7. Flash Memory Write/Erase Characteristics	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C) (V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Page	Section	Change Results
52	■ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics	Changed the Note While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing, be sure to turn the power off by using an external voltage detector. While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
56	■ORDERING INFORMATION	Deleted the Part number MCU with CAN controller MB96F612RBPMC-GTE2 MB96F613RBPMC-GTE2 MB96F615RBPMC-GTE2 MCU without CAN controller MB96F612ABPMC-GTE2 MB96F613ABPMC-GTE2 MB96F615ABPMC-GTE2
Revision 3.1		
-	-	Company name and layout design change
Rev.*B		
6, 8, 58, 59	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-48P-M26 → LQA048
58	16. Ordering Information	Added the following part number. MB96F612RBPMC-GS-UJE1, MB96F612RBPMC-GS-UJE2, MB96F613RBPMC-GS-UJE1, MB96F613RBPMC-GS-UJE2, MB96F615RBPMC-GS-UJE1, MB96F615RBPMC-GS-UJE2, MB96F612ABPMC-GS-UJE1, MB96F612ABPMC-GS-UJE2 MB96F613ABPMC-GS-UJE1, MB96F613ABPMC-GS-UJE2 MB96F615ABPMC-GS-UJE1, MB96F615ABPMC-GS-UJE2
Rev.*C		
58	16. Ordering Information	Deleted the Part number MCU without CAN controller MB96F615ABPMC-GS-UJE2
Rev.*D		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	

Page	Section	Change Results
58	16. Ordering Information	Revised Marketing Part Numbers as follows: Before) **MCU with CAN Controller** MB96F612RBPMC-GSE1 MB96F612RBPMC-GS-UJE1 MB96F612RBPMC-GSE2 MB96F612RBPMC-GS-UJE2 MB96F612RBPMC-GTE1 MB96F613RBPMC-GSE1 MB96F613RBPMC-GS-UJE1 MB96F613RBPMC-GSE2 MB96F613RBPMC-GS-UJE2 MB96F613RBPMC-GTE1 MB96F615RBPMC-GSE1 MB96F615RBPMC-GS-UJE1 MB96F615RBPMC-GSE2 MB96F615RBPMC-GS-UJE2 MB96F615RBPMC-GTE1 **MCU without CAN Controller** MB96F612ABPMC-GSE1 MB96F612ABPMC-GS-UJE1 MB96F612ABPMC-GSE2 MB96F612ABPMC-GS-UJE2 MB96F612ABPMC-GTE1 MB96F613ABPMC-GSE1 MB96F613ABPMC-GS-UJE1 MB96F613ABPMC-GSE2 MB96F613ABPMC-GS-UJE2 MB96F613ABPMC-GTE1 MB96F615ABPMC-GSE1 MB96F615ABPMC-GS-UJE1 MB96F615ABPMC-GSE2 MB96F615ABPMC-GTE1
58	16. Ordering Information	After) **MCU with CAN Controller** CY96F612RBPMC-GS-UJE1 CY96F612RBPMC-GS-UJE2 CY96F613RBPMC-GS-UJE1 CY96F613RBPMC-GS-UJE2 CY96F613RBPMC-GS-UJERE2 CY96F615RBPMC-GS-UJE1 CY96F615RBPMC-GS-UJE2 CY96F615RBPMC-GS-UJERE2 **MCU without CAN Controller** CY96F612ABPMC-GS-UJE1 CY96F612ABPMC-GS-UJE2 CY96F613ABPMC-GS-UJE1 CY96F613ABPMC-GS-UJE2 CY96F615ABPMC-GS-UJE1

Document History

Document Title: CY96610 Series, F²MC, 16FX, 16-bit Proprietary Microcontroller
Document Number: 002-04709

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04709. No change to document contents or format.
*A	5146534	KSUN	02/29/2016	Updated to Cypress template
*B	5735123	KUME	05/15/2017	Updated the Ordering Information and the Package Dimension For details, please see 18. Major Changes.
*C	5809040	MIYH	07/11/2017	Updated the Ordering Information For details, please see 18. Major Changes.
*D	5978072	MIYH	11/30/2017	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 16. Ordering Information For details, please see 18. Major Changes.