Infineon Technologies - MB96F613ABPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f613abpmc-gse2

- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

A/D Converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 ×8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

Quadrature Position/Revolution Counter (QPRC)

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

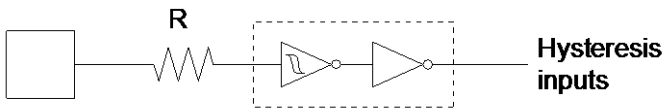
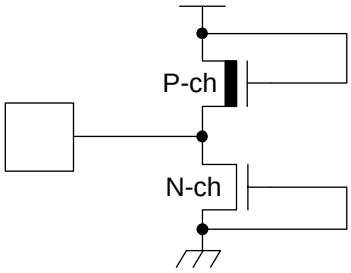
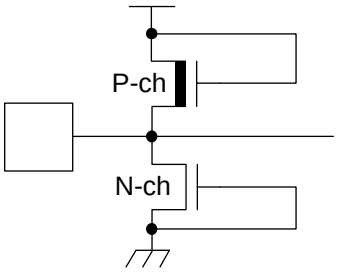
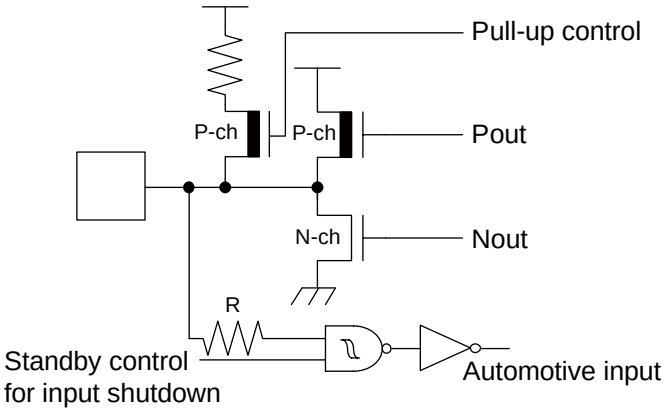
Contents

1. Product Lineup

Features		CY96610	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
32.5KB + 32KB	4KB	CY96F612R, CY96F612A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB	10KB	CY96F613R, CY96F613A	
128.5KB + 32KB	10KB	CY96F615R, CY96F615A	
Package		LQFP-48 LQA048	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO	No	
8/10-bit A/D Converter		16ch	AN 0/1/3/4/6 to 10/ 12/14/16/24/25/30/31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	No	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 0 to 3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		7ch (3 channels for LIN-USART)	ICU 0/1/4 to 6/9/10 (ICU 6/9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)		5ch	OCU 0/1/4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INT)		11ch	INT 0/2/3/4/7 to 13
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		35 (Dual clock mode) 37 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note:

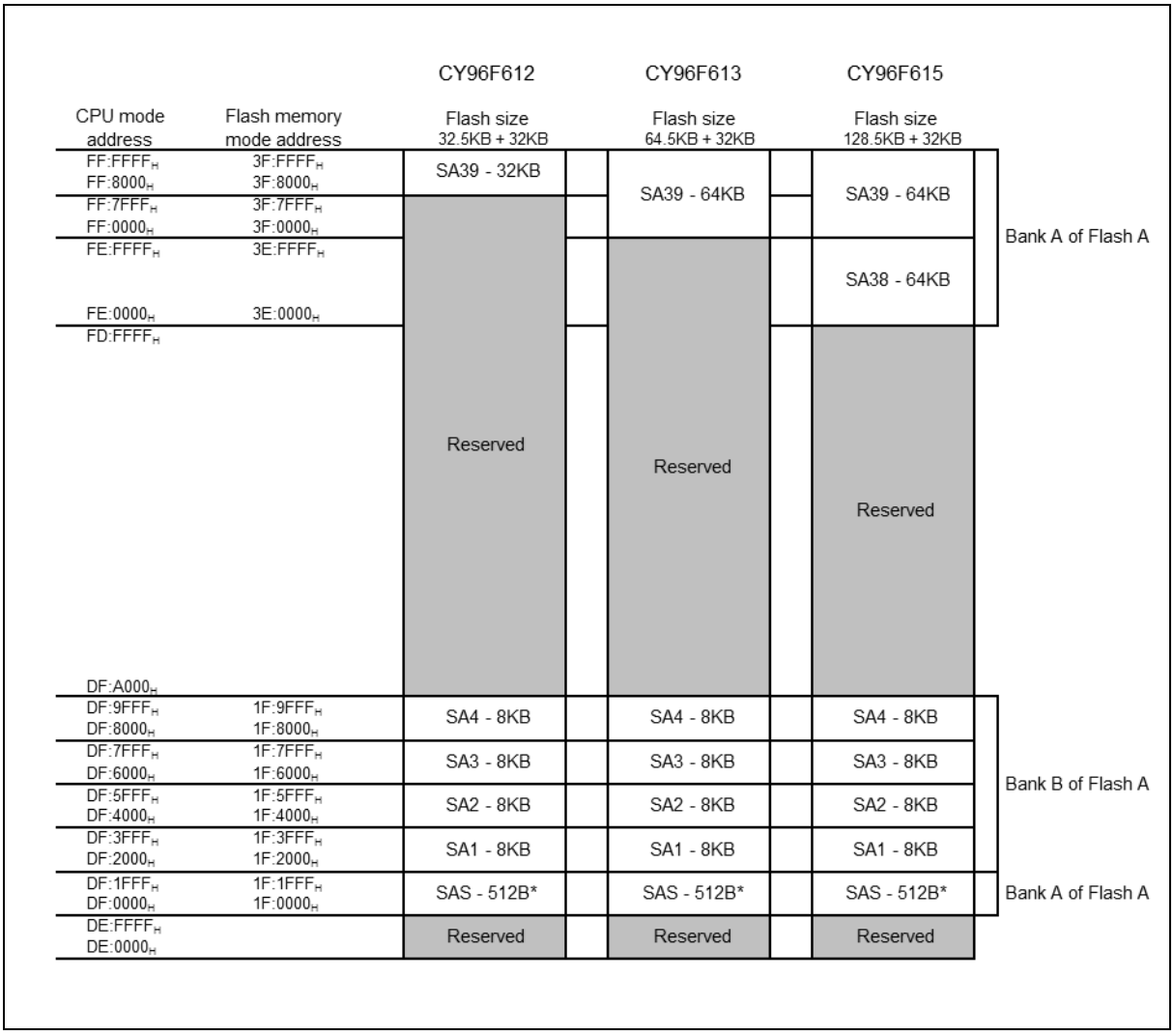
- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

Type	Circuit	Remarks
C		CMOS hysteresis input pin
F		Power supply input protection circuit
G		■ A/D converter ref+ (AVRH) power supply input pin with protection circuit ■ Without protection circuit against V_{CC} for pins AVRH
H		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor

8. RAMstart Addresses

Devices	Bank 0 RAM Size	RAMSTART0
CY96F612	4KB	$00:7200_H$
CY96F613, CY96F615	10KB	$00:5A00_H$

9. User ROM Memory Map for Flash Devices



*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

11. Interrupt Vector Table

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	-	-	18	Reserved
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	-	-	22	Reserved
23	$3A0_H$	-	-	23	Reserved
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	-	-	31	Reserved
32	$37C_H$	-	-	32	Reserved
33	378_H	-	-	33	Reserved
34	374_H	-	-	34	Reserved
35	370_H	CAN2	No	35	CAN Controller 2
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	$1D4_H$	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	-	-	140	Reserved
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable)

13.8 Pin Handling when Not Using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V_{CC} AV_{SS} = AVRH = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

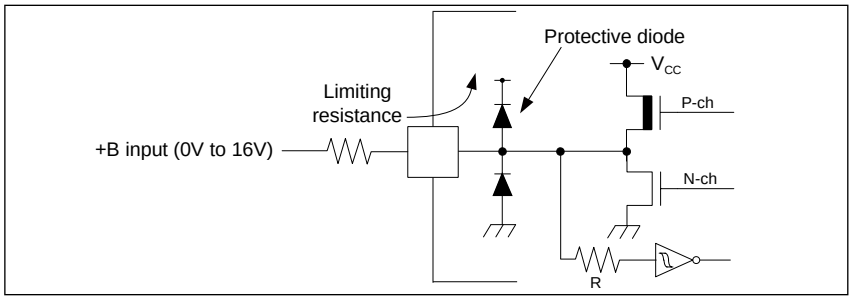
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.12 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Sample recommended circuits:



[5]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

[6]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[7]: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105°C$.

WARNING:
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes[2]	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	µA	T_A = +25°C
				-	-	3165	µA	T_A = +105°C
				-	-	3975	µA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	µA	T_A = +25°C
				-	-	1085	µA	T_A = +105°C
				-	-	1930	µA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	µA	T_A = +25°C
				-	-	1025	µA	T_A = +105°C
				-	-	1840	µA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	855	µA	T_A = +105°C
				-	-	1640	µA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	830	µA	T_A = +105°C
				-	-	1620	µA	T_A = +125°C
Power supply current in Stop mode[3]	I_{CCH}	Vcc	-	-	20	55	µA	T_A = +25°C
				-	-	825	µA	T_A = +105°C
				-	-	1615	µA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector[4]	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +125°C
Flash Write/ Erase current[5]	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

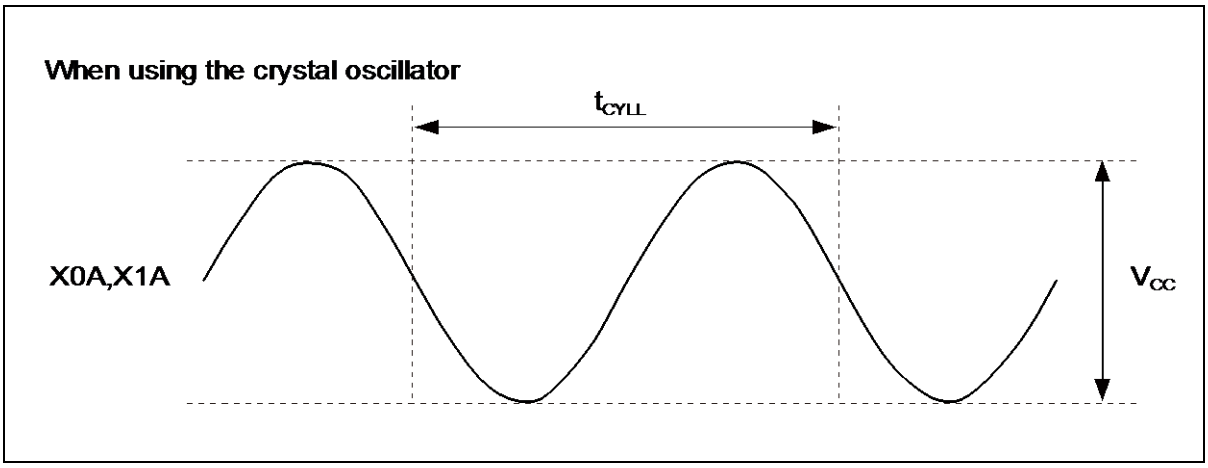
[4]: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

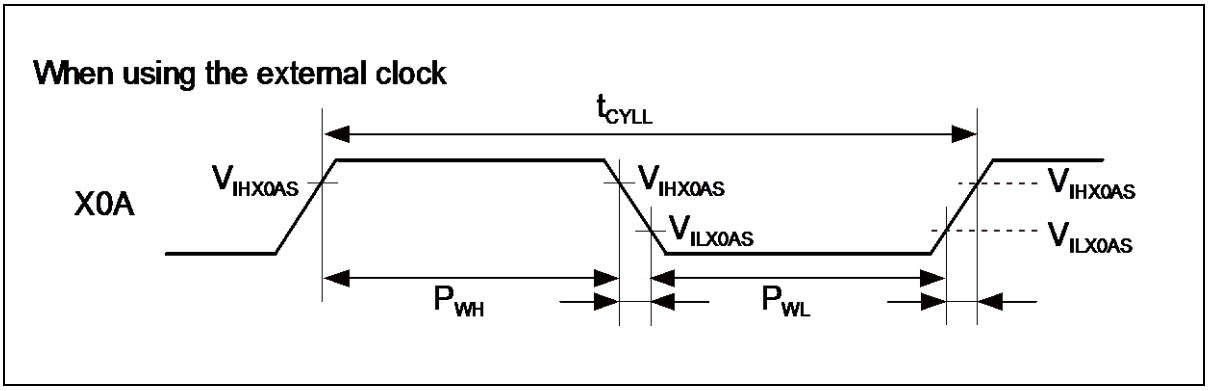
[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.3 *Built-in RC Oscillation Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 *Internal Clock Timing*

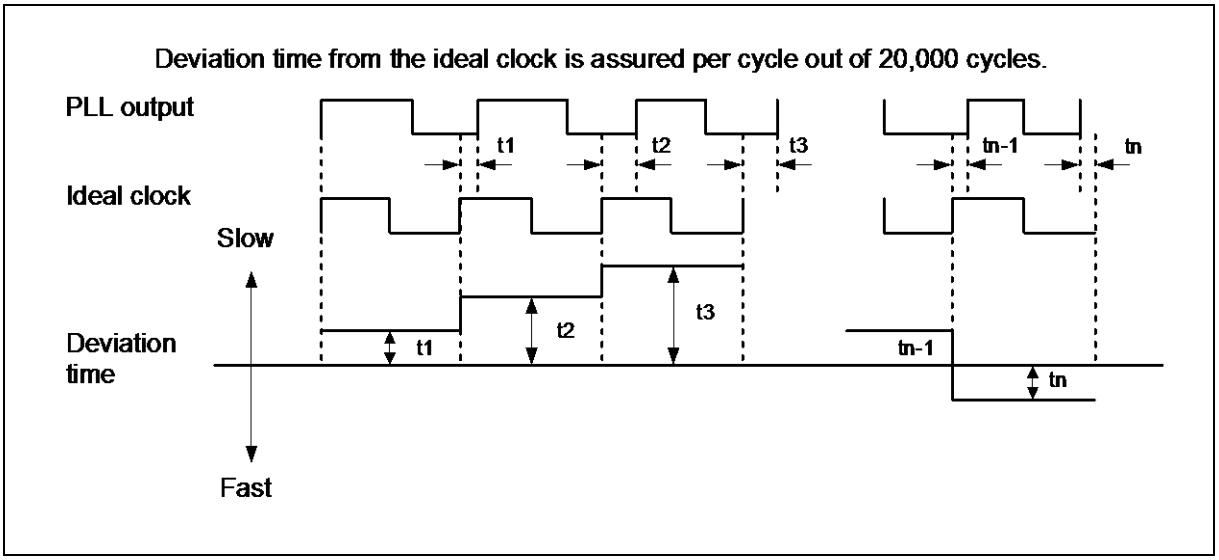
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

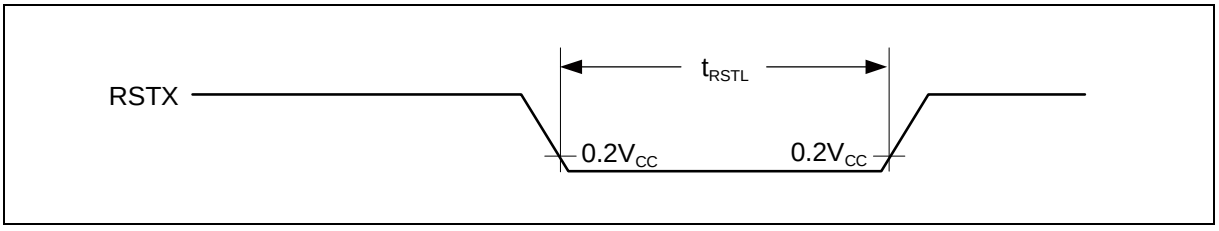
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz

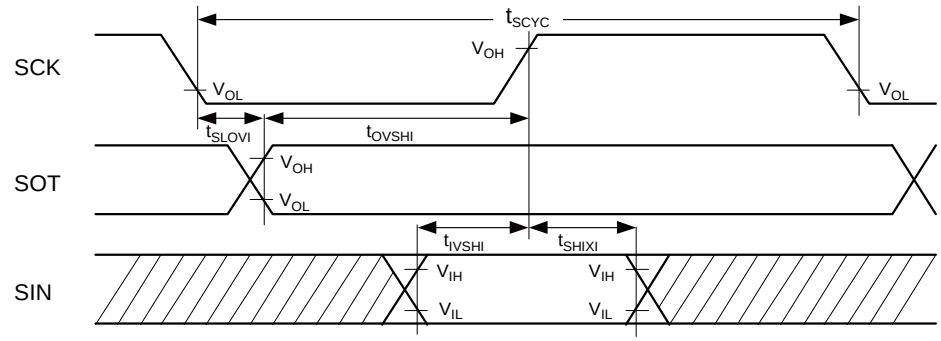


14.4.6 *Reset Input*

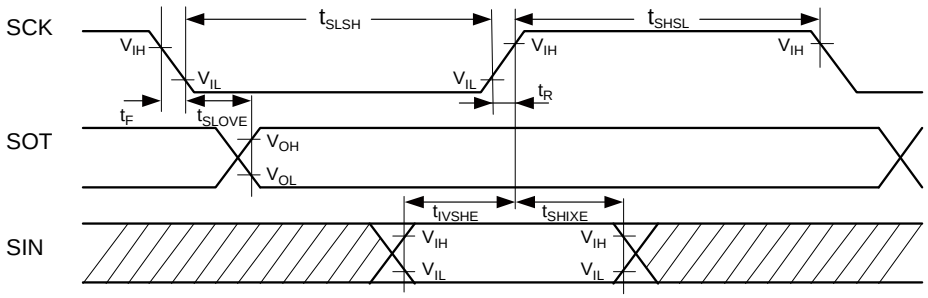
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs

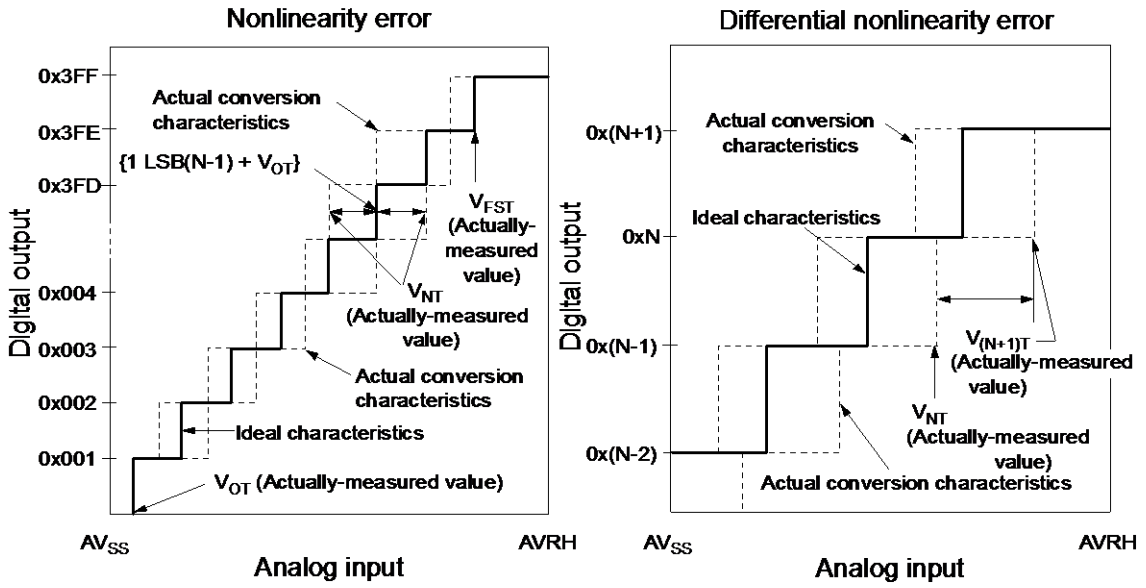




Internal shift clock mode



External shift clock mode



Nonlinearity error of digital output N = $\frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

Differential nonlinearity error of digital output N = $\frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

$1LSB = \frac{V_{FST} - V_{OT}}{1022}$

N : A/D converter digital output value.

V_O : Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.

V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

18. Major Changes

Spansion Publication Number: MB96610_DS704-00007

Page	Section	Change Results
Revision 3.0		
4	■FEATURES	Changed the description of “External Interrupts” Interrupt mask and pending bit per channel Interrupt mask bit per channel
23 to 26	■HANDLING PRECAUTIONS	Added a section
34	■ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,
		Changed the Conditions for I_{CCSRCL} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz CLKS1/2 = CLKP1/2 = CLKRC = 100kHz
35		Changed the Conditions for I_{CCTPLL} PLL Timer mode with CLKP1 = 32MHz PLL Timer mode with CLKPLL = 32MHz
		Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2480µA → 1800µA (T_A = +25°C) Max: 2710µA → 2245µA (T_A = +25°C) Max: 3985µA → 3165µA (T_A = +105°C) Max: 4830µA → 3975µA (T_A = +125°C)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)
36		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. The current for "On Chip Debugger" part is not included.
47	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
52	7. Flash Memory Write/Erase Characteristics	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C) (V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)