Infineon Technologies - MB96F613RBPMC-GS-128E2 Datasheet

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What is "Embedded - Microcontrollers"?

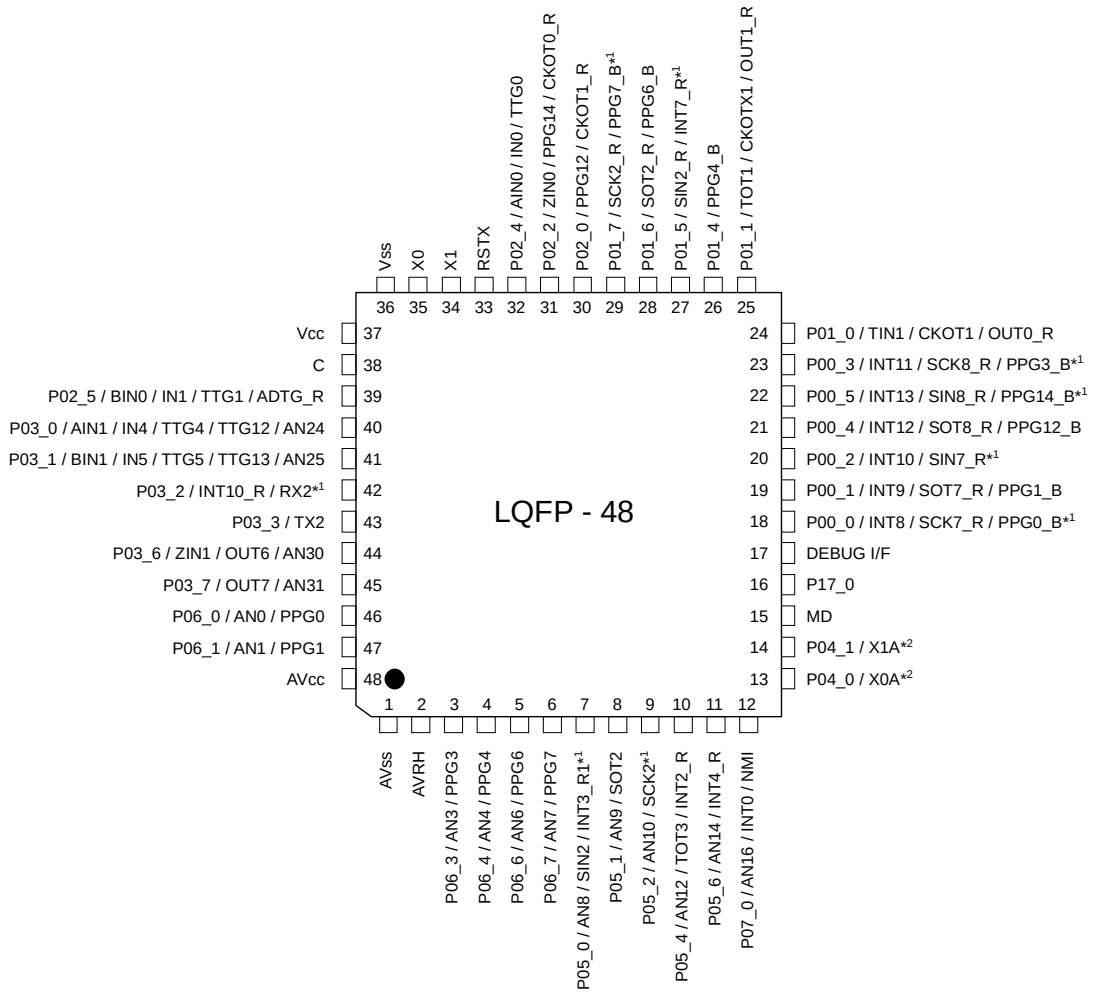
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f613rbpmc-gs-128e2

3. Pin Assignment

(Top view)



(LQA048)

*1: CMOS input level only

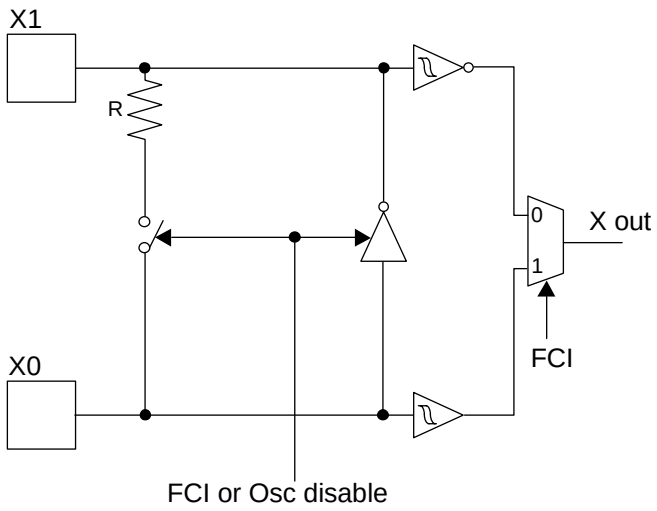
*2: Please set ROM Configuration Block (RCB) to use the subclock.

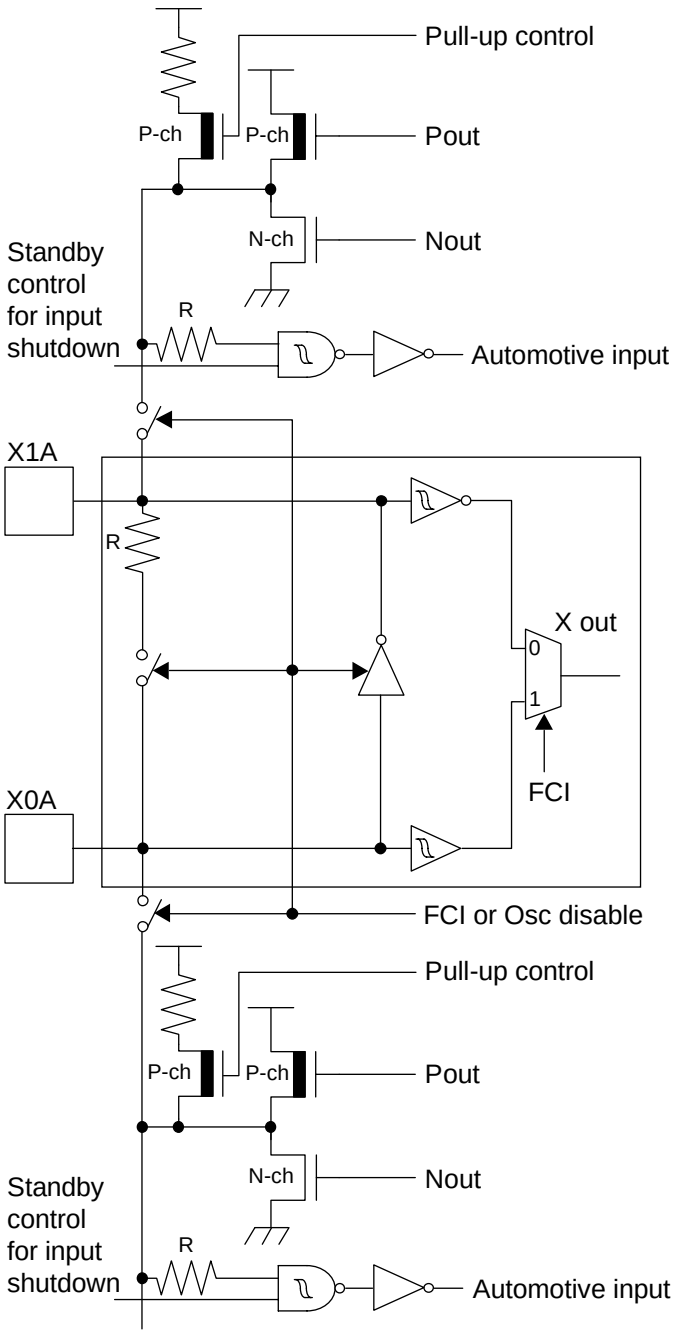
Other than those above, general-purpose pins have only Automotive input level.

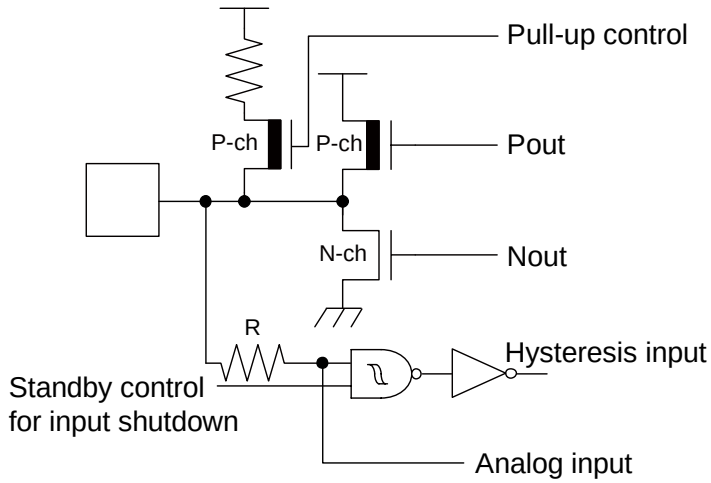
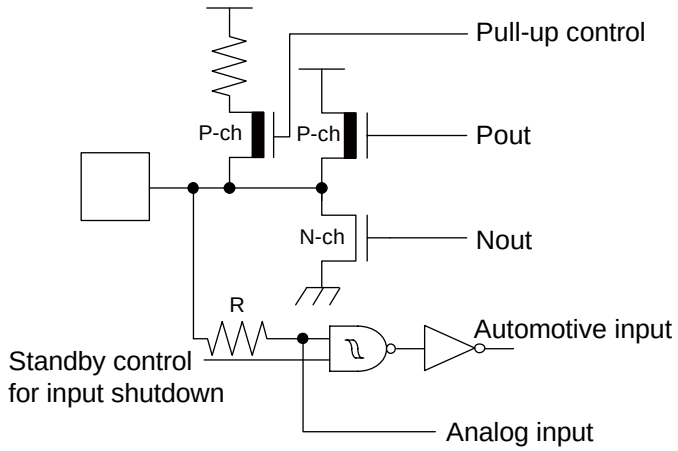
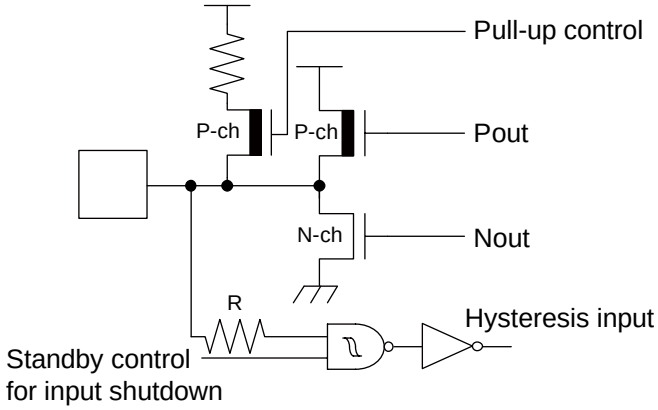
Pin No.	I/O Circuit Type*	Pin Name
33	C	RSTX
34	A	X1
35	A	X0
36	Supply	Vss
37	Supply	Vcc
38	F	C
39	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
40	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
41	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
42	M	P03_2 / INT10_R / RX2
43	H	P03_3 / TX2
44	K	P03_6 / ZIN1 / OUT6 / AN30
45	K	P03_7 / OUT7 / AN31
46	K	P06_0 / AN0 / PPG0
47	K	P06_1 / AN1 / PPG1
48	Supply	AVcc

*: See I/O Circuit Type" for details on the I/O circuit types.

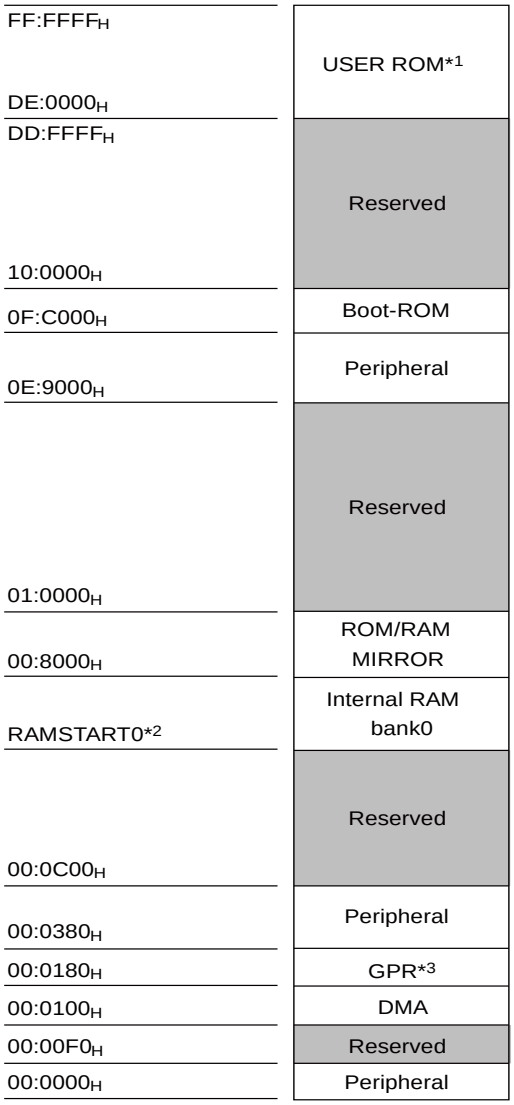
6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 1.0MΩ ■ The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: ■ Feedback resistor = approx. 5.0MΩ ■ GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)

Type	Circuit	Remarks
I		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor ■ Analog input
K		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ Analog input
M		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor

7. Memory Map



*1: For details about USER ROM area, see “
User ROM Memory Map for Flash Devices” on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	QPRC0	Yes	137	Quad Position/Revolution counter 0
138	$1D4_H$	QPRC1	Yes	138	Quad Position/Revolution counter 1
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	-	-	140	Reserved
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AVRH \geq AV_{SS}$
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	13	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	32	mA	
"L" level average overall output current	ΣI_{OLAV}	-	-	16	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-32	mA	
"H" level average overall output current	ΣI_{OHAV}	-	-	-16	mA	
Power consumption[5]	P_D	T_A= +125°C	-	284[6]	mW	
Operating ambient temperature	T_A	-	-40	+125[7]	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

[1]: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

[2]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

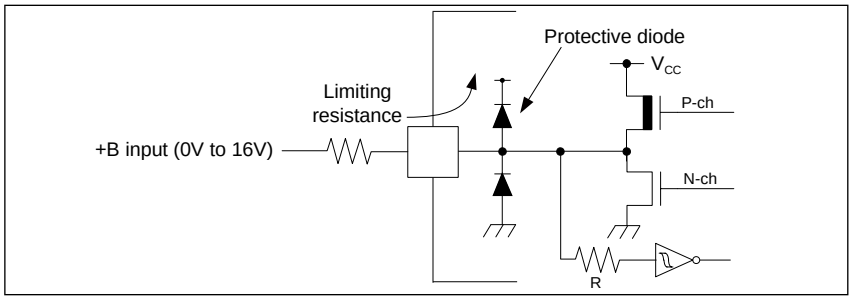
[3]: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

[4]:

- Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Sample recommended circuits:



[5]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

[6]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[7]: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105°C$.

WARNING:
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 *Current Rating*

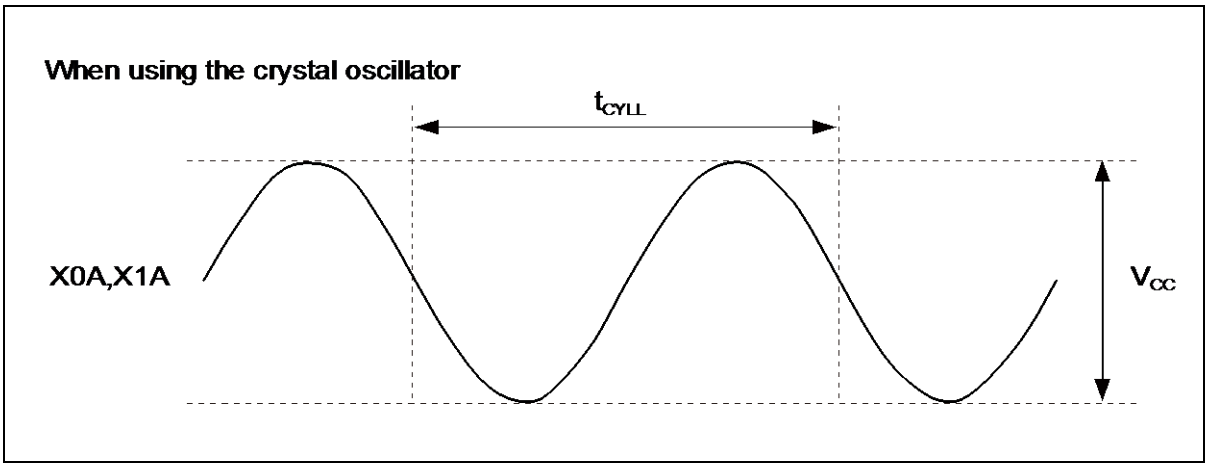
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

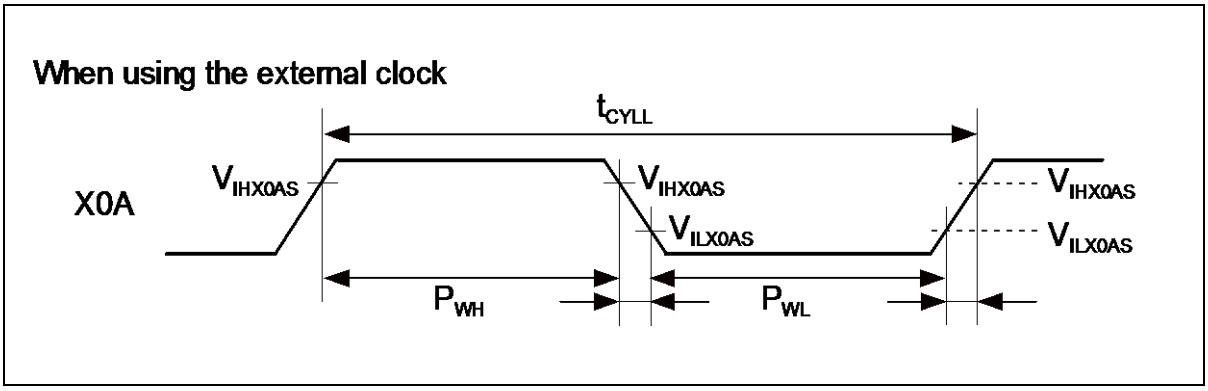
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
				-	-	35	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
				-	-	8.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
				-	-	6.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
				-	-	4.2	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	

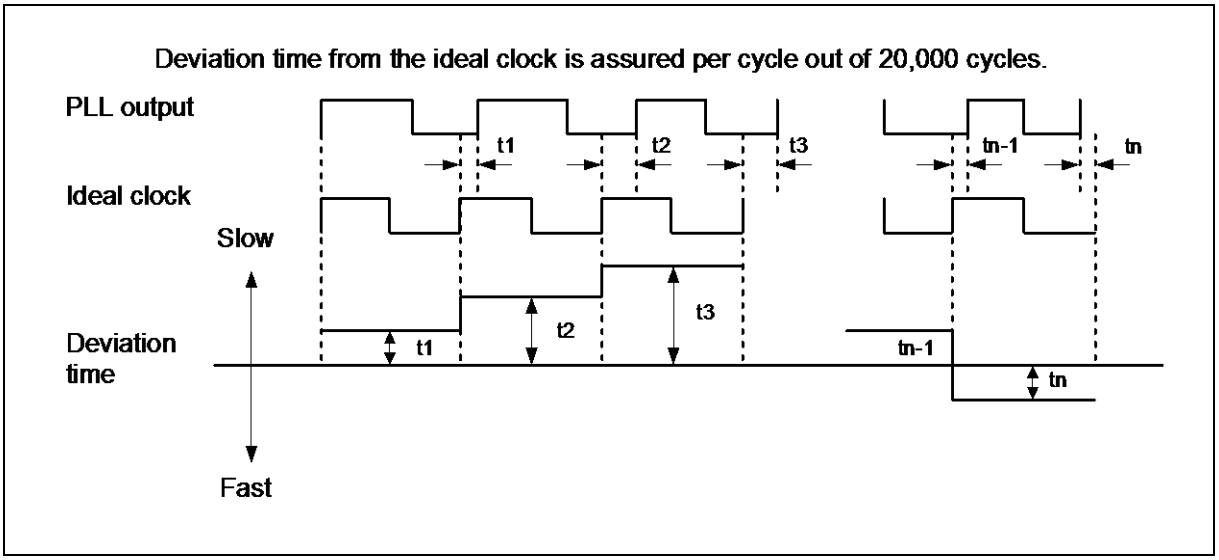




14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

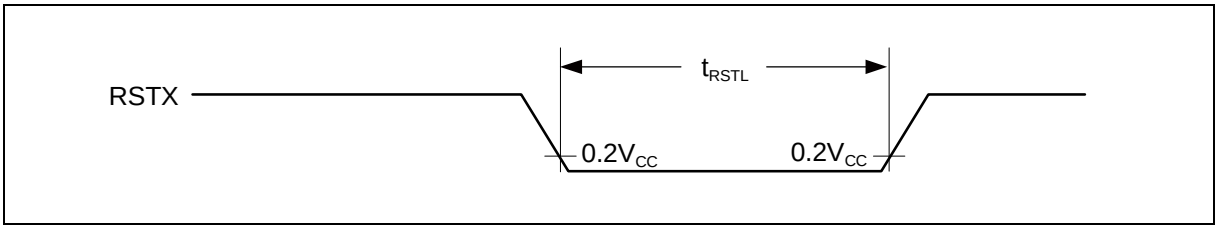
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs

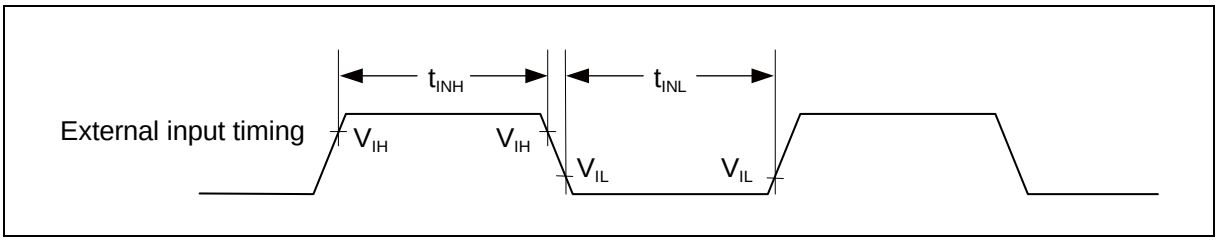


14.4.9 *External Input Timing*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}=1/f_{CLKP1})*	-	ns	General Purpose I/O
		ADTG_R				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		INn				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R, INTn_R1	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

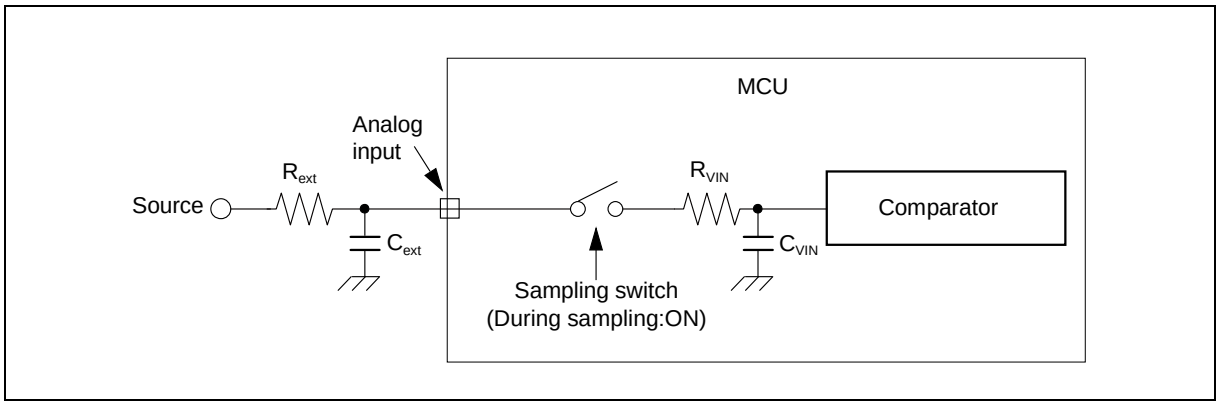
*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

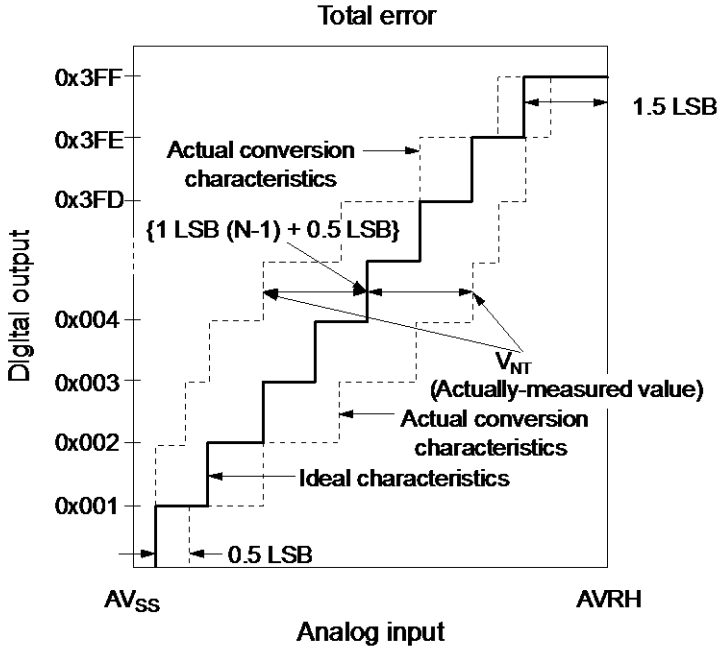
R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.



$$1LSB\ (Ideal\ value) = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT} (Ideal value) = AV_{SS} + 0.5LSB[V]
V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	T_A ≤ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	T_A ≤ + 105°C	-	25	400	µs	Not including system-level overheadtime.
	Small Sector	-	-	25	400	µs	
Chip erase time		T_A ≤ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

*To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].*

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

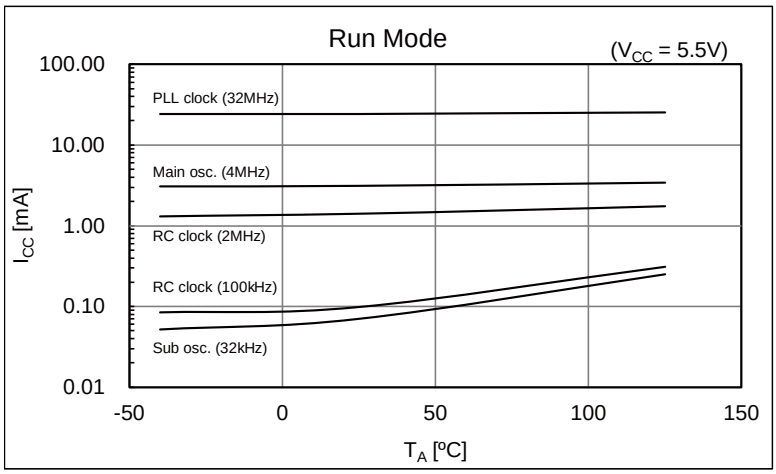
[1]:See "14.6 Low Voltage Detection Function Characteristics".

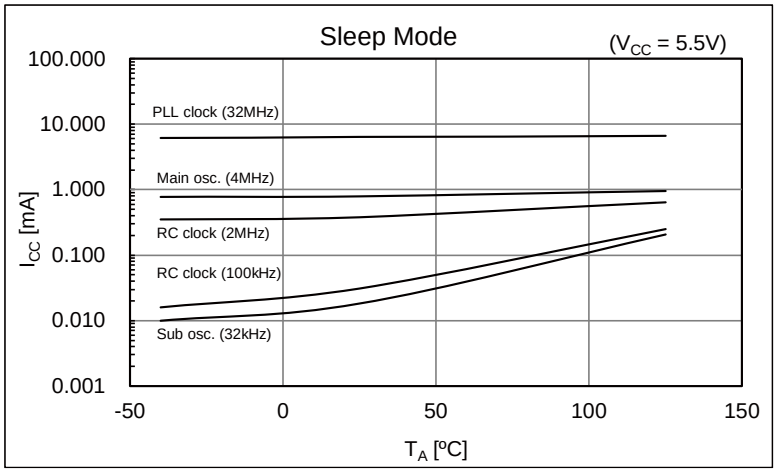
[2]:This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85˚c).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

CY96F615





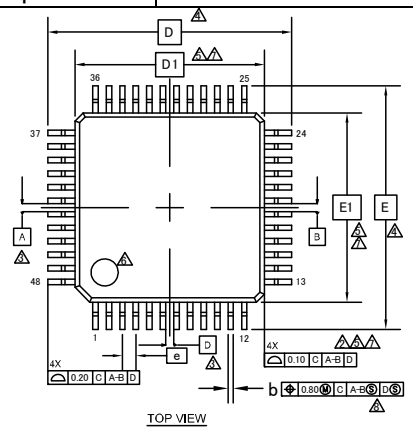
Used Setting

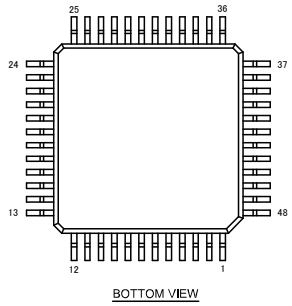
Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

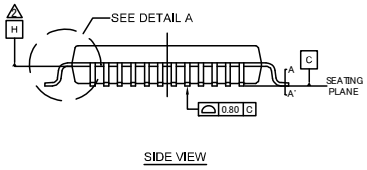
17. Package Dimension

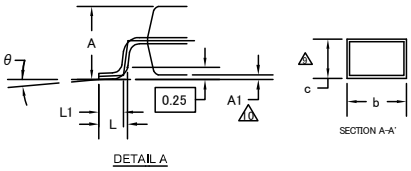
LQA048, 48 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 48pin	LQA048









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Page	Section	Change Results
52	■ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics	Changed the Note While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing, be sure to turn the power off by using an external voltage detector. While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
56	■ORDERING INFORMATION	Deleted the Part number MCU with CAN controller MB96F612RBPMC-GTE2 MB96F613RBPMC-GTE2 MB96F615RBPMC-GTE2 MCU without CAN controller MB96F612ABPMC-GTE2 MB96F613ABPMC-GTE2 MB96F615ABPMC-GTE2
Revision 3.1		
-	-	Company name and layout design change
Rev.*B		
6, 8, 58, 59	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-48P-M26 → LQA048
58	16. Ordering Information	Added the following part number. MB96F612RBPMC-GS-UJE1, MB96F612RBPMC-GS-UJE2, MB96F613RBPMC-GS-UJE1, MB96F613RBPMC-GS-UJE2, MB96F615RBPMC-GS-UJE1, MB96F615RBPMC-GS-UJE2, MB96F612ABPMC-GS-UJE1, MB96F612ABPMC-GS-UJE2 MB96F613ABPMC-GS-UJE1, MB96F613ABPMC-GS-UJE2 MB96F615ABPMC-GS-UJE1, MB96F615ABPMC-GS-UJE2
Rev.*C		
58	16. Ordering Information	Deleted the Part number MCU without CAN controller MB96F615ABPMC-GS-UJE2
Rev.*D		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	