# Infineon Technologies - MB96F613RBPMC-GSE1 Datasheet

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## What is "Embedded - Microcontrollers"?

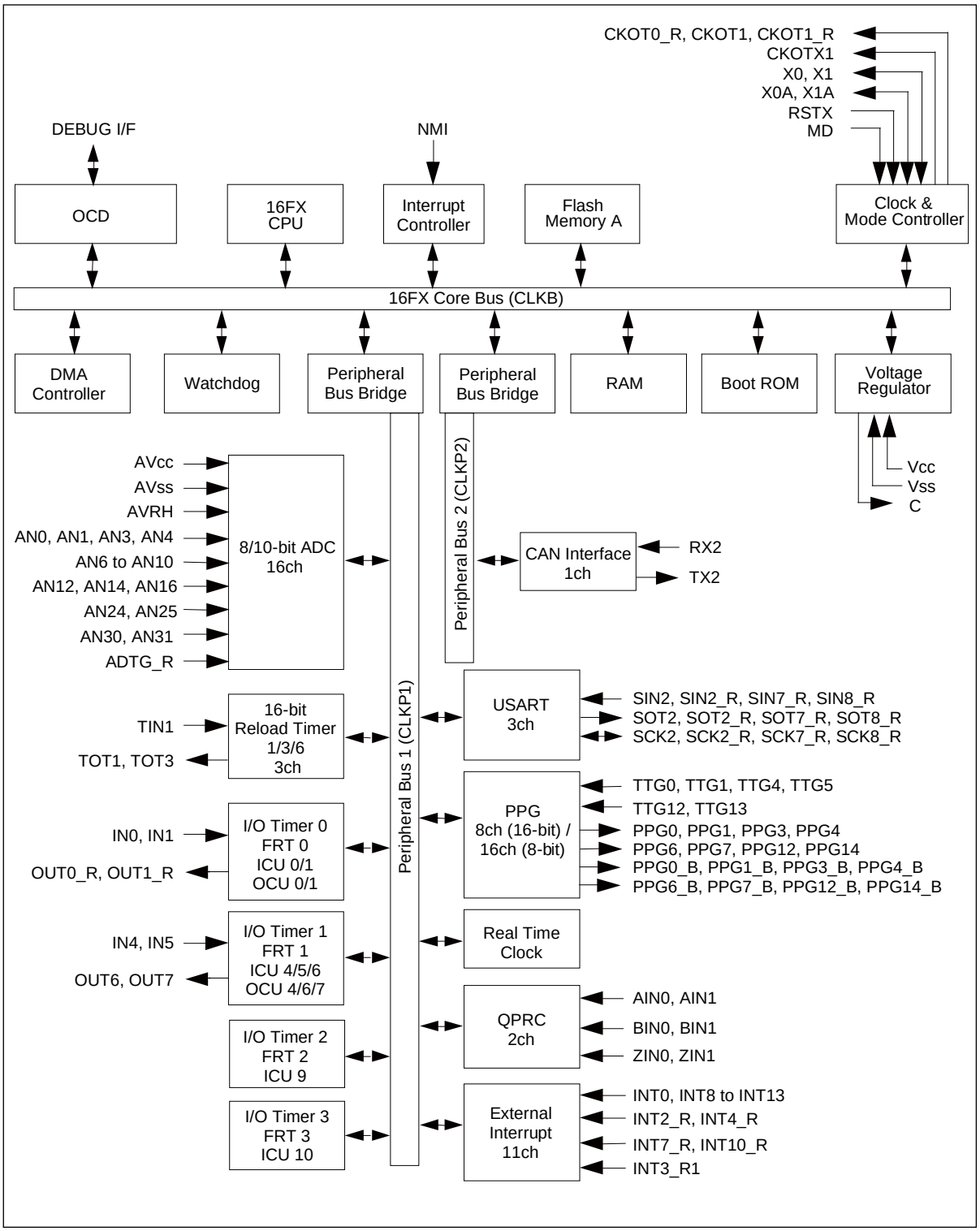
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

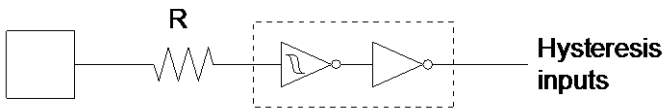
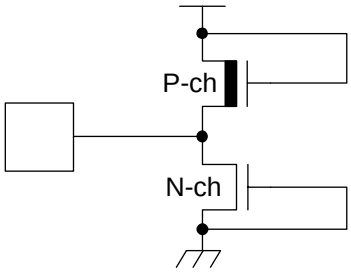
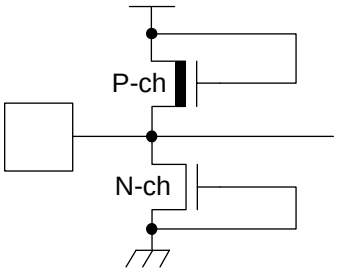
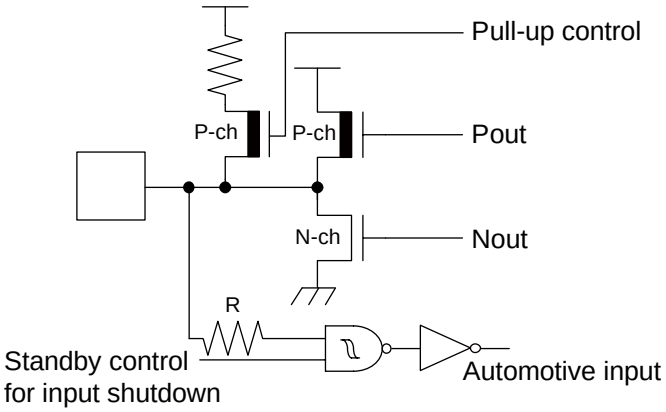
## Applications of "Embedded - Microcontrollers"

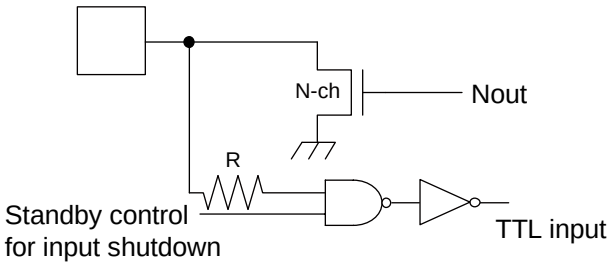
| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, SCI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 96KB (96K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f613rbpmc-gse1 |

## Contents

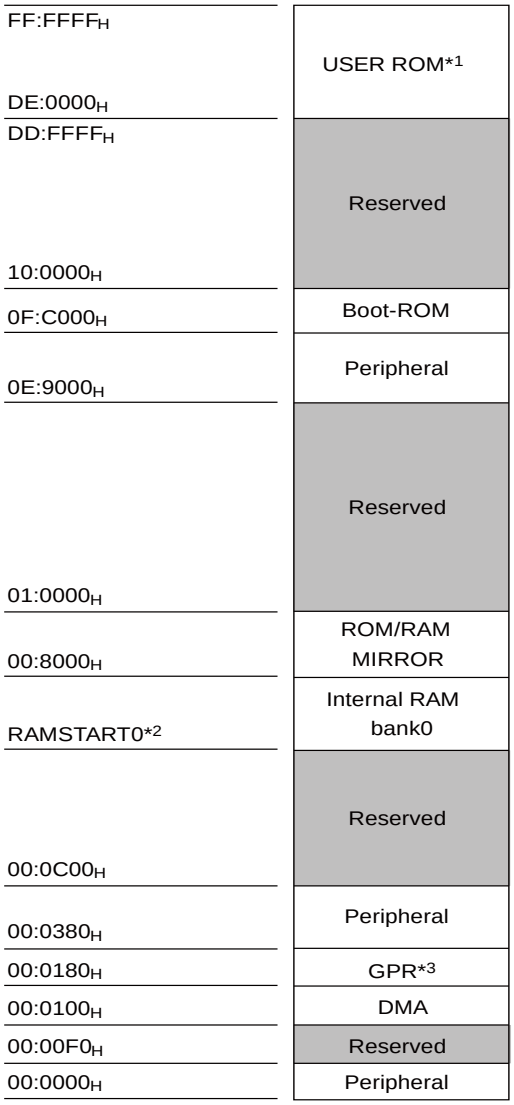
## 2. Block Diagram



| Type | Circuit | Remarks |
|---|---|---|
| C |  | CMOS hysteresis input pin |
| F |  | Power supply input protection circuit |
| G |  | ■ A/D converter ref+ (AVRH) power supply input pin with protection circuit<br>■ Without protection circuit against $V_{CC}$ for pins AVRH |
| H |  | ■ CMOS level output<br>■ ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>■ Automotive input with input shutdown function<br>■ Programmable pull-up resistor |

| Type | Circuit | Remarks |
|---|---|---|
| O |  | ■ Open-drain I/O<br>■ Output 25mA, Vcc = 2.7V<br>■ TTL input |

## 7. Memory Map




*1: For details about USER ROM area, see “
User ROM Memory Map for Flash Devices” on the following pages.

*2: For RAMSTART addresses, see the table on the next page.

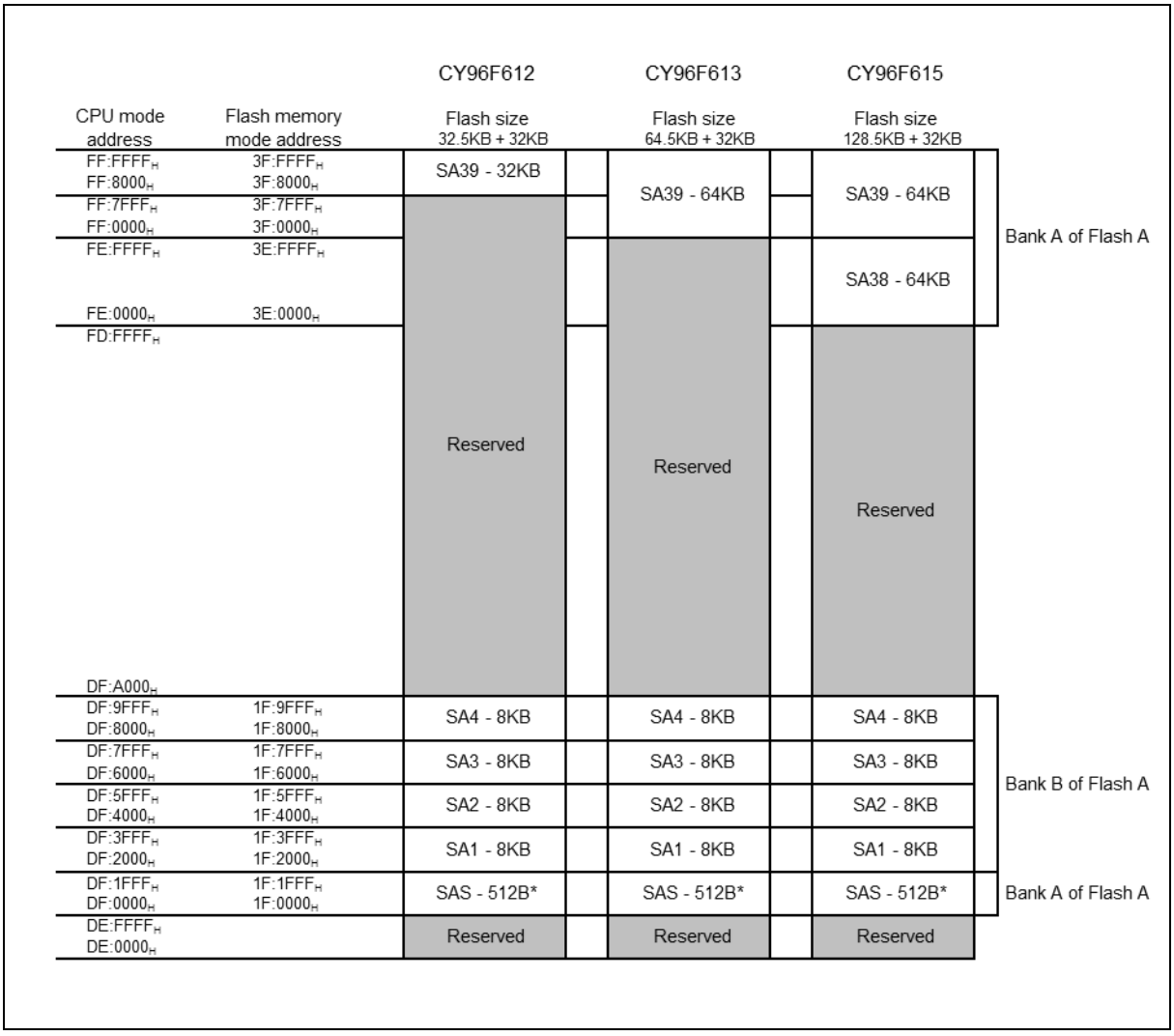
*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

## 9. User ROM Memory Map for Flash Devices




*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for $E^2$PROM emulation.

## 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

| CY96610 | | |
|---|---|---|
| **Pin Number** | **USART Number** | **Normal Function** |
| 7 | USART2 | SIN2 |
| 8 | | SOT2 |
| 9 | | SCK2 |
| 20 | USART7 | SIN7_R |
| 19 | | SOT7_R |
| 18 | | SCK7_R |
| 22 | USART8 | SIN8_R |
| 21 | | SOT8_R |
| 23 | | SCK8_R |

| Vector Number | Offset in Vector Table | Vector Name | Cleared by DMA | Index in ICR to Program | Description |
|---|---|---|---|---|---|
| 81 | $2B8_H$ | OCU4 | Yes | 81 | Output Compare Unit 4 |
| 82 | $2B4_H$ | - | - | 82 | Reserved |
| 83 | $2B0_H$ | OCU6 | Yes | 83 | Output Compare Unit 6 |
| 84 | $2AC_H$ | OCU7 | Yes | 84 | Output Compare Unit 7 |
| 85 | $2A8_H$ | - | - | 85 | Reserved |
| 86 | $2A4_H$ | - | - | 86 | Reserved |
| 87 | $2A0_H$ | - | - | 87 | Reserved |
| 88 | $29C_H$ | - | - | 88 | Reserved |
| 89 | $298_H$ | FRT0 | Yes | 89 | Free-Running Timer 0 |
| 90 | $294_H$ | FRT1 | Yes | 90 | Free-Running Timer 1 |
| 91 | $290_H$ | FRT2 | Yes | 91 | Free-Running Timer 2 |
| 92 | $28C_H$ | FRT3 | Yes | 92 | Free-Running Timer 3 |
| 93 | $288_H$ | RTC0 | No | 93 | Real Time Clock |
| 94 | $284_H$ | CAL0 | No | 94 | Clock Calibration Unit |
| 95 | $280_H$ | - | - | 95 | Reserved |
| 96 | $27C_H$ | - | - | 96 | Reserved |
| 97 | $278_H$ | - | - | 97 | Reserved |
| 98 | $274_H$ | ADC0 | Yes | 98 | A/D Converter 0 |
| 99 | $270_H$ | - | - | 99 | Reserved |
| 100 | $26C_H$ | - | - | 100 | Reserved |
| 101 | $268_H$ | - | - | 101 | Reserved |
| 102 | $264_H$ | - | - | 102 | Reserved |
| 103 | $260_H$ | - | - | 103 | Reserved |
| 104 | $25C_H$ | - | - | 104 | Reserved |
| 105 | $258_H$ | LINR2 | Yes | 105 | LIN USART 2 RX |
| 106 | $254_H$ | LINT2 | Yes | 106 | LIN USART 2 TX |
| 107 | $250_H$ | - | - | 107 | Reserved |
| 108 | $24C_H$ | - | - | 108 | Reserved |
| 109 | $248_H$ | - | - | 109 | Reserved |
| 110 | $244_H$ | - | - | 110 | Reserved |
| 111 | $240_H$ | - | - | 111 | Reserved |
| 112 | $23C_H$ | - | - | 112 | Reserved |
| 113 | $238_H$ | - | - | 113 | Reserved |
| 114 | $234_H$ | - | - | 114 | Reserved |
| 115 | $230_H$ | LINR7 | Yes | 115 | LIN USART 7 RX |
| 116 | $22C_H$ | LINT7 | Yes | 116 | LIN USART 7 TX |
| 117 | $228_H$ | LINR8 | Yes | 117 | LIN USART 8 RX |
| 118 | $224_H$ | LINT8 | Yes | 118 | LIN USART 8 TX |
| 119 | $220_H$ | - | - | 119 | Reserved |
| 120 | $21C_H$ | - | - | 120 | Reserved |
| 121 | $218_H$ | - | - | 121 | Reserved |

***CAUTION:***
*The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:*

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

■ Observance of Safety Regulations and Standards
Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design
Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
***CAUTION:***
*Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.*

## 12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

## 14.2 Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 2.7 | - | 5.5 | V | |
| | | 2.0 | - | 5.5 | V | Maintains RAM data in stop mode |
| Smoothing capacitor at C pin | $C_S$ | 0.5 | 1.0 to 3.9 | 4.7 | µF | 1.0µF (Allowance within ± 50%)<br>3.9µF (Allowance within ± 20%)<br>Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at $V_{CC}$ must use the one of a capacity value that is larger than $C_S$. |

***WARNING:***

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 14.3 DC Characteristics

### 14.3.1 *Current Rating*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Run modes[1] | $I_{CCPLL}$ | Vcc | PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz<br>Flash 0 wait<br>(CLKRC and CLKSC stopped) | - | 25 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 34 | mA | $T_A$ = +105°C |
| | | | | - | - | 35 | mA | $T_A$ = +125°C |
| | $I_{CCMAIN}$ | | Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz<br>Flash 0 wait<br>(CLKPLL, CLKSC and CLKRC stopped) | - | 3.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 7.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 8.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCH}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 1.7 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 5.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 6.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCL}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 0.15 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3.2 | mA | $T_A$ = +105°C |
| | | | | - | - | 4.2 | mA | $T_A$ = +125°C |
| | $I_{CCSUB}$ | | Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKRC stopped) | - | 0.1 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3 | mA | $T_A$ = +105°C |
| | | | | - | - | 4 | mA | $T_A$ = +125°C |

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Timer modes[2] | $I_{CCTPLL}$ | Vcc | PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped) | - | 1800 | 2245 | µA | $T_A$ = +25°C |
| | | | | - | - | 3165 | µA | $T_A$ = +105°C |
| | | | | - | - | 3975 | µA | $T_A$ = +125°C |
| | $I_{CCTMAIN}$ | | Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped) | - | 285 | 325 | µA | $T_A$ = +25°C |
| | | | | - | - | 1085 | µA | $T_A$ = +105°C |
| | | | | - | - | 1930 | µA | $T_A$ = +125°C |
| | $I_{CCTRCH}$ | | RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) | - | 160 | 210 | µA | $T_A$ = +25°C |
| | | | | - | - | 1025 | µA | $T_A$ = +105°C |
| | | | | - | - | 1840 | µA | $T_A$ = +125°C |
| | $I_{CCTRCL}$ | | RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped) | - | 35 | 75 | µA | $T_A$ = +25°C |
| | | | | - | - | 855 | µA | $T_A$ = +105°C |
| | | | | - | - | 1640 | µA | $T_A$ = +125°C |
| | $I_{CCTSUB}$ | | Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped) | - | 25 | 65 | µA | $T_A$ = +25°C |
| | | | | - | - | 830 | µA | $T_A$ = +105°C |
| | | | | - | - | 1620 | µA | $T_A$ = +125°C |
| Power supply current in Stop mode[3] | $I_{CCH}$ | Vcc | - | - | 20 | 55 | µA | $T_A$ = +25°C |
| | | | | - | - | 825 | µA | $T_A$ = +105°C |
| | | | | - | - | 1615 | µA | $T_A$ = +125°C |
| Flash Power Down current | $I_{CCFLASHPD}$ | | - | - | 36 | 70 | µA | |
| Power supply current for active Low Voltage detector[4] | $I_{CCLVD}$ | | Low voltage detector enabled | - | 5 | - | µA | $T_A$ = +25°C |
| | | | | - | - | 12.5 | µA | $T_A$ = +125°C |
| Flash Write/ Erase current[5] | $I_{CCFLASH}$ | | - | - | 12.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 20 | mA | $T_A$ = +125°C |

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

[4]: When low voltage detector is enabled, $I_{CCLVD}$ must be added to Power supply current.

[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

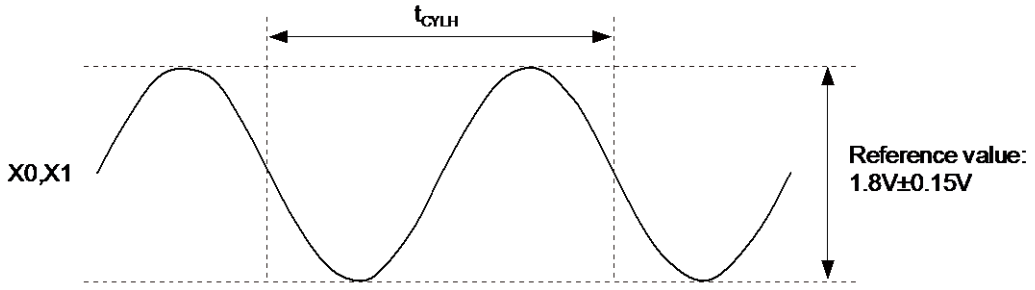
## 14.4 AC Characteristics

### 14.4.1 *Main Clock Input Characteristics*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, VD=1.8V±0.15V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

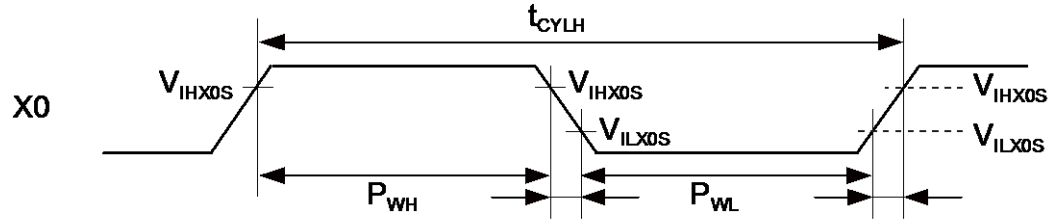
| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Input frequency | $f_C$ | X0, X1 | 4 | - | 8 | MHz | When using a crystal oscillator, PLL off |
| | | | - | - | 8 | MHz | When using an opposite phase external clock, PLL off |
| | | | 4 | - | 8 | MHz | When using a crystal oscillator or opposite phase external clock, PLL on |
| Input frequency | $f_{FCI}$ | X0 | - | - | 8 | MHz | When using a single phase external clock in “Fast Clock Input mode”, PLL off |
| | | | 4 | - | 8 | MHz | When using a single phase external clock in “Fast Clock Input mode”, PLL on |
| Input clock cycle | $t_{CYLH}$ | - | 125 | - | - | ns | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | - | 55 | - | - | ns | |

**When using the crystal oscillator**




**The amplitude changes by resistance, capacity which added outside or the difference of the device.**

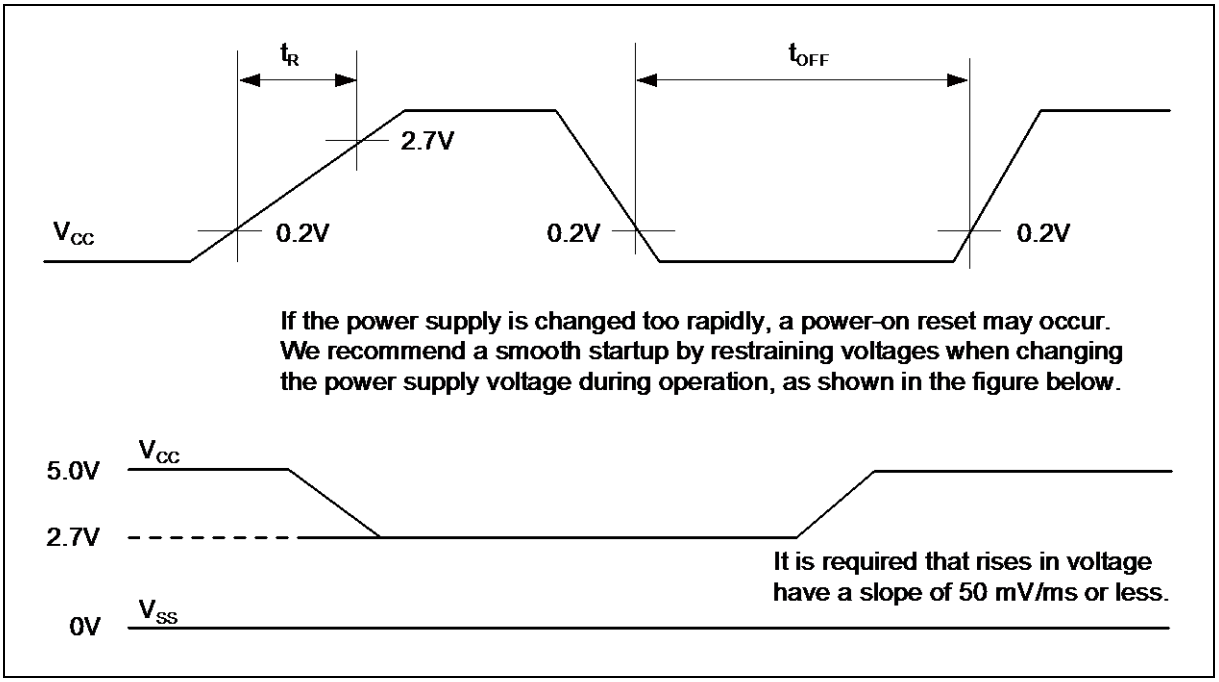
**When using the external clock**



### 14.4.7 *Power-on Reset Timing*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin Name | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power on rise time | $t_R$ | Vcc | 0.05 | - | 30 | ms |
| Power off time | $t_{OFF}$ | Vcc | 1 | - | - | ms |



### 14.4.8 *USART Timing*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C, $C_L$=50pF)

| Parameter | Symbol | Pin name | Conditions | 4.5V ≤ $V_{CC}$ <5.5V | | 2.7V ≤ $V_{CC}$ <4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKn | Internal shift clock mode | $4t_{CLKP1}$ | - | $4t_{CLKP1}$ | - | ns |
| SCK ↓ →SOT delay time | $t_{SLOVI}$ | SCKn, SOTn | | - 20 | + 20 | - 30 | + 30 | ns |
| SOT → SCK ↑ delay time | $t_{OVSHI}$ | SCKn, SOTn | | $N \times t_{CLKP1} - 20^*$ | - | $N \times t_{CLKP1} - 30^*$ | - | ns |
| SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKn, SINn | | $t_{CLKP1}$+ 45 | - | $t_{CLKP1}$ + 55 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXI}$ | SCKn, SINn | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKn | External shift clock mode | $t_{CLKP1}$+ 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKn | | $t_{CLKP1}$+ 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKn, SOTn | | - | $2t_{CLKP1}$ + 45 | - | $2t_{CLKP1}$ + 55 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKn, SINn | | $t_{CLKP1}$/2+ 10 | - | $t_{CLKP1}$/2 + 10 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXE}$ | SCKn, SINn | | $t_{CLKP1}$+ 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK fall time | $t_F$ | SCKn | | - | 20 | - | 20 | ns |
| SCK rise time | $t_R$ | SCKn | | - | 20 | - | 20 | ns |

***Notes:***

- *AC characteristic in CLK synchronized mode*
- *$C_L$ is he load capacity value of pins when testing.*
- *Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96600 series HARDWARE MANUAL".*
- *$t_{CLKP1}$ indicates the peripheral clock 1 (CLKP1), Unit: ns*
  *These characteristics only guarantee the same relocate port number.*

For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on $t_{SCYC}$ and can be calculated as follows:

- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

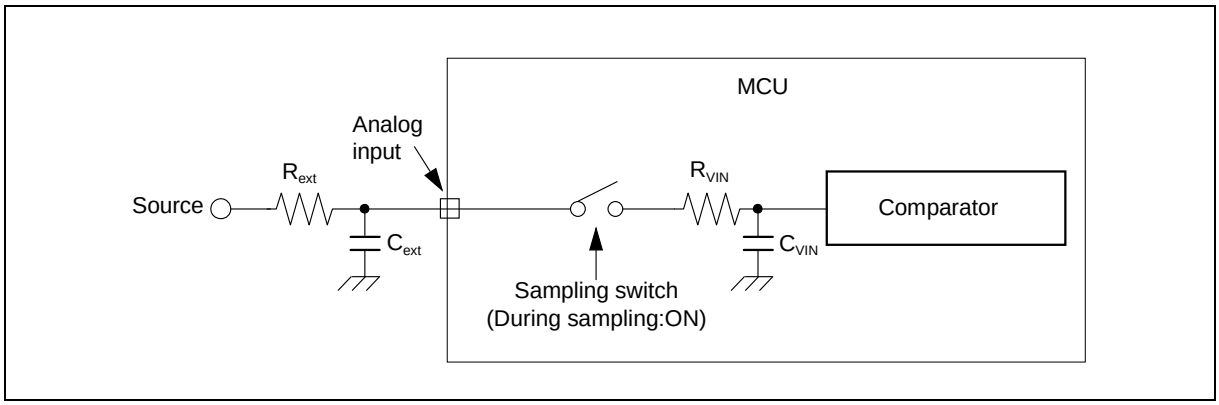
Examples:

| $t_{SCYC}$ | N |
|---|---|
| $4 \times t_{CLKP1}$ | 2 |
| $5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$ | 3 |
| $7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$ | 4 |

### 14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance $R_{ext}$, the board capacitance of the A/D converter input pin $C_{ext}$ and the $AV_{CC}$ voltage level. The following replacement model can be used for the calculation:




$R_{ext}$: External driving impedance

$C_{ext}$: Capacitance of PCB at A/D converter input

$C_{VIN}$: Analog input capacity (I/O, analog switch and ADC are contained)

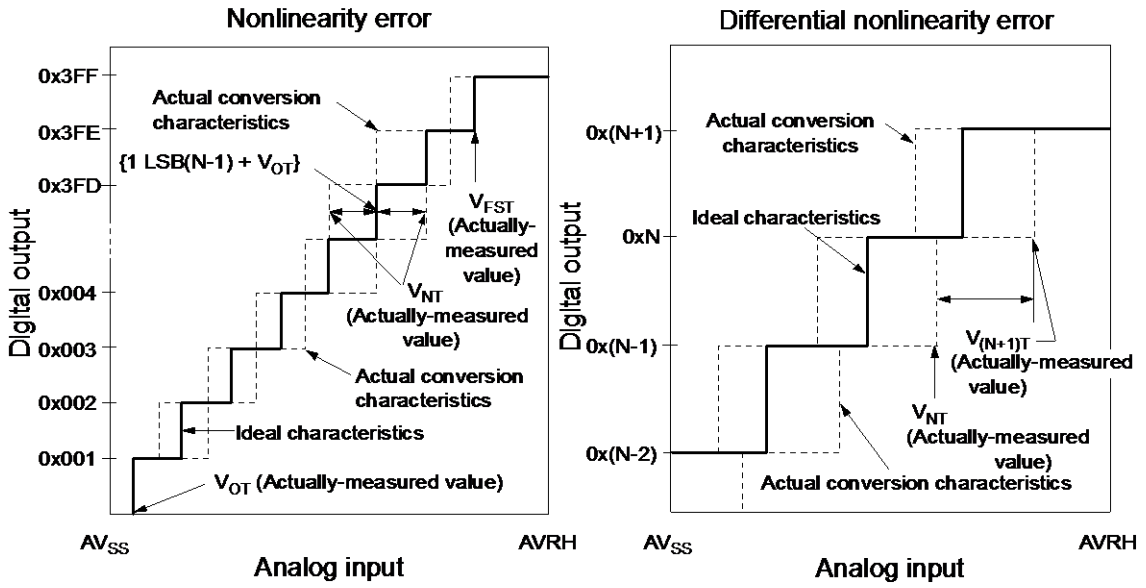
$R_{VIN}$: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

### 14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.




Nonlinearity error of digital output N = $\frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

Differential nonlinearity error of digital output N = $\frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

$1LSB = \frac{V_{FST} - V_{OT}}{1022}$

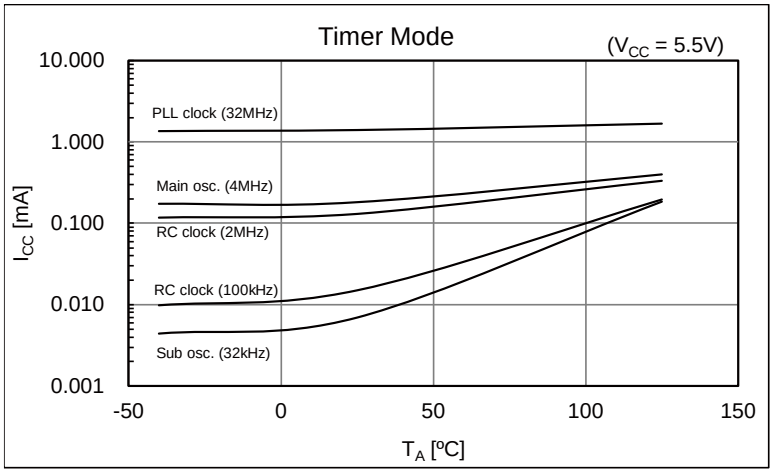
N : A/D converter digital output value.

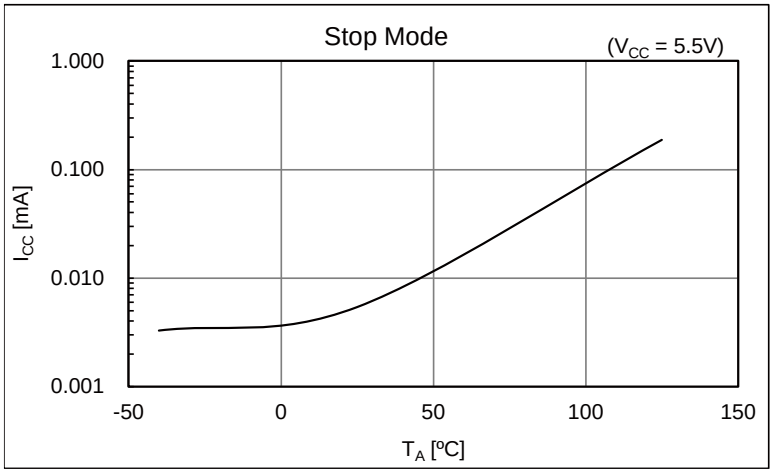
$V_O$ : Voltage at which the digital output changes from 0x000 to 0x001.

$V_{FST}$ : Voltage at which the digital output changes from 0x3FE to 0x3FF.

$V_{NT}$ : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

CY96F615

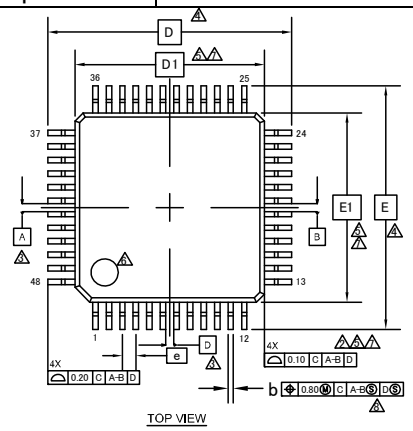

Timer Mode
($V_{CC}$ = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}$ [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
$T_A$ [ºC]

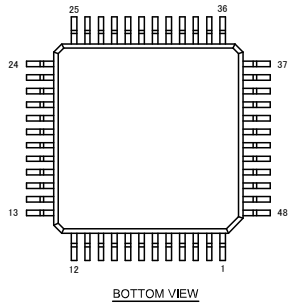

Stop Mode
($V_{CC}$ = 5.5V)
1.000
0.100
0.010
0.001
$I_{CC}$ [mA]
-50
0
50
100
150
$T_A$ [ºC]

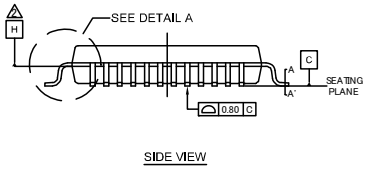
# 17. Package Dimension

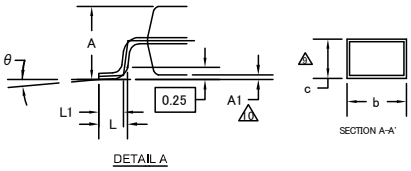
## LQA048, 48 Lead Plastic Low Profile Quad Flat Package

| Package Type | Package Code |
|---|---|
| LQFP 48pin | LQA048 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

## Document History

**Document Title: CY96610 Series, F²MC, 16FX, 16-bit Proprietary Microcontroller**
**Document Number: 002-04709**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | – | KSUN | 01/31/2014 | Migrated to Cypress and assigned document number 002-04709.<br>No change to document contents or format. |
| *A | 5146534 | KSUN | 02/29/2016 | Updated to Cypress template |
| *B | 5735123 | KUME | 05/15/2017 | Updated the Ordering Information and the Package Dimension<br>For details, please see 18. Major Changes. |
| *C | 5809040 | MIYH | 07/11/2017 | Updated the Ordering Information<br>For details, please see 18. Major Changes. |
| *D | 5978072 | MIYH | 11/30/2017 | Revised the following items:<br>Marketing Part Numbers changed from an MB prefix to a CY prefix.<br>16. Ordering Information<br>For details, please see 18. Major Changes. |