# Infineon Technologies - MB96F613RBPMC-GSE2 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, SCI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 96KB (96K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 10K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f613rbpmc-gse2 |

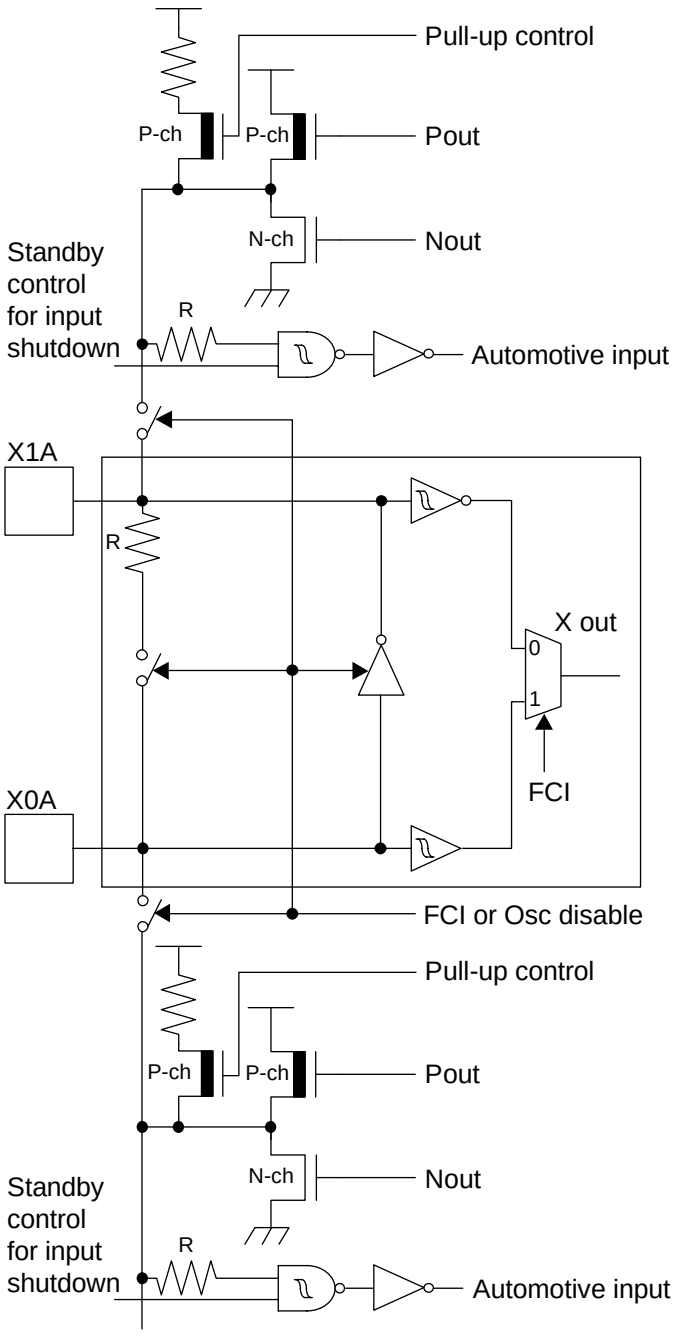
# 1. Product Lineup

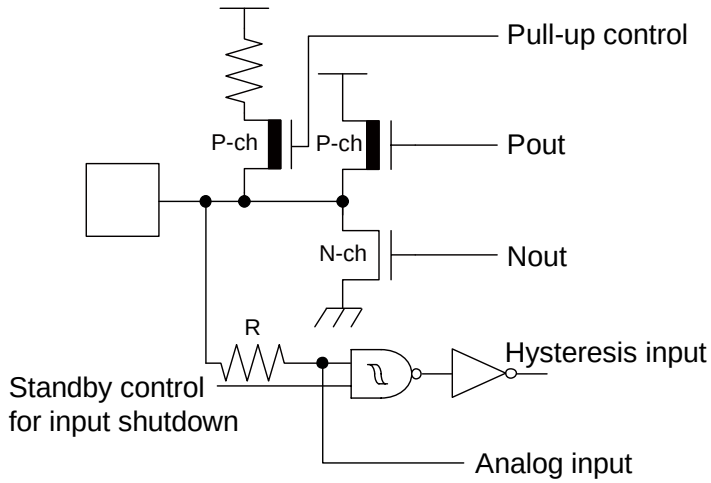
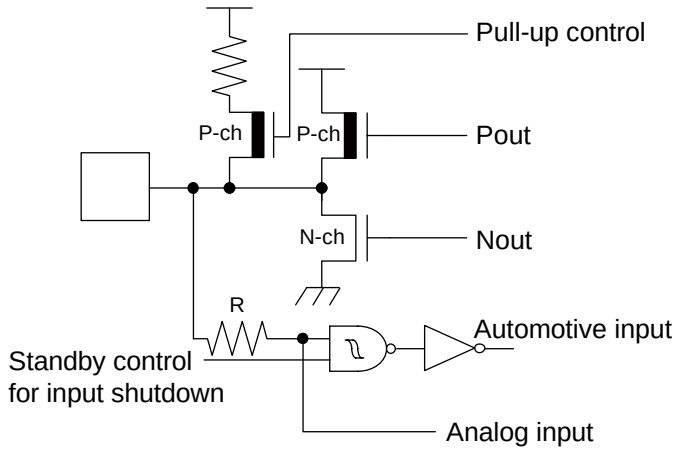
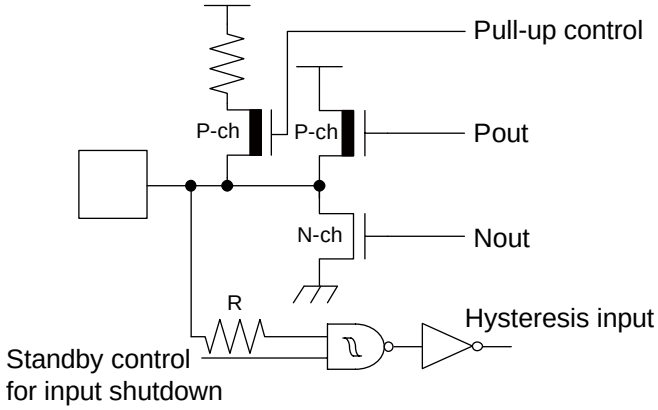
| Features | | CY96610 | Remark |
|---|---|---|---|
| Product Type | | Flash Memory Product | |
| Subclock | | Subclock can be set by software | |
| Dual Operation Flash Memory | RAM | - | |
| 32.5KB + 32KB | 4KB | CY96F612R, CY96F612A | Product Options<br>R: MCU with CAN<br>A: MCU without CAN |
| 64.5KB + 32KB | 10KB | CY96F613R, CY96F613A | |
| 128.5KB + 32KB | 10KB | CY96F615R, CY96F615A | |
| Package | | LQFP-48<br>LQA048 | |
| DMA | | 2ch | |
| USART | | 3ch | LIN-USART 2/7/8 |
| | with automatic LIN-Header transmission/reception | Yes (only 1ch) | LIN-USART 2 |
| | with 16 byte RX- and TX-FIFO | No | |
| 8/10-bit A/D Converter | | 16ch | AN 0/1/3/4/6 to 10/<br>12/14/16/24/25/30/31 |
| | with Data Buffer | No | |
| | with Range Comparator | Yes | |
| | with Scan Disable | No | |
| | with ADC Pulse Detection | No | |
| 16-bit Reload Timer (RLT) | | 3ch | RLT 1/3/6 |
| 16-bit Free-Running Timer (FRT) | | 4ch | FRT 0 to 3<br>FRT 0 to 3 does not have external clock input pin |
| 16-bit Input Capture Unit (ICU) | | 7ch<br>(3 channels for LIN-USART) | ICU 0/1/4 to 6/9/10<br>(ICU 6/9/10 for LIN-USART) |
| 16-bit Output Compare Unit (OCU) | | 5ch | OCU 0/1/4/6/7<br>(OCU 4 for FRT clear) |
| 8/16-bit Programmable Pulse Generator (PPG) | | 8ch (16-bit) / 16ch (8-bit) | PPG 0/1/3/4/6/7/12/14 |
| | with Timing point capture | Yes | |
| | with Start delay | No | |
| | with Ramp | No | |
| Quadrature Position/Revolution Counter (QPRC) | | 2ch | QPRC 0/1 |
| CAN Interface | | 1ch | CAN 2<br>32 Message Buffers |
| External Interrupts (INT) | | 11ch | INT 0/2/3/4/7 to 13 |
| Non-Maskable Interrupt (NMI) | | 1ch | |
| Real Time Clock (RTC) | | 1ch | |
| I/O Ports | | 35 (Dual clock mode)<br>37 (Single clock mode) | |
| Clock Calibration Unit (CAL) | | 1ch | |
| Clock Output Function | | 2ch | |
| Low Voltage Detection Function | | Yes | Low voltage detection function can be disabled by software |
| Hardware Watchdog Timer | | Yes | |
| On-chip RC-oscillator | | Yes | |
| On-chip Debugger | | Yes | |

***Note:***

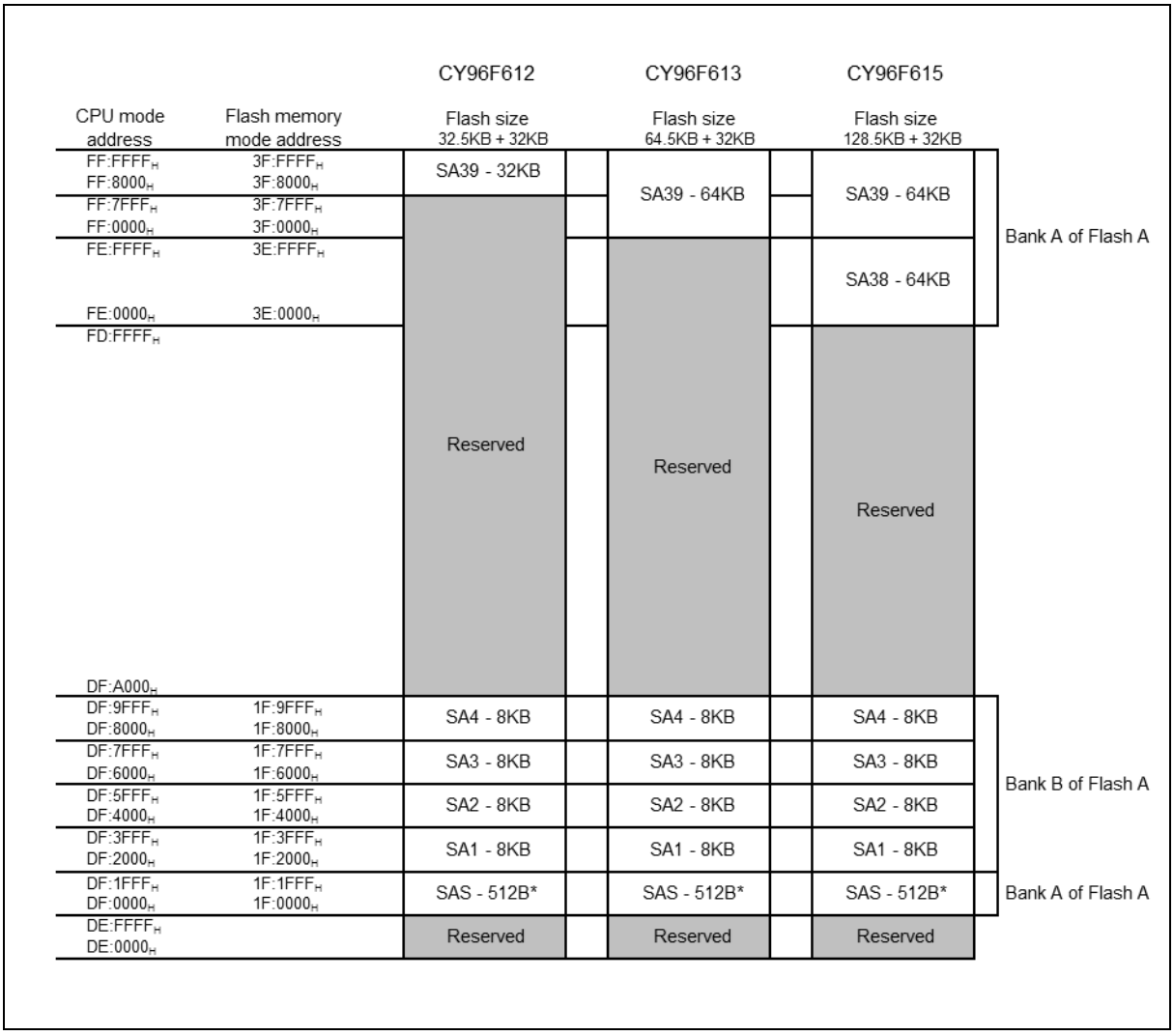
- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

| Pin Name | Feature | Description |
|---|---|---|
| ZINn | QPRC | Quadrature Position/Revolution Counter Unit n input pin |

| Type | Circuit | Remarks |
|---|---|---|
| B |  | Low-speed oscillation circuit shared with GPIO functionality:<br>■ Feedback resistor = approx. 5.0MΩ<br>■ GPIO functionality selectable (CMOS level output ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA), Automotive input with input shutdown function and programmable pull-up resistor) |

| Type | Circuit | Remarks |
|---|---|---|
| I |  | ■ CMOS level output<br>■ ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>■ CMOS hysteresis input with input shutdown function<br>■ Programmable pull-up resistor<br>■ Analog input |
| K |  | ■ CMOS level output<br>■ ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>■ Automotive input with input shutdown function<br>■ Programmable pull-up resistor<br>■ Analog input |
| M |  | ■ CMOS level output<br>■ ($I_{OL}$ = 4mA, $I_{OH}$ = -4mA)<br>■ CMOS hysteresis input with input shutdown function<br>■ Programmable pull-up resistor |

## 9. User ROM Memory Map for Flash Devices




*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for $E^2$PROM emulation.

| Vector Number | Offset in Vector Table | Vector Name | Cleared by DMA | Index in ICR to Program | Description |
|---|---|---|---|---|---|
| 81 | $2B8_H$ | OCU4 | Yes | 81 | Output Compare Unit 4 |
| 82 | $2B4_H$ | - | - | 82 | Reserved |
| 83 | $2B0_H$ | OCU6 | Yes | 83 | Output Compare Unit 6 |
| 84 | $2AC_H$ | OCU7 | Yes | 84 | Output Compare Unit 7 |
| 85 | $2A8_H$ | - | - | 85 | Reserved |
| 86 | $2A4_H$ | - | - | 86 | Reserved |
| 87 | $2A0_H$ | - | - | 87 | Reserved |
| 88 | $29C_H$ | - | - | 88 | Reserved |
| 89 | $298_H$ | FRT0 | Yes | 89 | Free-Running Timer 0 |
| 90 | $294_H$ | FRT1 | Yes | 90 | Free-Running Timer 1 |
| 91 | $290_H$ | FRT2 | Yes | 91 | Free-Running Timer 2 |
| 92 | $28C_H$ | FRT3 | Yes | 92 | Free-Running Timer 3 |
| 93 | $288_H$ | RTC0 | No | 93 | Real Time Clock |
| 94 | $284_H$ | CAL0 | No | 94 | Clock Calibration Unit |
| 95 | $280_H$ | - | - | 95 | Reserved |
| 96 | $27C_H$ | - | - | 96 | Reserved |
| 97 | $278_H$ | - | - | 97 | Reserved |
| 98 | $274_H$ | ADC0 | Yes | 98 | A/D Converter 0 |
| 99 | $270_H$ | - | - | 99 | Reserved |
| 100 | $26C_H$ | - | - | 100 | Reserved |
| 101 | $268_H$ | - | - | 101 | Reserved |
| 102 | $264_H$ | - | - | 102 | Reserved |
| 103 | $260_H$ | - | - | 103 | Reserved |
| 104 | $25C_H$ | - | - | 104 | Reserved |
| 105 | $258_H$ | LINR2 | Yes | 105 | LIN USART 2 RX |
| 106 | $254_H$ | LINT2 | Yes | 106 | LIN USART 2 TX |
| 107 | $250_H$ | - | - | 107 | Reserved |
| 108 | $24C_H$ | - | - | 108 | Reserved |
| 109 | $248_H$ | - | - | 109 | Reserved |
| 110 | $244_H$ | - | - | 110 | Reserved |
| 111 | $240_H$ | - | - | 111 | Reserved |
| 112 | $23C_H$ | - | - | 112 | Reserved |
| 113 | $238_H$ | - | - | 113 | Reserved |
| 114 | $234_H$ | - | - | 114 | Reserved |
| 115 | $230_H$ | LINR7 | Yes | 115 | LIN USART 7 RX |
| 116 | $22C_H$ | LINT7 | Yes | 116 | LIN USART 7 TX |
| 117 | $228_H$ | LINR8 | Yes | 117 | LIN USART 8 RX |
| 118 | $224_H$ | LINT8 | Yes | 118 | LIN USART 8 TX |
| 119 | $220_H$ | - | - | 119 | Reserved |
| 120 | $21C_H$ | - | - | 120 | Reserved |
| 121 | $218_H$ | - | - | 121 | Reserved |

***CAUTION:***
*The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:*

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

■ Observance of Safety Regulations and Standards
Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design
Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
***CAUTION:***
*Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.*

## 12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

# 13. Handling Devices

**Special Care is Required for the Following when Handling the Device:**

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

## 13.1 Latch-Up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

## 13.2 Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

## 13.3 External Clock Usage

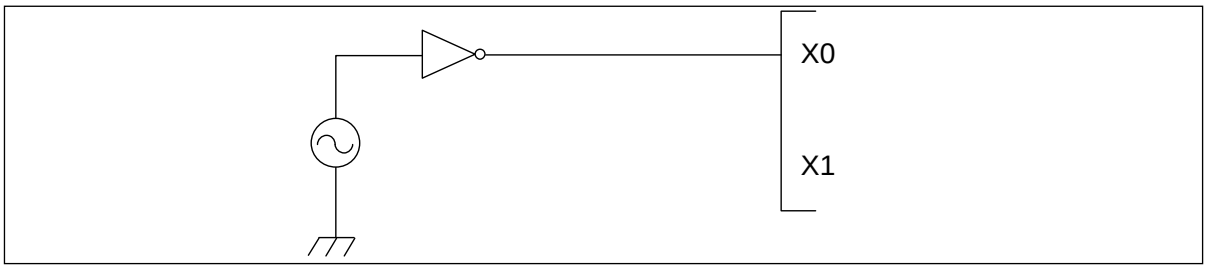
The permitted frequency range of an external clock depends on the oscillator type and configuration.

See

AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

### 13.3.1 *Single Phase External Clock for Main Oscillator*

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.

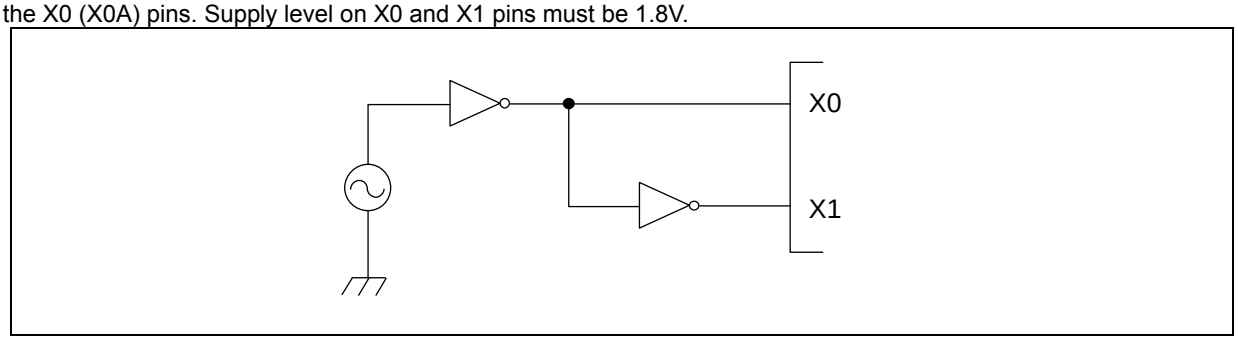



### 13.3.2 *Single Phase External Clock for Sub Oscillator*

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

### 13.3.3 *Opposite Phase External Clock*

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.




## 13.4 Notes on PLL Clock Mode Operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

## 13.5 Power Supply Pins (Vcc/Vss)

It is required that all $V_{CC}$-level as well as all $V_{SS}$-level power supply pins are at the same potential. If there is more than one $V_{CC}$ or $V_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

## 13.6 Crystal Oscillator and ceramic resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

### 13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply ($AV_{CC}$, AVRH) and analog inputs (ANn) on after turning the digital power supply ($V_{CC}$) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed $AV_{CC}$ Input voltage for ports shared with analog input ports also must not exceed $AV_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable)

### 13.8 Pin Handling when Not Using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC}$ = $V_{CC}$ $AV_{SS}$ = AVRH = $V_{SS}$.

### 13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

### 13.10 Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the $V_{CC}$ power supply voltage, a malfunction may occur. The $V_{CC}$ power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that $V_{CC}$ ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard $V_{CC}$ power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

### 13.11 Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

### 13.12 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

## 14.2 Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 2.7 | - | 5.5 | V | |
| | | 2.0 | - | 5.5 | V | Maintains RAM data in stop mode |
| Smoothing capacitor at C pin | $C_S$ | 0.5 | 1.0 to 3.9 | 4.7 | µF | 1.0µF (Allowance within ± 50%)<br>3.9µF (Allowance within ± 20%)<br>Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at $V_{CC}$ must use the one of a capacity value that is larger than $C_S$. |

***WARNING:***

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 14.3 DC Characteristics

### 14.3.1 *Current Rating*

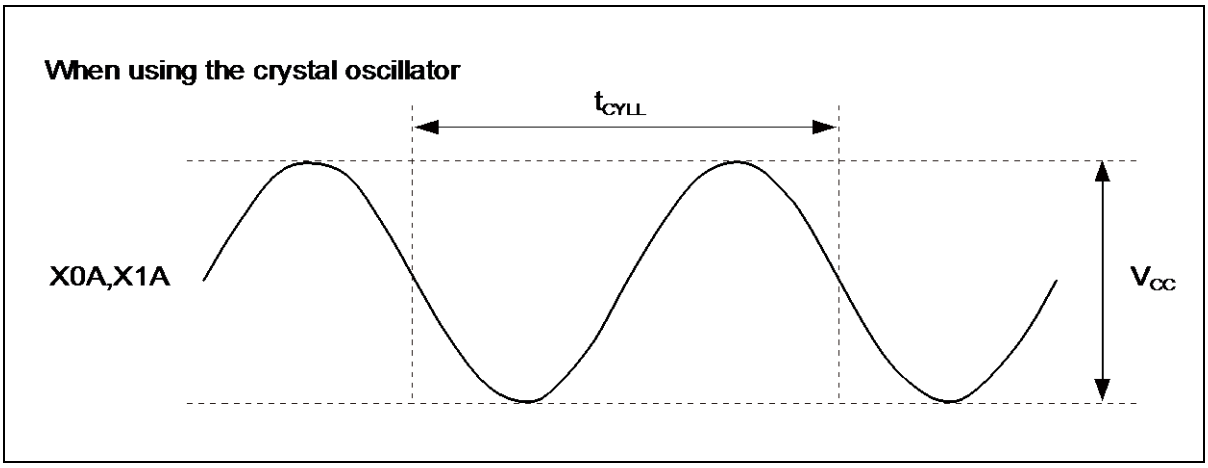
($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

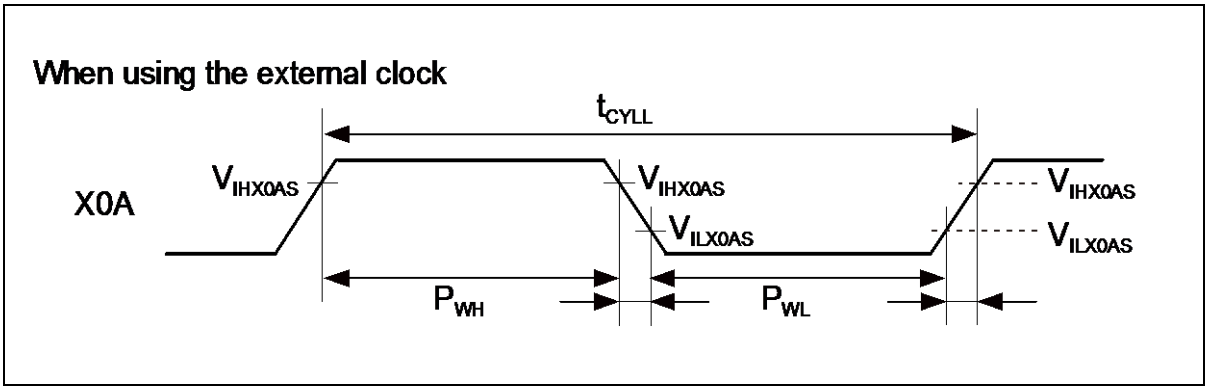
| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current in Run modes[1] | $I_{CCPLL}$ | Vcc | PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz<br>Flash 0 wait<br>(CLKRC and CLKSC stopped) | - | 25 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 34 | mA | $T_A$ = +105°C |
| | | | | - | - | 35 | mA | $T_A$ = +125°C |
| | $I_{CCMAIN}$ | | Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz<br>Flash 0 wait<br>(CLKPLL, CLKSC and CLKRC stopped) | - | 3.5 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 7.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 8.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCH}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 1.7 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 5.5 | mA | $T_A$ = +105°C |
| | | | | - | - | 6.5 | mA | $T_A$ = +125°C |
| | $I_{CCRCL}$ | | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKSC stopped) | - | 0.15 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3.2 | mA | $T_A$ = +105°C |
| | | | | - | - | 4.2 | mA | $T_A$ = +125°C |
| | $I_{CCSUB}$ | | Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz<br>Flash 0 wait<br>(CLKMC, CLKPLL and CLKRC stopped) | - | 0.1 | - | mA | $T_A$ = +25°C |
| | | | | - | - | 3 | mA | $T_A$ = +105°C |
| | | | | - | - | 4 | mA | $T_A$ = +125°C |

### 14.4.2 *Sub Clock Input Characteristics*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input frequency | $f_{CL}$ | X0A, X1A | - | - | 32.768 | - | kHz | When using an oscillation circuit |
| | | | - | - | - | 100 | kHz | When using an opposite phase external clock |
| | | X0A | - | - | - | 50 | kHz | When using a single phase external clock |
| Input clock cycle | $t_{CYLL}$ | - | - | 10 | - | - | µs | |
| Input clock pulse width | - | - | $P_{WH}/t_{CYLL}$, $P_{WL}/t_{CYLL}$ | 30 | - | 70 | % | |



### 14.4.3 *Built-in RC Oscillation Characteristics*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Clock frequency | $f_{RC}$ | 50 | 100 | 200 | kHz | When using slow frequency of RC oscillator |
| | | 1 | 2 | 4 | MHz | When using fast frequency of RC oscillator |
| RC clock stabilization time | $t_{RCSTAB}$ | 80 | 160 | 320 | µs | When using slow frequency of RC oscillator (16 RC clock cycles) |
| | | 64 | 128 | 256 | µs | When using fast frequency of RC oscillator (256 RC clock cycles) |

### 14.4.4 *Internal Clock Timing*

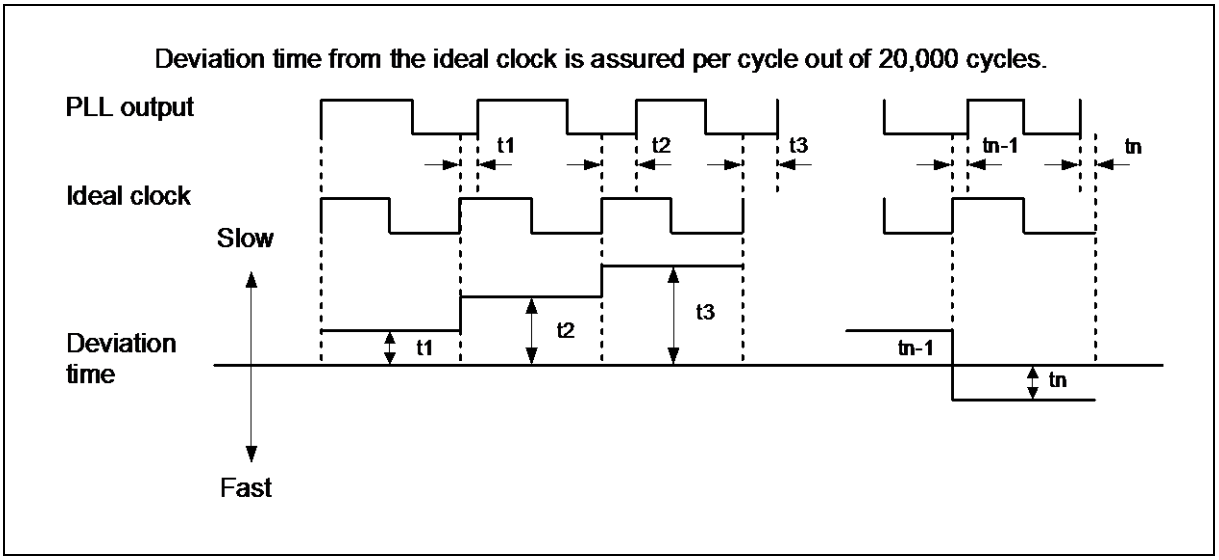
($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Internal System clock frequency (CLKS1 and CLKS2) | $f_{CLKS1}$, $f_{CLKS2}$ | - | 54 | MHz |
| Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1) | $f_{CLKB}$, $f_{CLKP1}$ | - | 32 | MHz |
| Internal peripheral clock frequency (CLKP2) | $f_{CLKP2}$ | - | 32 | MHz |

### 14.4.5 *Operating Conditions of PLL*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

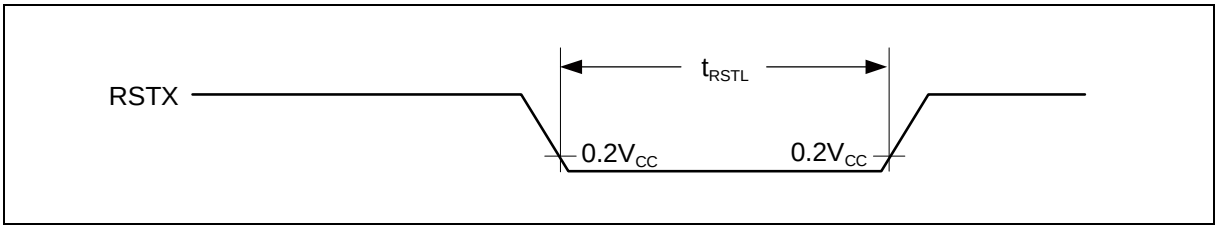
| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time | $t_{LOCK}$ | 1 | - | 4 | ms | For CLKMC = 4MHz |
| PLL input clock frequency | $f_{PLLI}$ | 4 | - | 8 | MHz | |
| PLL oscillation clock frequency | $f_{CLKVCO}$ | 56 | - | 108 | MHz | Permitted VCO output frequency of PLL (CLKVCO) |
| PLL phase jitter | $t_{PSKEW}$ | -5 | - | +5 | ns | For CLKMC (PLL input clock) ≥ 4MHz |




### 14.4.6 *Reset Input*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

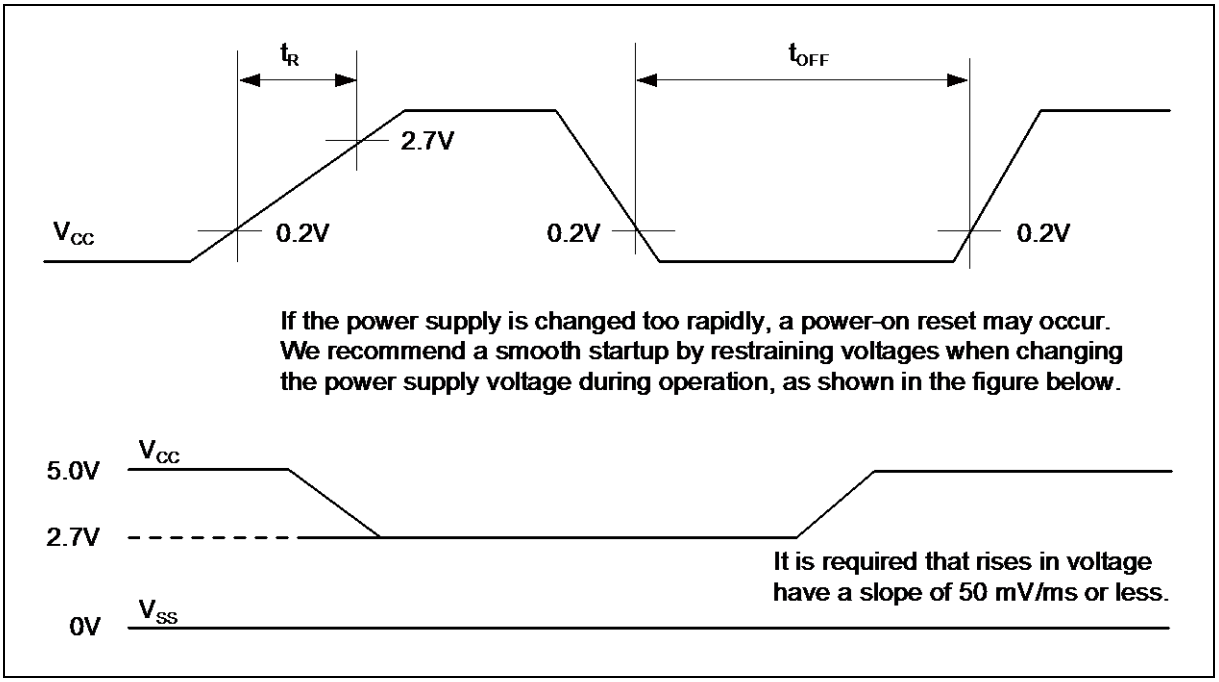
| Parameter | Symbol | Pin Name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Reset input time | $t_{RSTL}$ | RSTX | 10 | - | µs |
| Rejection of reset input time | | | 1 | - | µs |



### 14.4.7 *Power-on Reset Timing*

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

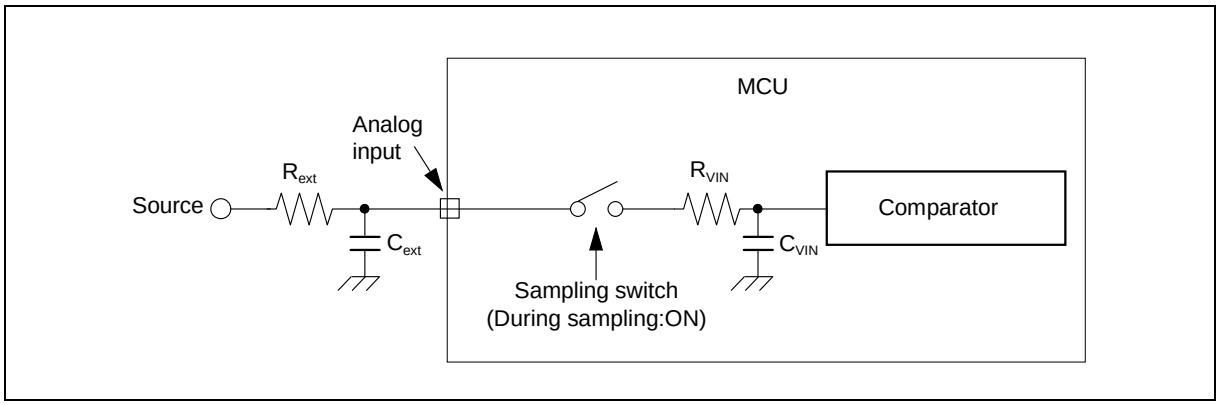
| Parameter | Symbol | Pin Name | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power on rise time | $t_R$ | Vcc | 0.05 | - | 30 | ms |
| Power off time | $t_{OFF}$ | Vcc | 1 | - | - | ms |



### 14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance $R_{ext}$, the board capacitance of the A/D converter input pin $C_{ext}$ and the $AV_{CC}$ voltage level. The following replacement model can be used for the calculation:




$R_{ext}$: External driving impedance

$C_{ext}$: Capacitance of PCB at A/D converter input

$C_{VIN}$: Analog input capacity (I/O, analog switch and ADC are contained)

$R_{VIN}$: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

### 14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.

## 14.7 Flash Memory Write/Erase Characteristics

($V_{CC}$ = $AV_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $T_A$ = - 40°C to + 125°C)

| Parameter | | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Sector erase time | Large Sector | $T_A$ ≤ + 105°C | - | 1.6 | 7.5 | s | Includes write time prior to internal erase. |
| | Small Sector | - | - | 0.4 | 2.1 | s | |
| | Security Sector | - | - | 0.31 | 1.65 | s | |
| Word (16-bit) write time | Large Sector | $T_A$ ≤ + 105°C | - | 25 | 400 | µs | Not including system-level overheadtime. |
| | Small Sector | - | - | 25 | 400 | µs | |
| Chip erase time | | $T_A$ ≤ + 105°C | - | 5.11 | 25.05 | s | Includes write time prior to internal erase. |

***Note:***

*While the Flash memory is written or erased, shutdown of the external power ($V_{CC}$) is prohibited. In the application system where the external power ($V_{CC}$) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.*

*To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage ($V_{DLX}$)[*1].*

Write/Erase cycles and data hold time

| Write/Erase Cycles (Cycle) | Data Hold Time (Year) |
|---|---|
| 1,000 | 20 [2] |
| 10,000 | 10 [2] |
| 100,000 | 5 [2] |

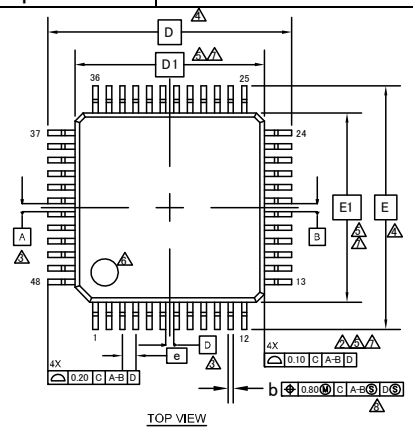
[1]:See "14.6 Low Voltage Detection Function Characteristics".

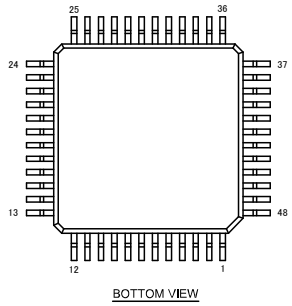
[2]:This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85˚c).

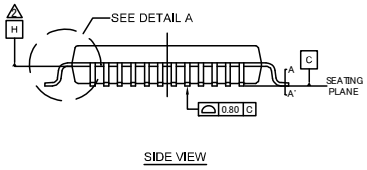
# 17. Package Dimension

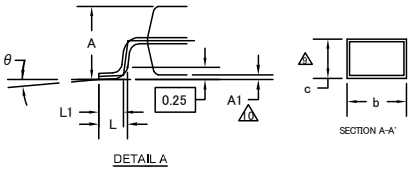
## LQA048, 48 Lead Plastic Low Profile Quad Flat Package

| Package Type | Package Code |
|---|---|
| LQFP 48pin | LQA048 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

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