Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f615abpmc-gte1

Contents

Features **1**
1. Product Lineup **6**
2. Block Diagram **7**
3. Pin Assignment **8**
4. Pin Description **9**
5. Pin Circuit Type **11**
6. I/O Circuit Type **13**
7. Memory Map **18**
8. RAMstart Addresses **19**
9. User ROM Memory Map for Flash Devices **20**
10. Serial Programming Communication Interface **21**
11. Interrupt Vector Table **22**
12. Handling Precautions **26**
12.1 Precautions for Product Design 26
12.2 Precautions for Package Mounting 27
12.3 Precautions for Use Environment 29
13. Handling Devices **30**
13.1 Latch-Up Prevention 30
13.2 Unused Pins Handling 30
13.3 External Clock Usage 30
13.3.1 Single Phase External Clock for Main Oscillator 31
13.3.2 Single Phase External Clock for Sub Oscillator 31
13.3.3 Opposite Phase External Clock 31
13.4 Notes on PLL Clock Mode Operation 31
13.5 Power Supply Pins (Vcc/Vss) 31
13.6 Crystal Oscillator and ceramic resonator Circuit 31
13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs 32
13.8 Pin Handling when Not Using the A/D Converter 32
13.9 Notes on Power-on 32
13.10 Stabilization of Power Supply Voltage 32
13.11 Serial Communication 32
13.12 Mode Pin (MD) 32
14. Electrical Characteristics **33**
14.1 Absolute Maximum Ratings 33
14.2 Recommended Operating Conditions 35
14.3 DC Characteristics 36
14.3.1 Current Rating 36
14.3.2 Pin Characteristics 39
14.4 AC Characteristics 40
14.4.1 Main Clock Input Characteristics 40
14.4.2 Sub Clock Input Characteristics 41
14.4.3 Built-in RC Oscillation Characteristics 42
14.4.4 Internal Clock Timing 42
14.4.5 Operating Conditions of PLL 43
14.4.6 Reset Input 43
14.4.7 Power-on Reset Timing 44
14.4.8 USART Timing 45
14.4.9 External Input Timing 47
14.5 A/D Converter 48
14.5.1 Electrical Characteristics for the A/D Converter 48

14.5.2 Accuracy and Setting of the A/D Converter Sampling Time 49
14.5.3 Definition of A/D Converter Terms 49
14.6 Low Voltage Detection Function Characteristics 52
14.7 Flash Memory Write/Erase Characteristics 54
15. Example Characteristics 55
16. Ordering Information 58
17. Package Dimension 59
18. Major Changes 60
Document History 63
Sales, Solutions, and Legal Information 64

1. Product Lineup

Features		CY96610	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
32.5KB + 32KB	4KB	CY96F612R, CY96F612A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB	10KB	CY96F613R, CY96F613A	
128.5KB + 32KB	10KB	CY96F615R, CY96F615A	
Package		LQFP-48 LQA048	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO	No	
8/10-bit A/D Converter		16ch	AN 0/1/3/4/6 to 10/ 12/14/16/24/25/30/31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	No	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 0 to 3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		7ch (3 channels for LIN-USART)	ICU 0/1/4 to 6/9/10 (ICU 6/9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)		5ch	OCU 0/1/4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INT)		11ch	INT 0/2/3/4/7 to 13
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		35 (Dual clock mode) 37 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.*

5. Pin Circuit Type

Pin No.	I/O Circuit Type*	Pin Name
1	Supply	AVss
2	G	AVRH
3	K	P06_3 / AN3 / PPG3
4	K	P06_4 / AN4 / PPG4
5	K	P06_6 / AN6 / PPG6
6	K	P06_7 / AN7 / PPG7
7	I	P05_0 / AN8 / SIN2 / INT3_R1
8	K	P05_1 / AN9 / SOT2
9	I	P05_2 / AN10 / SCK2
10	K	P05_4 / AN12 / TOT3 / INT2_R
11	K	P05_6 / AN14 / INT4_R
12	K	P07_0 / AN16 / INT0 / NMI
13	B	P04_0 / X0A
14	B	P04_1 / X1A
15	C	MD
16	H	P17_0
17	O	DEBUG I/F
18	M	P00_0 / INT8 / SCK7_R / PPG0_B
19	H	P00_1 / INT9 / SOT7_R / PPG1_B
20	M	P00_2 / INT10 / SIN7_R
21	H	P00_4 / INT12 / SOT8_R / PPG12_B
22	M	P00_5 / INT13 / SIN8_R / PPG14_B
23	M	P00_3 / INT11 / SCK8_R / PPG3_B
24	H	P01_0 / TIN1 / CKOT1 / OUT0_R
25	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
26	H	P01_4 / PPG4_B
27	M	P01_5 / SIN2_R / INT7_R
28	H	P01_6 / SOT2_R / PPG6_B
29	M	P01_7 / SCK2_R / PPG7_B
30	H	P02_0 / PPG12 / CKOT1_R
31	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
32	H	P02_4 / AIN0 / IN0 / TTG0

Pin No.	I/O Circuit Type*	Pin Name
33	C	RSTX
34	A	X1
35	A	X0
36	Supply	Vss
37	Supply	Vcc
38	F	C
39	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
40	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
41	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
42	M	P03_2 / INT10_R / RX2
43	H	P03_3 / TX2
44	K	P03_6 / ZIN1 / OUT6 / AN30
45	K	P03_7 / OUT7 / AN31
46	K	P06_0 / AN0 / PPG0
47	K	P06_1 / AN1 / PPG1
48	Supply	AVcc

*: See I/O Circuit Type" for details on the I/O circuit types.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96610		
Pin Number	**USART Number**	**Normal Function**
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
81	$2B8_H$	OCU4	Yes	81	Output Compare Unit 4
82	$2B4_H$	-	-	82	Reserved
83	$2B0_H$	OCU6	Yes	83	Output Compare Unit 6
84	$2AC_H$	OCU7	Yes	84	Output Compare Unit 7
85	$2A8_H$	-	-	85	Reserved
86	$2A4_H$	-	-	86	Reserved
87	$2A0_H$	-	-	87	Reserved
88	$29C_H$	-	-	88	Reserved
89	298_H	FRT0	Yes	89	Free-Running Timer 0
90	294_H	FRT1	Yes	90	Free-Running Timer 1
91	290_H	FRT2	Yes	91	Free-Running Timer 2
92	$28C_H$	FRT3	Yes	92	Free-Running Timer 3
93	288_H	RTC0	No	93	Real Time Clock
94	284_H	CAL0	No	94	Clock Calibration Unit
95	280_H	-	-	95	Reserved
96	$27C_H$	-	-	96	Reserved
97	278_H	-	-	97	Reserved
98	274_H	ADC0	Yes	98	A/D Converter 0
99	270_H	-	-	99	Reserved
100	$26C_H$	-	-	100	Reserved
101	268_H	-	-	101	Reserved
102	264_H	-	-	102	Reserved
103	260_H	-	-	103	Reserved
104	$25C_H$	-	-	104	Reserved
105	258_H	LINR2	Yes	105	LIN USART 2 RX
106	254_H	LINT2	Yes	106	LIN USART 2 TX
107	250_H	-	-	107	Reserved
108	$24C_H$	-	-	108	Reserved
109	248_H	-	-	109	Reserved
110	244_H	-	-	110	Reserved
111	240_H	-	-	111	Reserved
112	$23C_H$	-	-	112	Reserved
113	238_H	-	-	113	Reserved
114	234_H	-	-	114	Reserved
115	230_H	LINR7	Yes	115	LIN USART 7 RX
116	$22C_H$	LINT7	Yes	116	LIN USART 7 TX
117	228_H	LINR8	Yes	117	LIN USART 8 RX
118	224_H	LINT8	Yes	118	LIN USART 8 TX
119	220_H	-	-	119	Reserved
120	$21C_H$	-	-	120	Reserved
121	218_H	-	-	121	Reserved

CAUTION:
The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

■ Observance of Safety Regulations and Standards
Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design
Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AVRH \geq AV_{SS}$
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	13	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	32	mA	
"L" level average overall output current	ΣI_{OLAV}	-	-	16	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-32	mA	
"H" level average overall output current	ΣI_{OHAV}	-	-	-16	mA	
Power consumption[5]	P_D	T_A= +125°C	-	284[6]	mW	
Operating ambient temperature	T_A	-	-40	+125[7]	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

[1]: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

[2]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

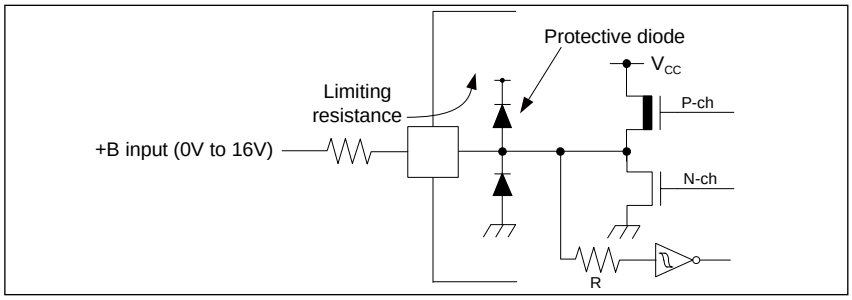
[3]: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

[4]:

- Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Sample recommended circuits:



[5]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

[6]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[7]: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105°C$.

WARNING:
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 *Current Rating*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
				-	-	35	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
				-	-	8.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
				-	-	6.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
				-	-	4.2	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

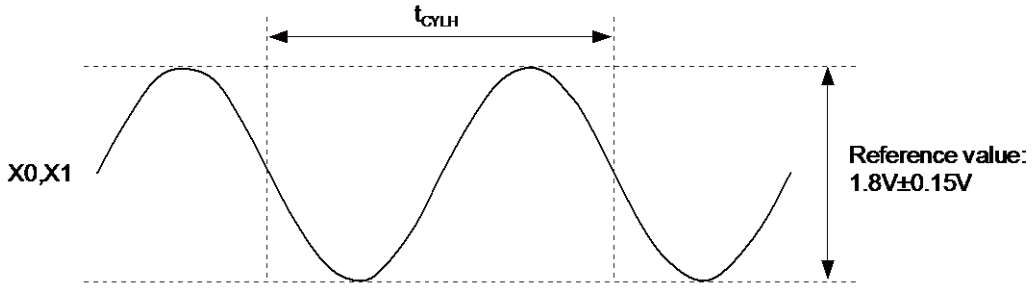
14.4 AC Characteristics

14.4.1 *Main Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

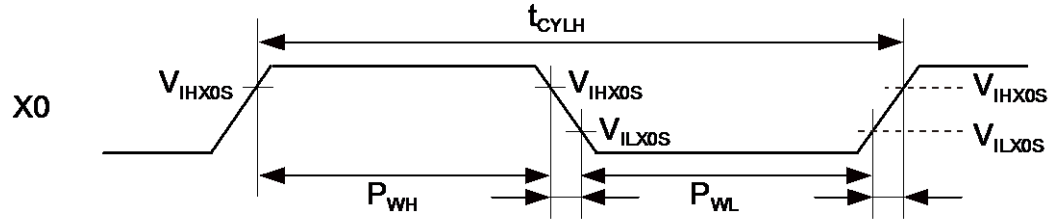
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

When using the crystal oscillator



The amplitude changes by resistance, capacity which added outside or the difference of the device.

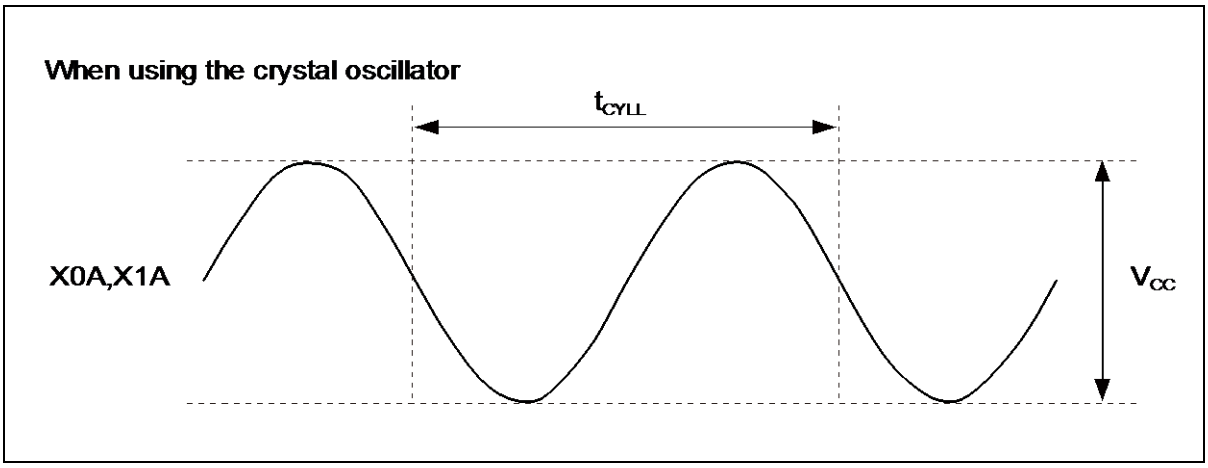
When using the external clock

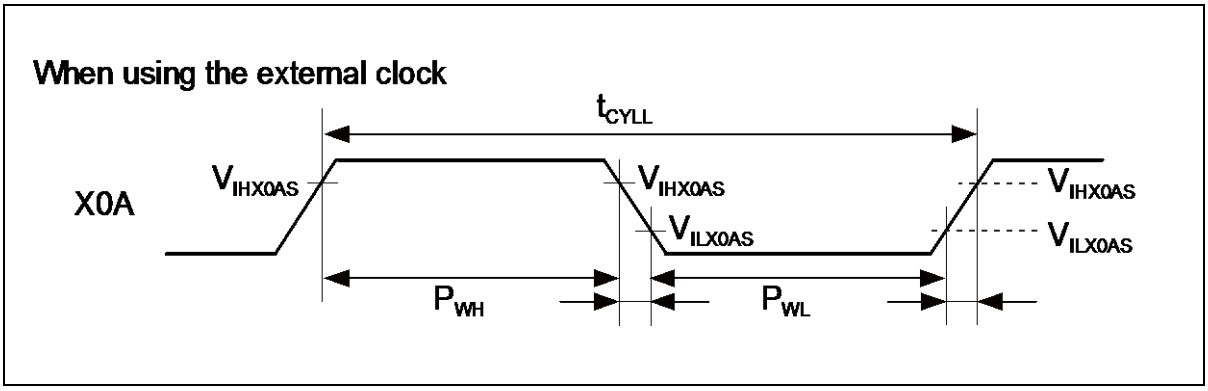


14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	

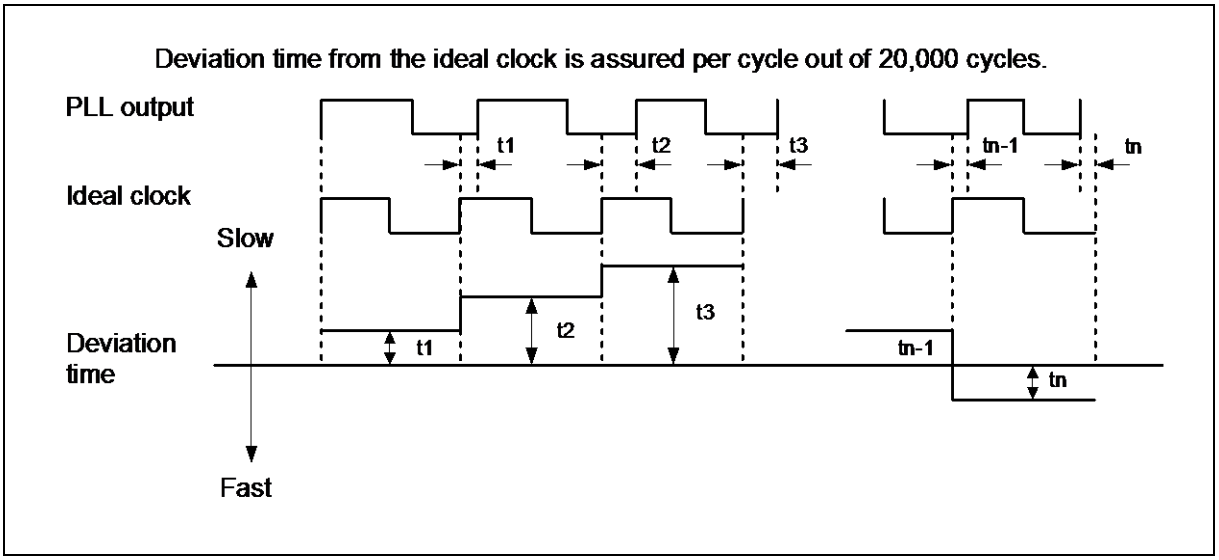




14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

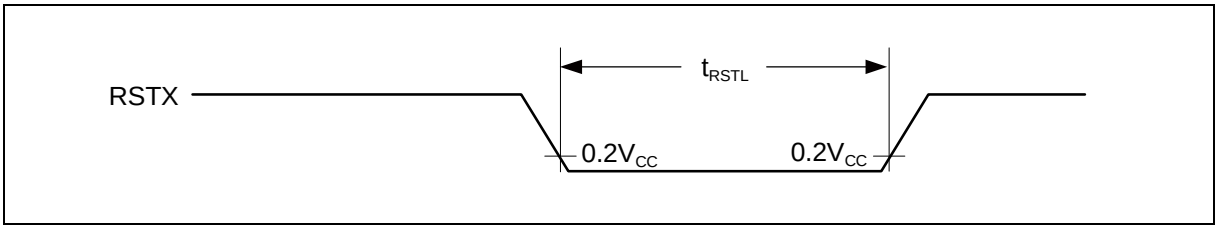
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

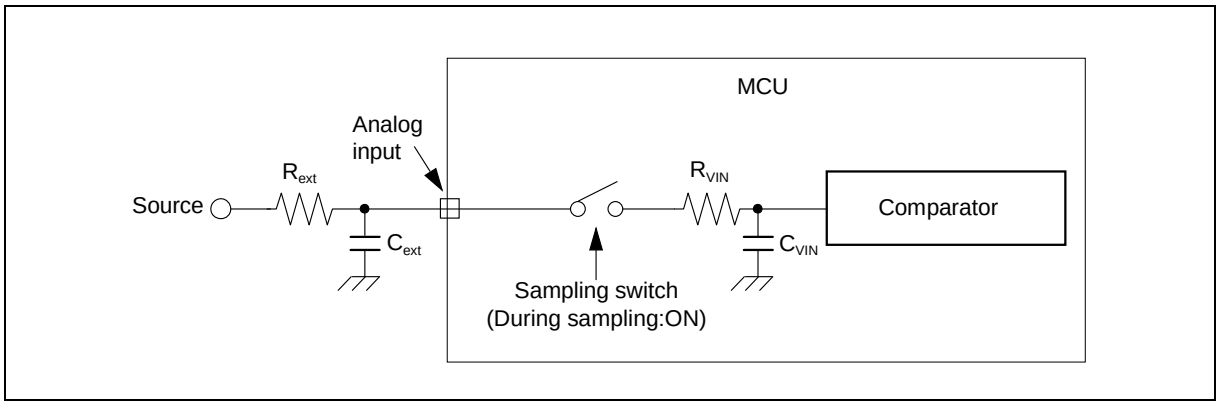
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

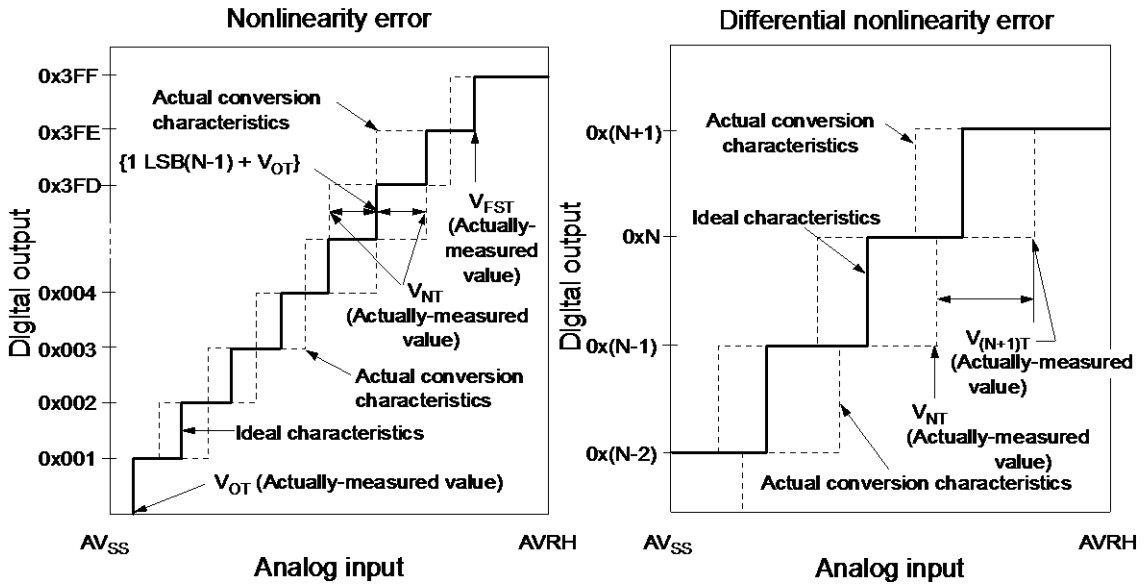
R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.



Nonlinearity error of digital output N = $\frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

Differential nonlinearity error of digital output N = $\frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

$1LSB = \frac{V_{FST} - V_{OT}}{1022}$

N : A/D converter digital output value.

V_O : Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.

V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	T_A ≤ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	T_A ≤ + 105°C	-	25	400	µs	Not including system-level overheadtime.
	Small Sector	-	-	25	400	µs	
Chip erase time		T_A ≤ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

*To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].*

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

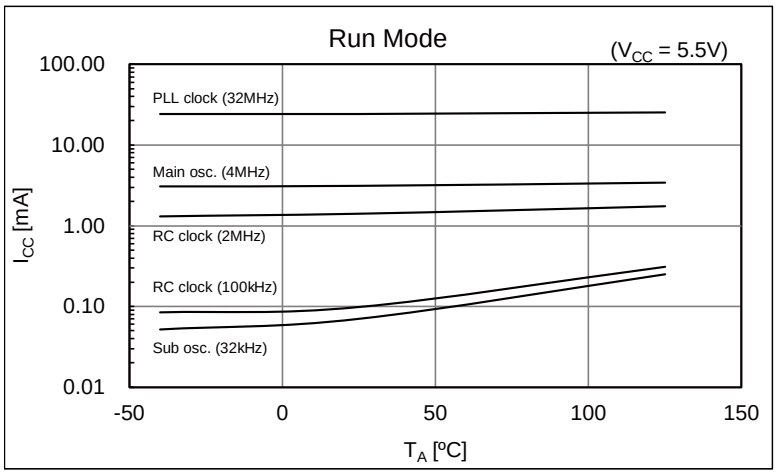
[1]:See "14.6 Low Voltage Detection Function Characteristics".

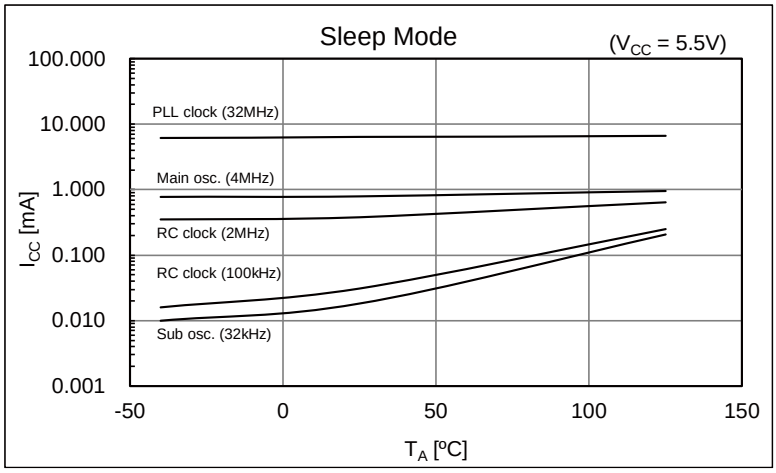
[2]:This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85˚c).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

CY96F615





Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support