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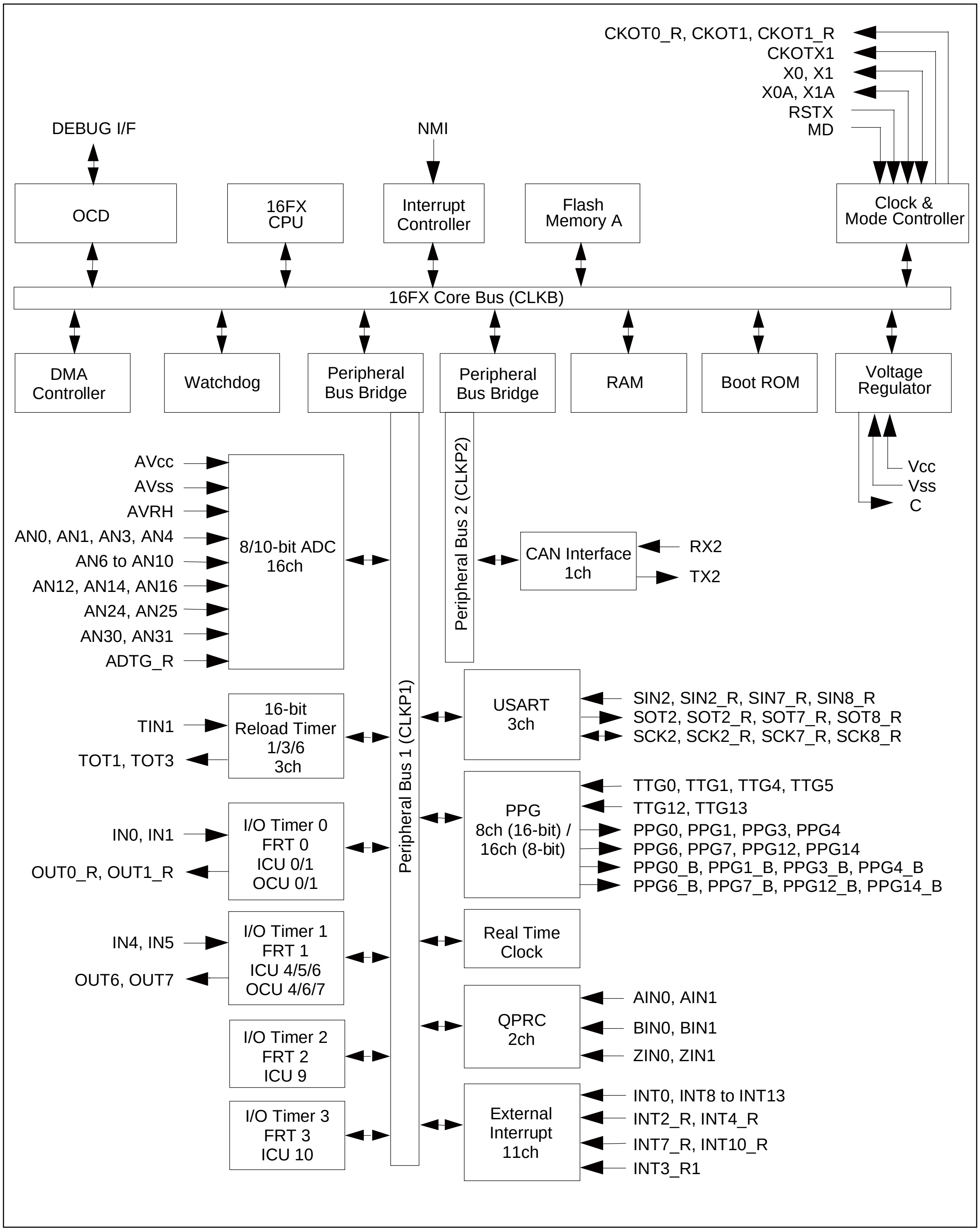
What is "Embedded - Microcontrollers"?

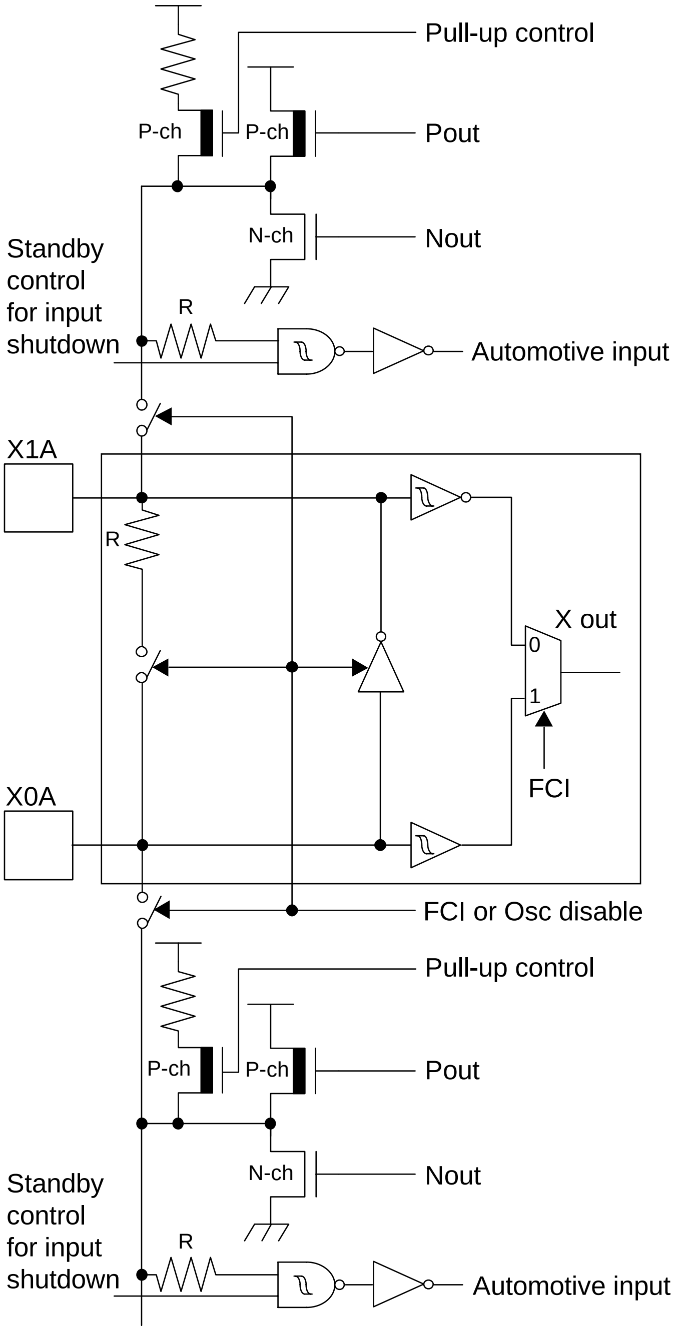
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

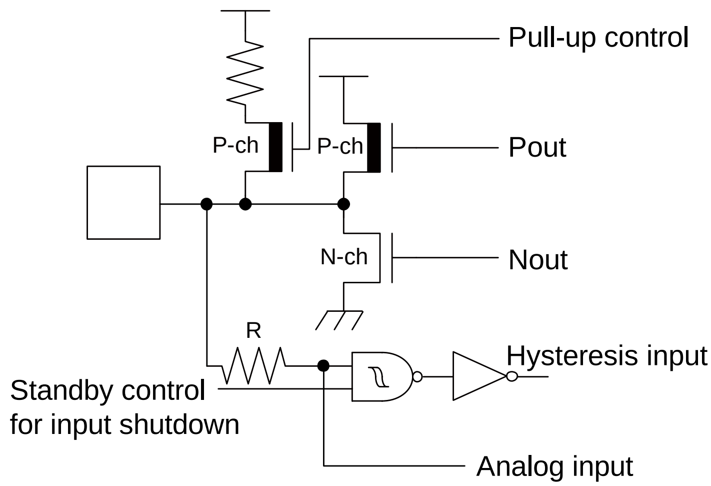
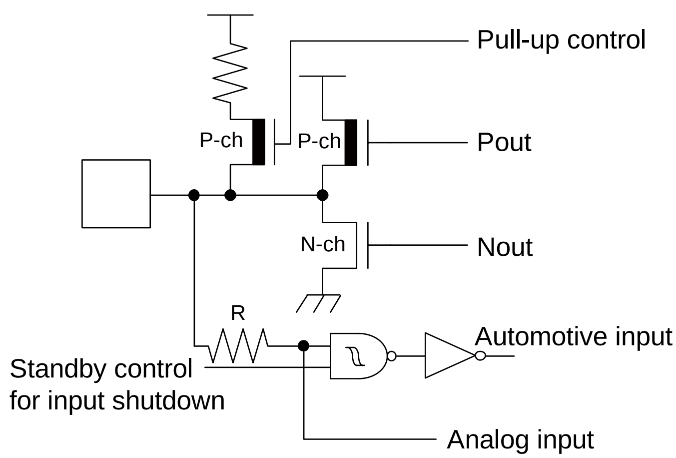
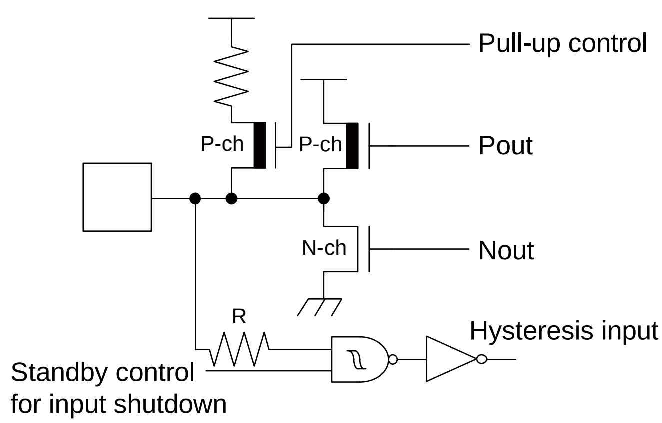
Applications of "Embedded - Microcontrollers"

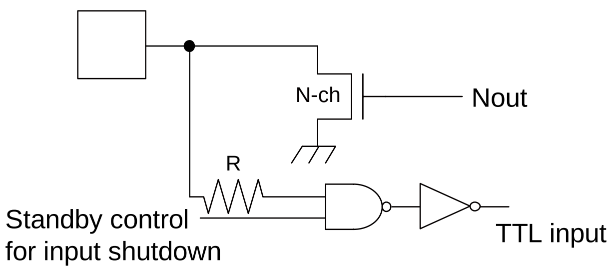
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f615rbpmc-gs-ujere2

2. Block Diagram

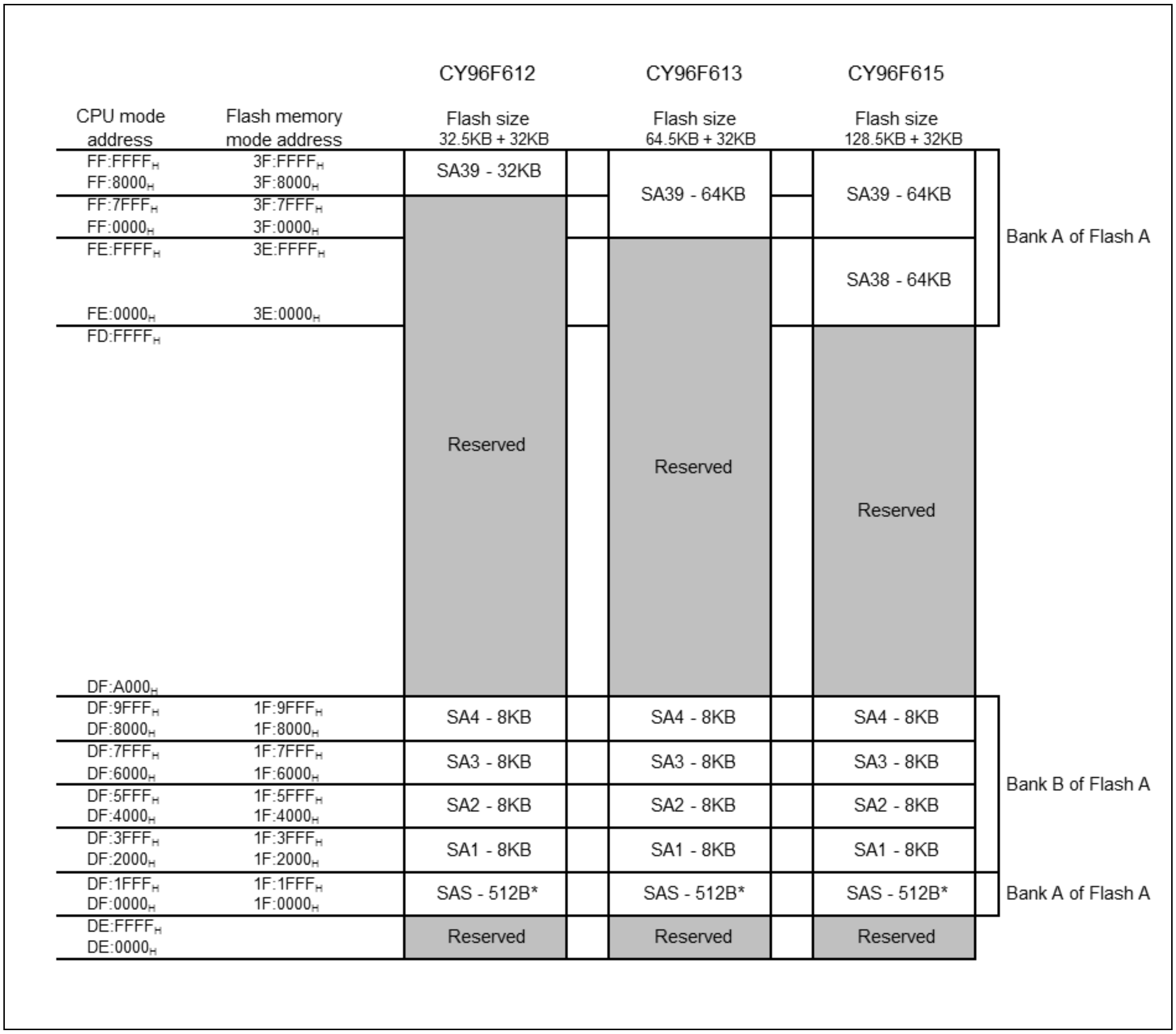


Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: ■ Feedback resistor = approx. 5.0MΩ ■ GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)

Type	Circuit	Remarks
I		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor ■ Analog input
K		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ Analog input
M		■ CMOS level output ■ (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor

Type	Circuit	Remarks
O		■ Open-drain I/O ■ Output 25mA, Vcc = 2.7V ■ TTL input

9. User ROM Memory Map for Flash Devices



*: Physical address area of SAS-512B is from DF:0000H to DF:01FFH.
Others (from DF:0200H to DF:1FFFH) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000H -DF:01FFH.
SAS can not be used for E^{2}PROM emulation.

CAUTION:
The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging
CAUTION:
When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking
Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity
Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

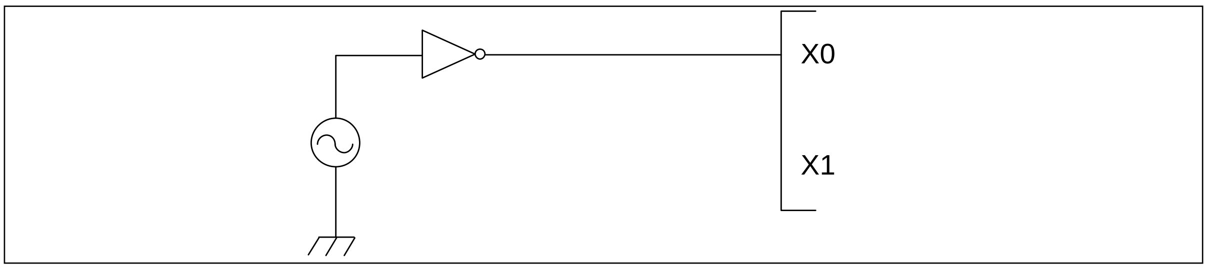
Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 *Single Phase External Clock for Main Oscillator*

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.

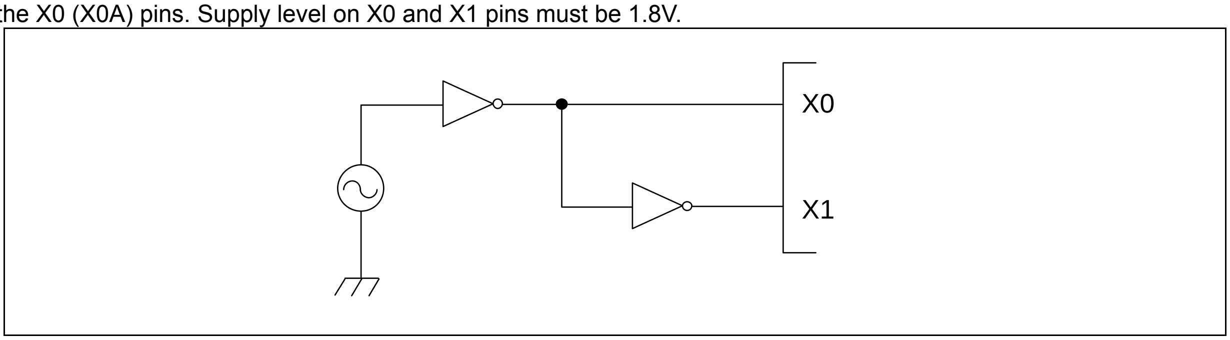


13.3.2 *Single Phase External Clock for Sub Oscillator*

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 *Opposite Phase External Clock*

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL Clock Mode Operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power Supply Pins (Vcc/Vss)

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

13.6 Crystal Oscillator and ceramic resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes[2]	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	μA	T_A = +25°C
				-	-	3165	μA	T_A = +105°C
				-	-	3975	μA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	μA	T_A = +25°C
				-	-	1085	μA	T_A = +105°C
				-	-	1930	μA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	μA	T_A = +25°C
				-	-	1025	μA	T_A = +105°C
				-	-	1840	μA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	μA	T_A = +25°C
				-	-	855	μA	T_A = +105°C
				-	-	1640	μA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	μA	T_A = +25°C
				-	-	830	μA	T_A = +105°C
				-	-	1620	μA	T_A = +125°C
Power supply current in Stop mode[3]	I_{CCH}	Vcc	-	-	20	55	μA	T_A = +25°C
				-	-	825	μA	T_A = +105°C
				-	-	1615	μA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	μA	
Power supply current for active Low Voltage detector[4]	I_{CCLVD}		Low voltage detector enabled	-	5	-	μA	T_A = +25°C
				-	-	12.5	μA	T_A = +125°C
Flash Write/ Erase current[5]	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

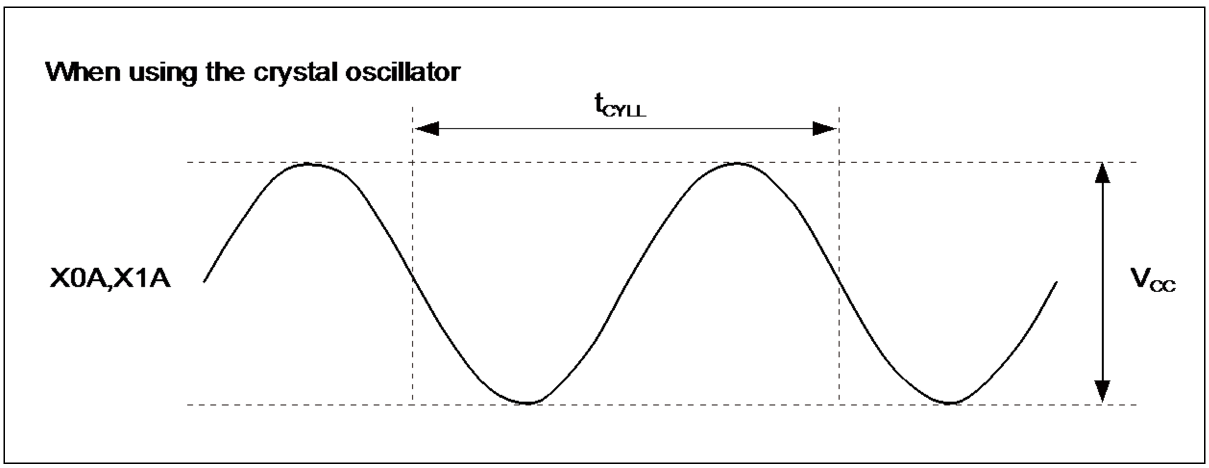
[4]: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

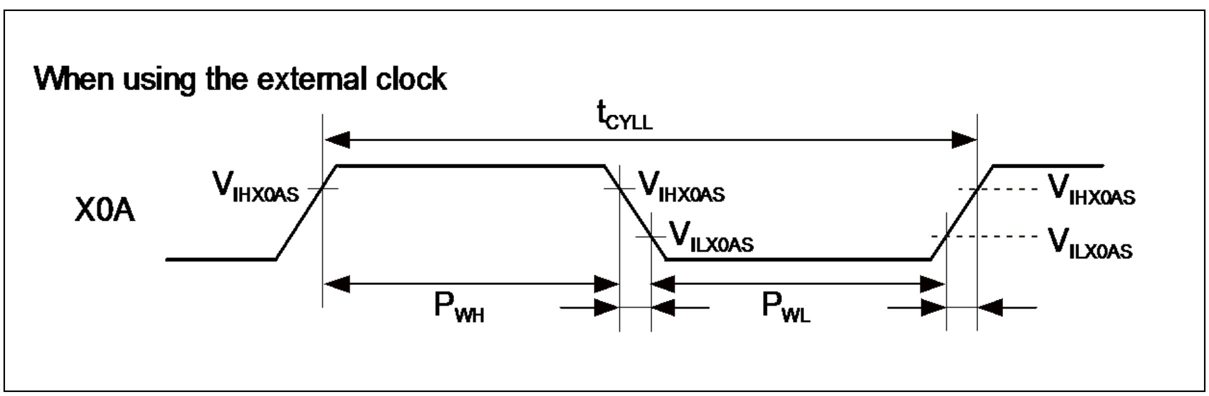
[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.3 *Built-in RC Oscillation Characteristics*

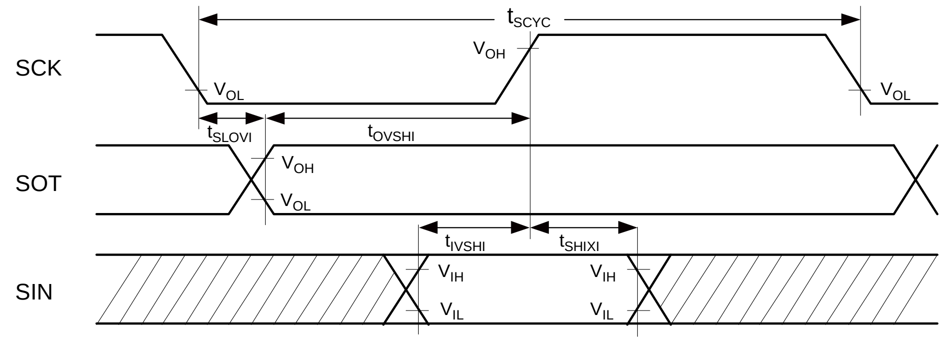
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

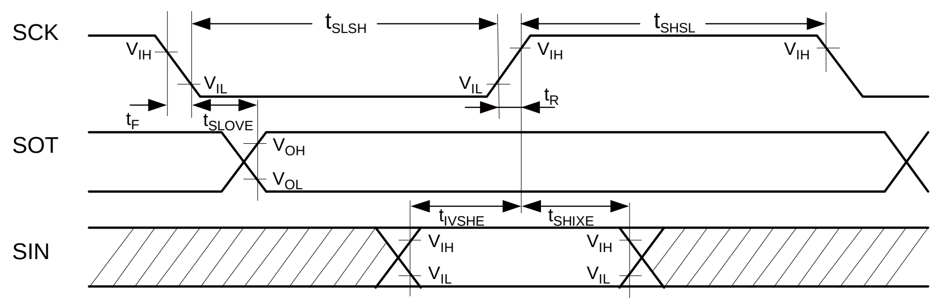
14.4.4 *Internal Clock Timing*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz



Internal shift clock mode



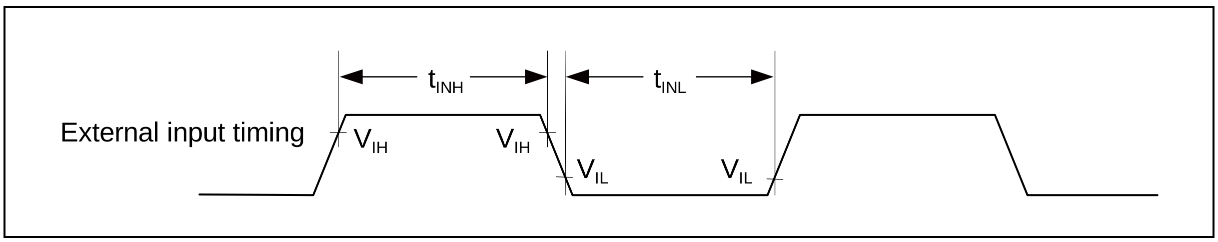
External shift clock mode

14.4.9 *External Input Timing*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}=1/f_{CLKP1})*	-	ns	General Purpose I/O
		ADTG_R				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		INn				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R, INTn_R1	200	-	ns	External Interrupt
		NMI				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



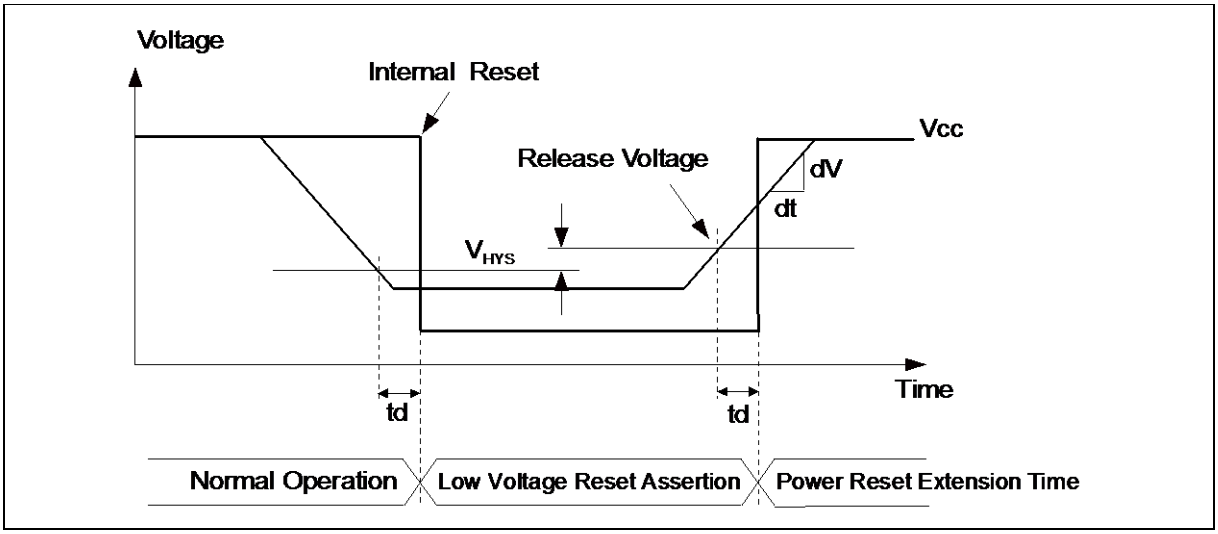
14.5 A/D Converter

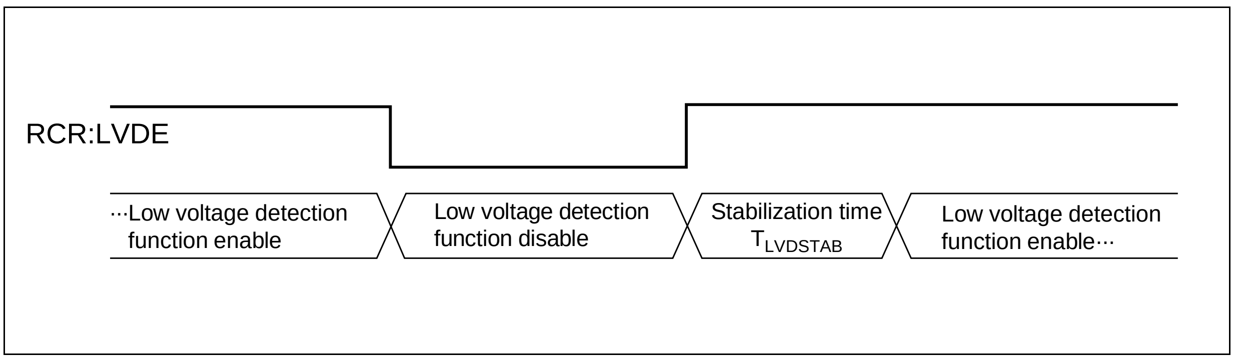
14.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS}+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} <4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} <4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANn	-	-	15.6	pF	
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	Ω	AV_{SS} <V_{AIN} <AV_{CC}, AVRH
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC}- 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

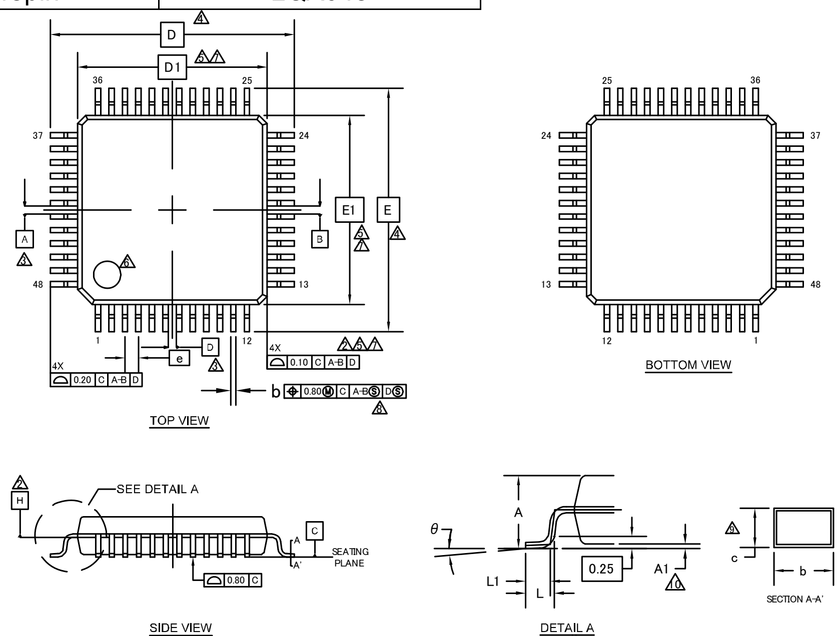

Voltage
Internal Reset
Release Voltage
Vcc
dV
dt
V HYS
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time T LVDSTAB
Low voltage detection function enable···

17. Package Dimension

LQA048, 48 Lead Plastic Low Profile Quad Flat Package

Package Type	Package Code
LQFP 48pin	LQA048



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

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