Infineon Technologies - MB96F615RBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

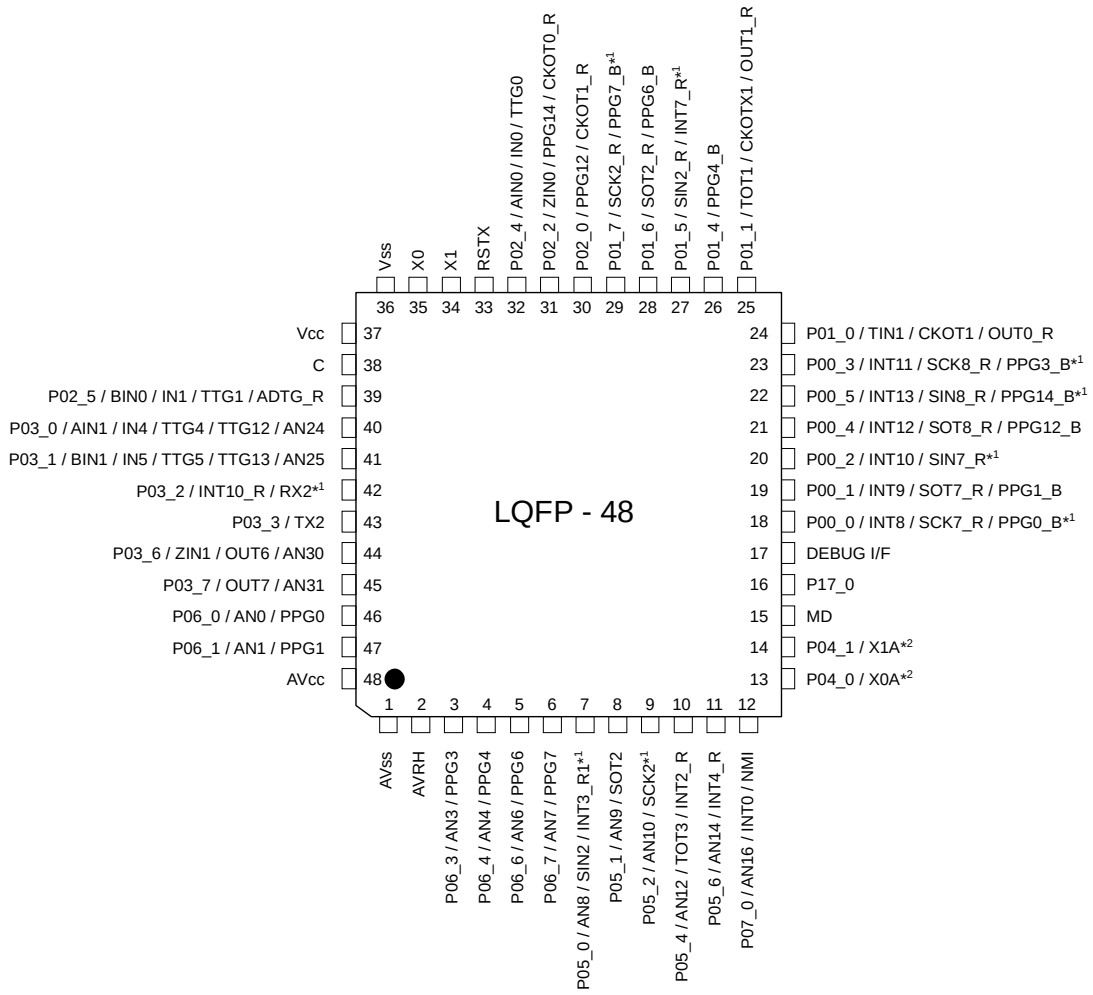
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f615rbpmc-gse2

3. Pin Assignment

(Top view)



(LQA048)

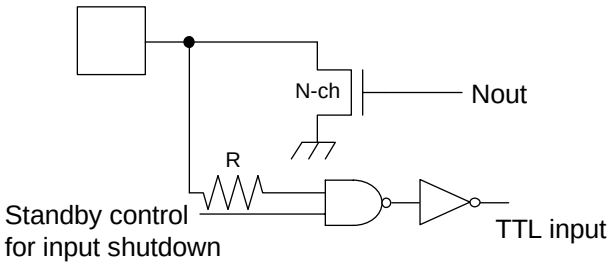
*1: CMOS input level only

*2: Please set ROM Configuration Block (RCB) to use the subclock.

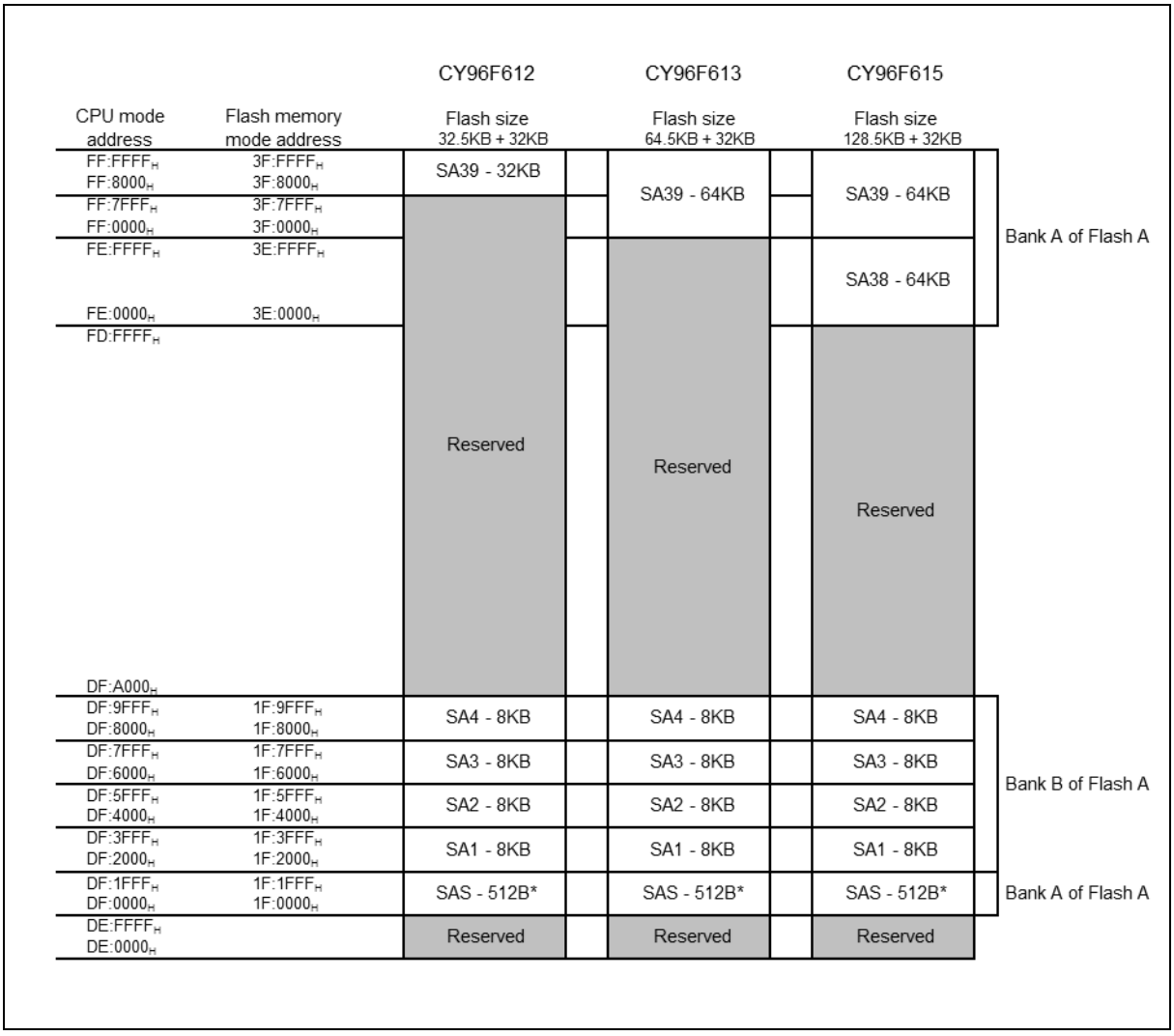
Other than those above, general-purpose pins have only Automotive input level.

4. Pin Description

Pin Name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
INn	ICU	Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
INTn_R1	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
V_{cc}	Supply	Power supply pin
V_{ss}	Supply	Power supply pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

Type	Circuit	Remarks
O		■ Open-drain I/O ■ Output 25mA, Vcc = 2.7V ■ TTL input

9. User ROM Memory Map for Flash Devices



*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
40	$35C_H$	-	-	40	Reserved
41	358_H	PPG3	Yes	41	Programmable Pulse Generator 3
42	354_H	PPG4	Yes	42	Programmable Pulse Generator 4
43	350_H	-	-	43	Reserved
44	$34C_H$	PPG6	Yes	44	Programmable Pulse Generator 6
45	348_H	PPG7	Yes	45	Programmable Pulse Generator 7
46	344_H	-	-	46	Reserved
47	340_H	-	-	47	Reserved
48	$33C_H$	-	-	48	Reserved
49	338_H	-	-	49	Reserved
50	334_H	PPG12	Yes	50	Programmable Pulse Generator 12
51	330_H	-	-	51	Reserved
52	$32C_H$	PPG14	Yes	52	Programmable Pulse Generator 14
53	328_H	-	-	53	Reserved
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	-	-	58	Reserved
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	-	-	60	Reserved
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	RLT6	Yes	64	Reload Timer 6
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6
72	$2DC_H$	-	-	72	Reserved
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	ICU9	Yes	74	Input Capture Unit 9
75	$2D0_H$	ICU10	Yes	75	Input Capture Unit 10
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	-	-	79	Reserved
80	$2BC_H$	-	-	80	Reserved

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage[1]	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage[1]	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$[2]
Analog reference voltage[1]	AVRH	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AVRH \geq AV_{SS}$
Input voltage[1]	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V[3]
Output voltage[1]	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V[3]
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins [4]
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	-	-	13	mA	Applicable to general purpose I/O pins [4]
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	32	mA	
"L" level average overall output current	ΣI_{OLAV}	-	-	16	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-32	mA	
"H" level average overall output current	ΣI_{OHAV}	-	-	-16	mA	
Power consumption[5]	P_D	T_A= +125°C	-	284[6]	mW	
Operating ambient temperature	T_A	-	-40	+125[7]	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

[1]: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

[2]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

[3]: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of standard ports depend on V_{CC}.

[4]:

- Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[1]	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
				-	-	14	mA	T_A = +125°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T_A = +25°C
				-	-	4	mA	T_A = +105°C
				-	-	5	mA	T_A = +125°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
				-	-	4.5	mA	T_A = +125°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T_A = +25°C
				-	-	2.7	mA	T_A = +105°C
				-	-	3.7	mA	T_A = +125°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.5	mA	T_A = +105°C
				-	-	3.5	mA	T_A = +125°C

14.3.2 *Pin Characteristics*

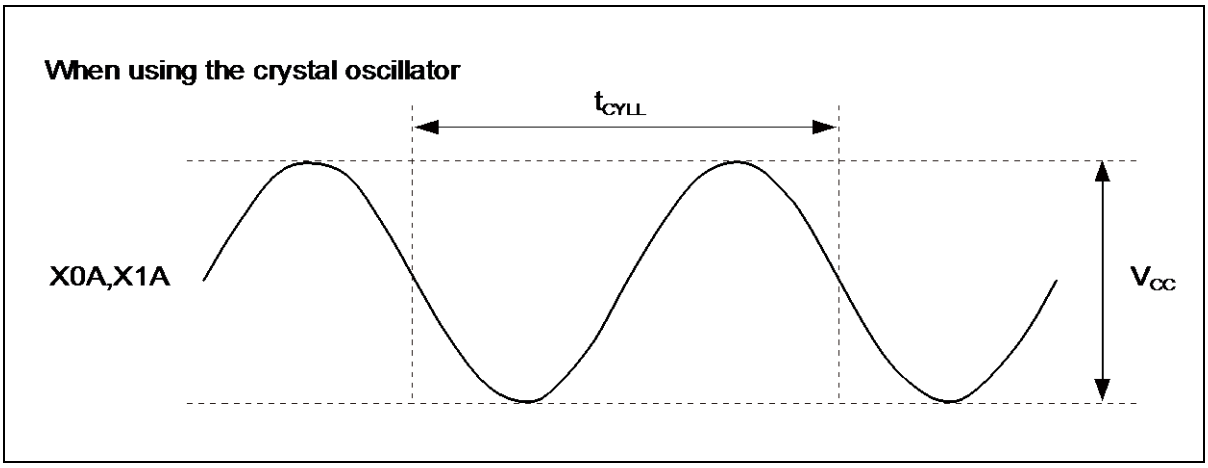
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

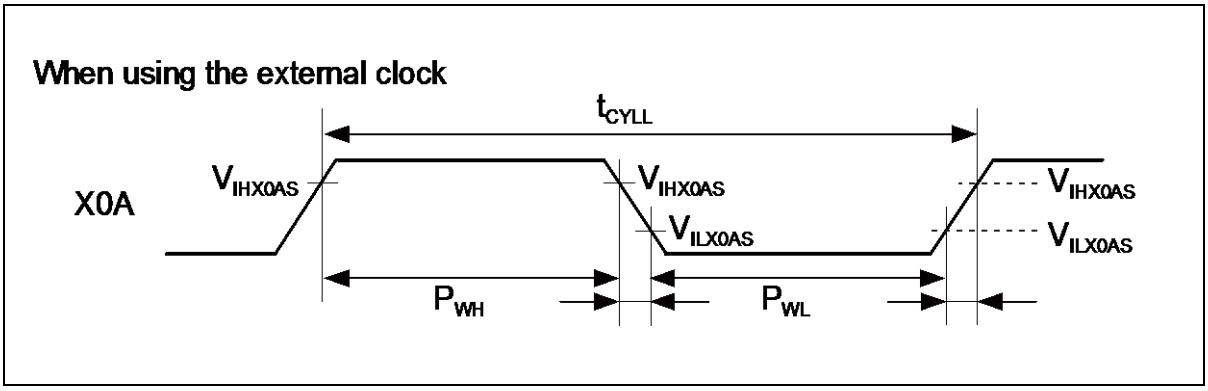
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC}×0.7	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
			-	V_{CC}×0.8	-	V_{CC}+ 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD×0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC}×0.8	-	V_{CC}+ 0.3	V	
	V_{IHR}	RSTX	-	V_{CC}×0.8	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC}- 0.3	-	V_{CC}+ 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC}+ 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS}- 0.3	-	V_{CC}×0.3	V	CMOS Hysteresis input
			-	V_{SS}- 0.3	-	V_{CC}×0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD×0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS}- 0.3	-	V_{CC}×0.2	V	
	V_{ILR}	RSTX	-	V_{SS}- 0.3	-	V_{CC}×0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS}- 0.3	-	V_{SS}+ 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS}- 0.3	-	0.8	V	TTL Input
"H" level output voltage	V_{OH4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -4mA	V_{CC}- 0.5	-	V_{CC}	V	
			2.7V ≤ V_{CC} < 4.5V I_{OH} = -1.5mA					
"L" level output voltage	V_{OL4}	4mA type	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ V_{CC} < 4.5V I_{OL} = +1.7mA					
	V_{OLD}	DEBUG I/F	V_{CC} = 2.7V I_{OL} = +25mA	0	-	0.25	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS} < V_I <AV_{CC}, AVRH	- 1	-	+ 1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH	-	-	5	15	pF	

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	





14.4.3 *Built-in RC Oscillation Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 *Internal Clock Timing*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.5 A/D Converter

14.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

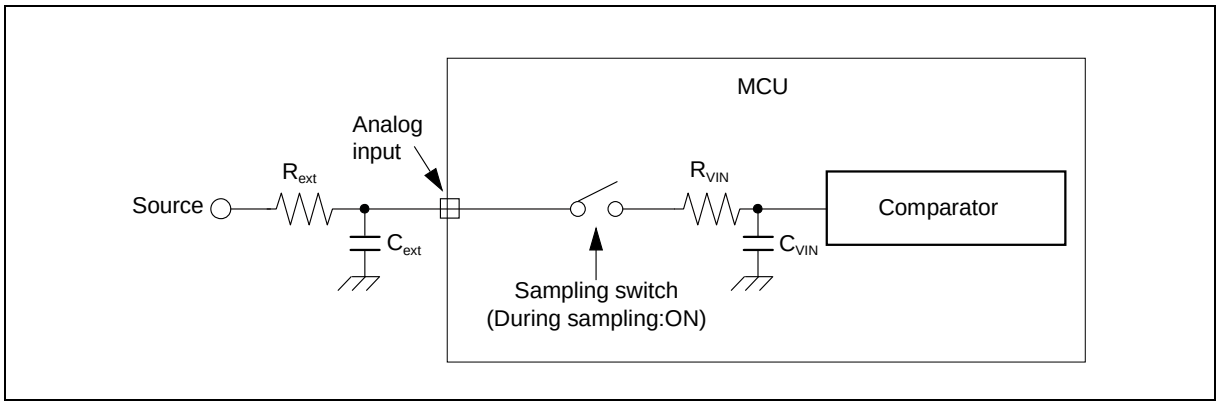
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS}+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} <4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} <4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANn	-	-	15.6	pF	
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	Ω	AV_{SS} <V_{AIN} <AV_{CC}, AVRH
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC}- 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

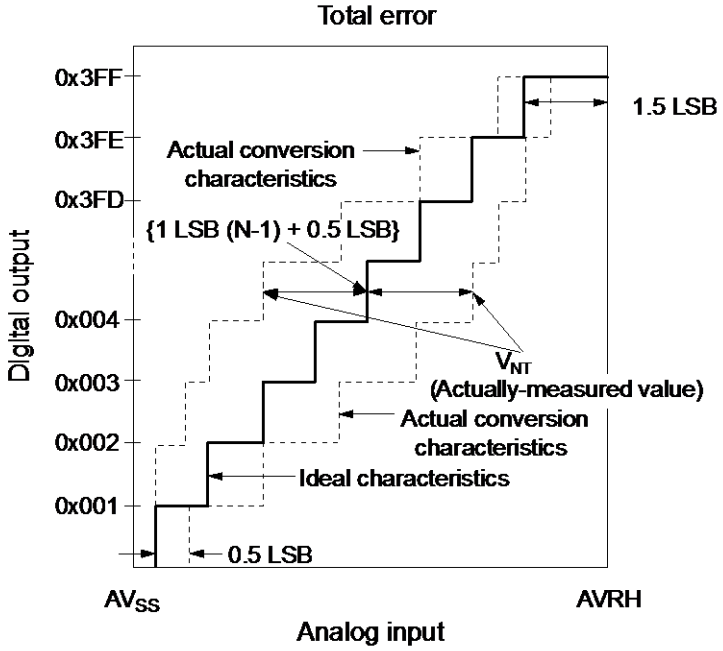
R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.



$$1LSB\ (Ideal\ value) = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT} (Ideal value) = AV_{SS} + 0.5LSB[V]
V_{FST} (Ideal value) = AVRH - 1.5LSB[V]

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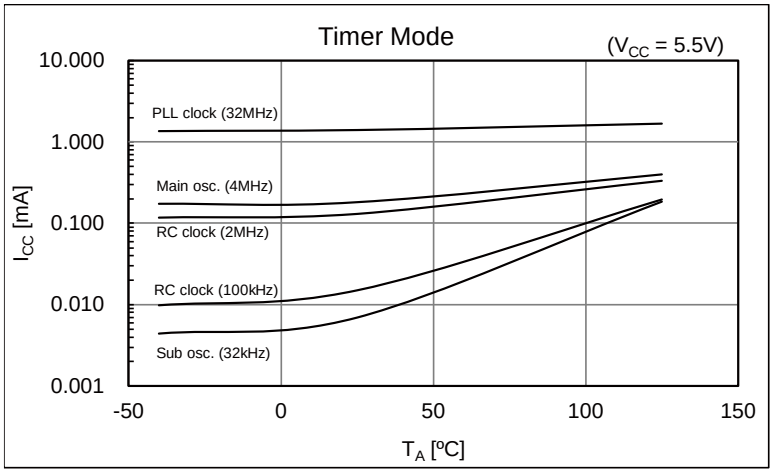
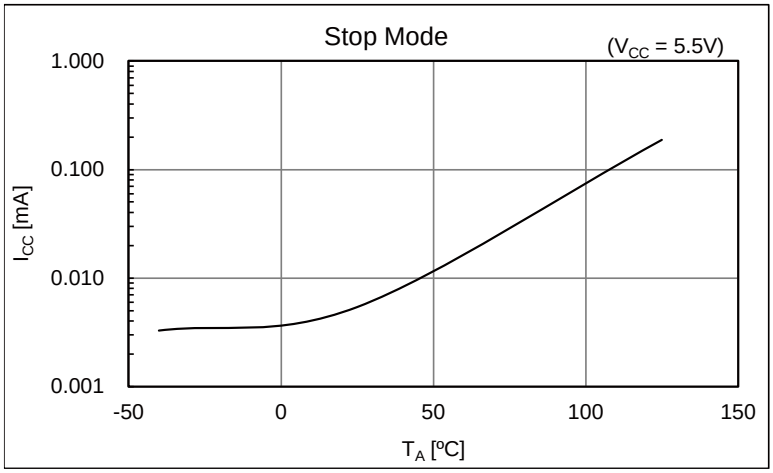

Timer Mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC} [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
T_A [ºC]


Stop Mode
(V_{CC} = 5.5V)
1.000
0.100
0.010
0.001
I_{CC} [mA]
-50
0
50
100
150
T_A [ºC]

Used Setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

18. Major Changes

Spansion Publication Number: MB96610_DS704-00007

Page	Section	Change Results
Revision 3.0		
4	■FEATURES	Changed the description of “External Interrupts” Interrupt mask and pending bit per channel Interrupt mask bit per channel
23 to 26	■HANDLING PRECAUTIONS	Added a section
34	■ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,
		Changed the Conditions for I_{CCSRCL} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz CLKS1/2 = CLKP1/2 = CLKRC = 100kHz
35		Changed the Conditions for I_{CCTPLL} PLL Timer mode with CLKP1 = 32MHz PLL Timer mode with CLKPLL = 32MHz
		Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2480µA → 1800µA (T_A = +25°C) Max: 2710µA → 2245µA (T_A = +25°C) Max: 3985µA → 3165µA (T_A = +105°C) Max: 4830µA → 3975µA (T_A = +125°C)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)
36		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. The current for "On Chip Debugger" part is not included.
47	5. A/D Converter (2) Accuracy and Setting of the A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
52	7. Flash Memory Write/Erase Characteristics	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C) (V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)