Infineon Technologies - MB96F622ABPMC1-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f622abpmc1-gse1

- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

A/D Converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 ×8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

Quadrature Position/Revolution Counter (QPRC)

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

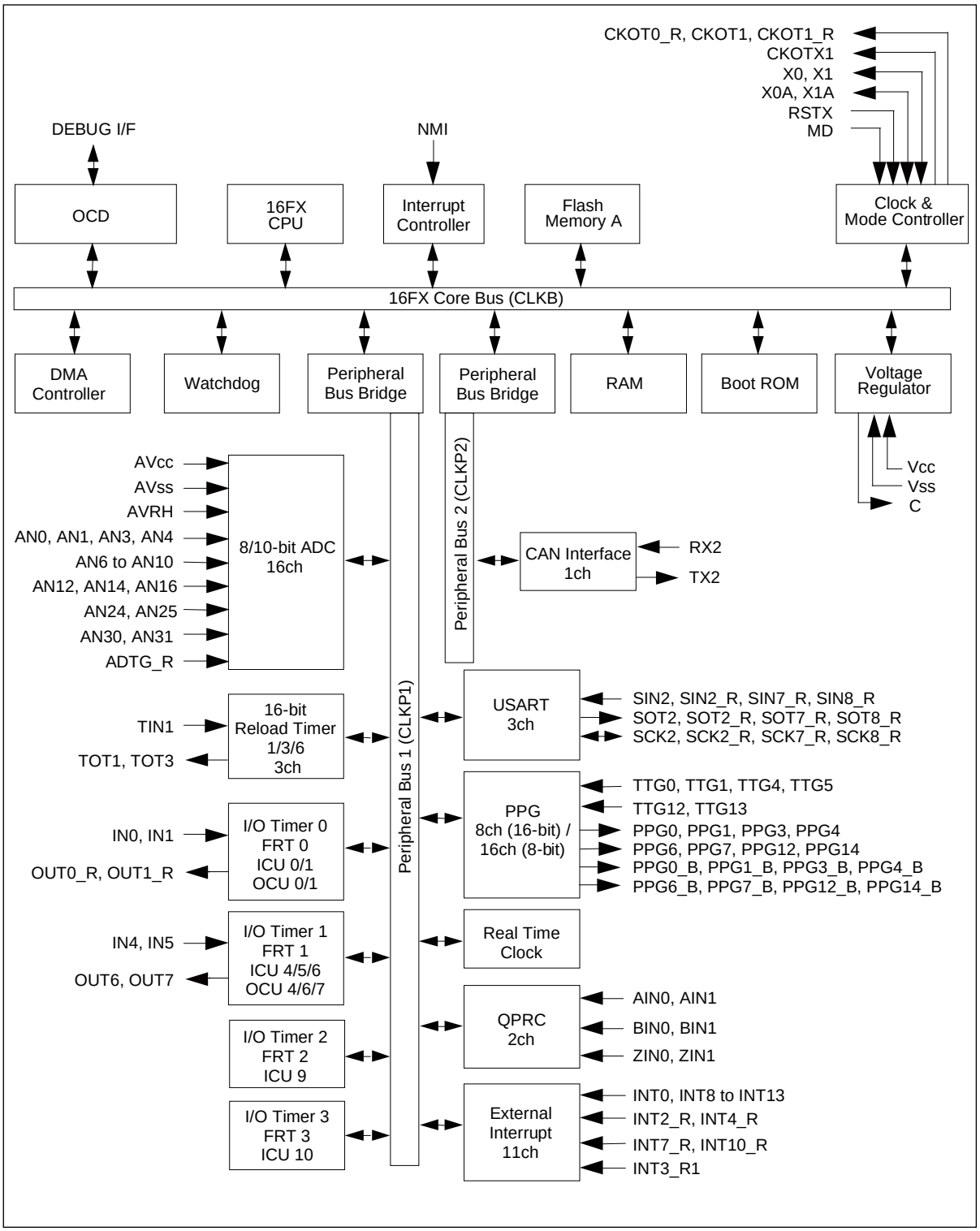
Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

2. Block Diagram



4. Pin Description

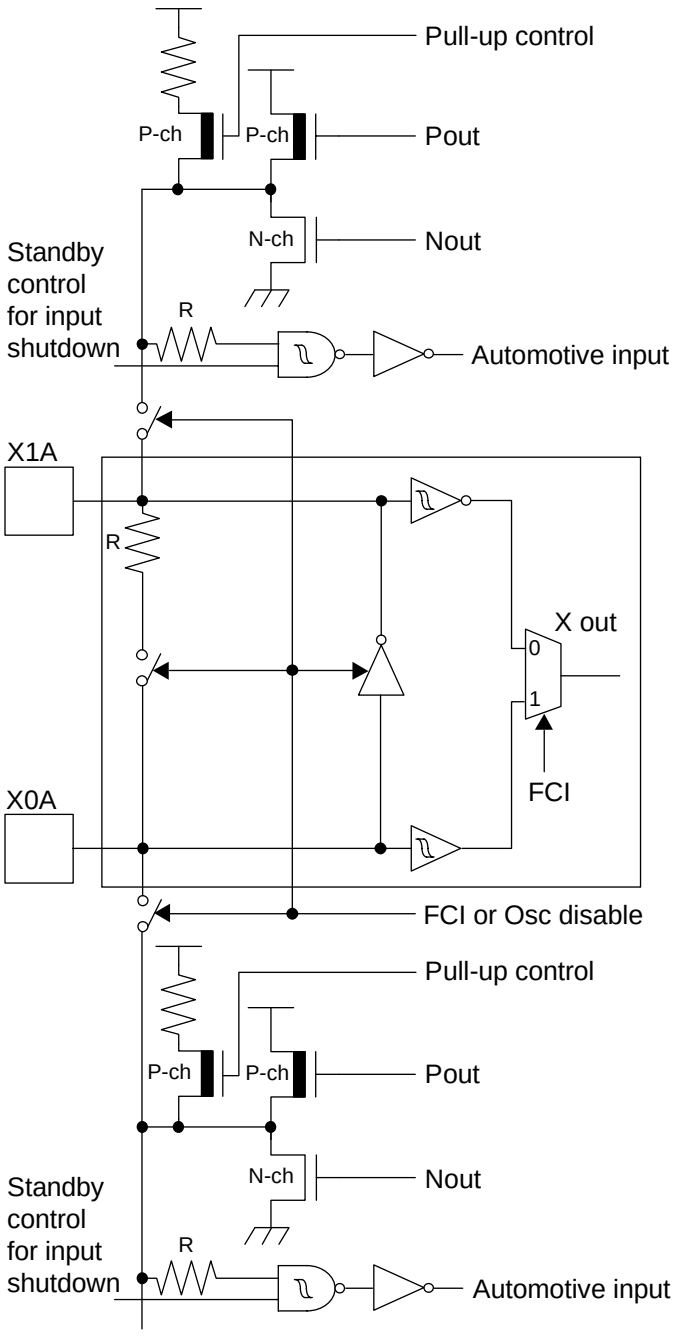
Pin Name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
INn	ICU	Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
INTn_R1	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
V_{cc}	Supply	Power supply pin
V_{ss}	Supply	Power supply pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin

5. Pin Circuit Type

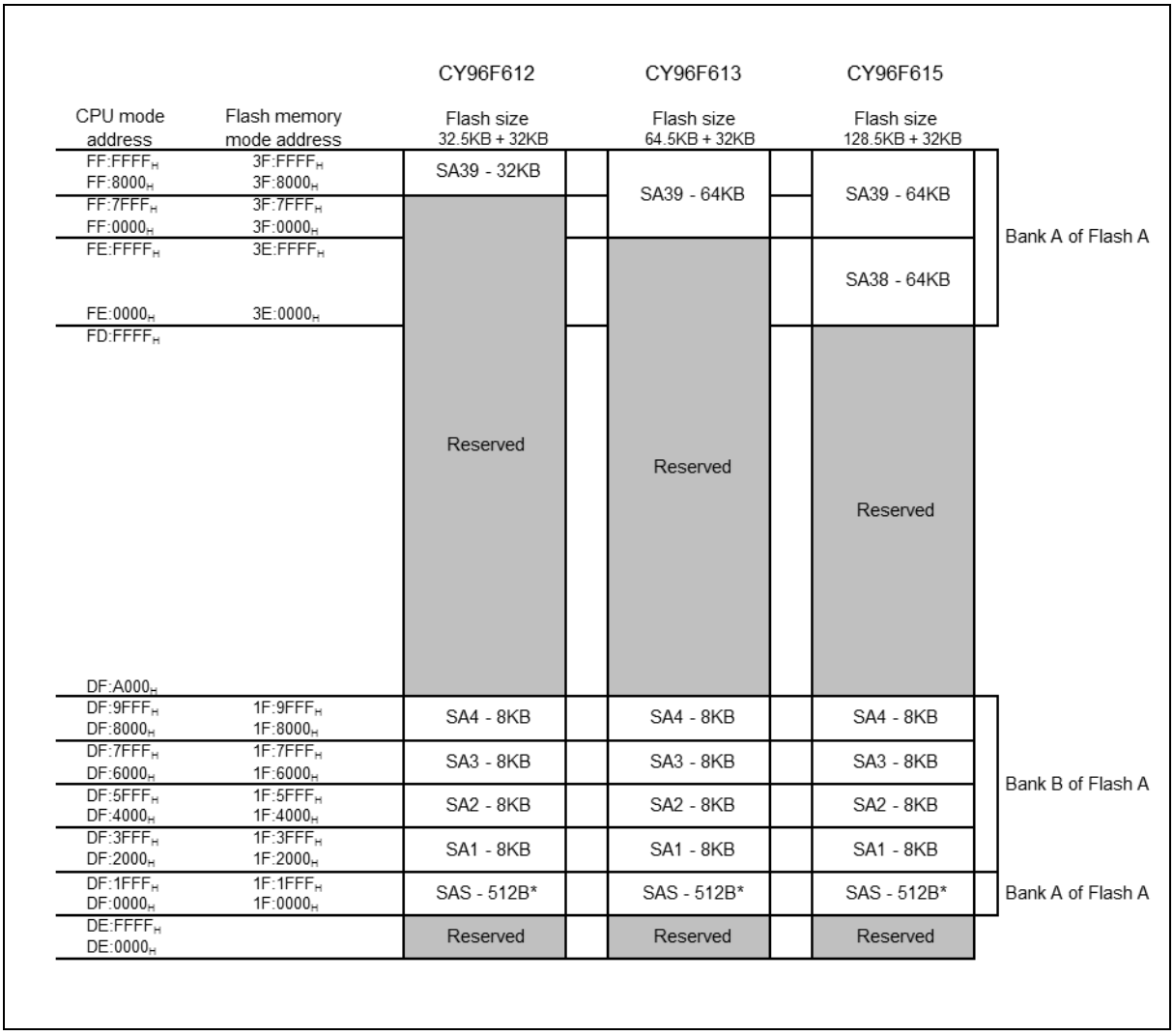
Pin No.	I/O Circuit Type*	Pin Name
1	Supply	AVss
2	G	AVRH
3	K	P06_3 / AN3 / PPG3
4	K	P06_4 / AN4 / PPG4
5	K	P06_6 / AN6 / PPG6
6	K	P06_7 / AN7 / PPG7
7	I	P05_0 / AN8 / SIN2 / INT3_R1
8	K	P05_1 / AN9 / SOT2
9	I	P05_2 / AN10 / SCK2
10	K	P05_4 / AN12 / TOT3 / INT2_R
11	K	P05_6 / AN14 / INT4_R
12	K	P07_0 / AN16 / INT0 / NMI
13	B	P04_0 / X0A
14	B	P04_1 / X1A
15	C	MD
16	H	P17_0
17	O	DEBUG I/F
18	M	P00_0 / INT8 / SCK7_R / PPG0_B
19	H	P00_1 / INT9 / SOT7_R / PPG1_B
20	M	P00_2 / INT10 / SIN7_R
21	H	P00_4 / INT12 / SOT8_R / PPG12_B
22	M	P00_5 / INT13 / SIN8_R / PPG14_B
23	M	P00_3 / INT11 / SCK8_R / PPG3_B
24	H	P01_0 / TIN1 / CKOT1 / OUT0_R
25	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
26	H	P01_4 / PPG4_B
27	M	P01_5 / SIN2_R / INT7_R
28	H	P01_6 / SOT2_R / PPG6_B
29	M	P01_7 / SCK2_R / PPG7_B
30	H	P02_0 / PPG12 / CKOT1_R
31	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
32	H	P02_4 / AIN0 / IN0 / TTG0

Pin No.	I/O Circuit Type*	Pin Name
33	C	RSTX
34	A	X1
35	A	X0
36	Supply	Vss
37	Supply	Vcc
38	F	C
39	H	P02_5 / BIN0 / IN1 / TTG1 / ADTG_R
40	K	P03_0 / AIN1 / IN4 / TTG4 / TTG12 / AN24
41	K	P03_1 / BIN1 / IN5 / TTG5 / TTG13 / AN25
42	M	P03_2 / INT10_R / RX2
43	H	P03_3 / TX2
44	K	P03_6 / ZIN1 / OUT6 / AN30
45	K	P03_7 / OUT7 / AN31
46	K	P06_0 / AN0 / PPG0
47	K	P06_1 / AN1 / PPG1
48	Supply	AVcc

*: See I/O Circuit Type" for details on the I/O circuit types.

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: ■ Feedback resistor = approx. 5.0MΩ ■ GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)

9. User ROM Memory Map for Flash Devices



*: Physical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96610		
Pin Number	**USART Number**	**Normal Function**
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

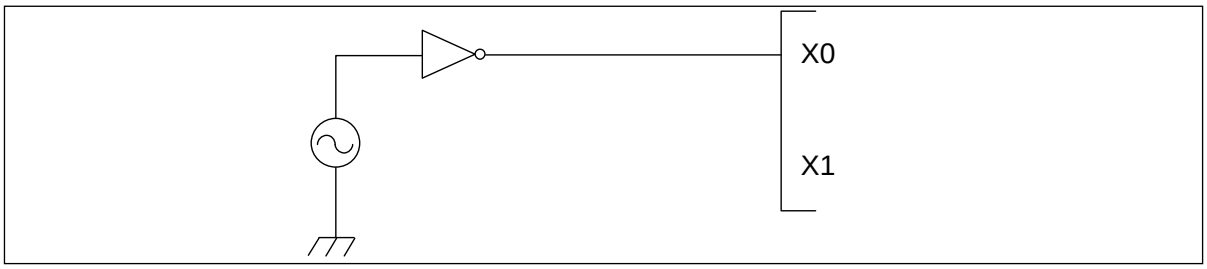
Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 *Single Phase External Clock for Main Oscillator*

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 1.8V power to the external clock.

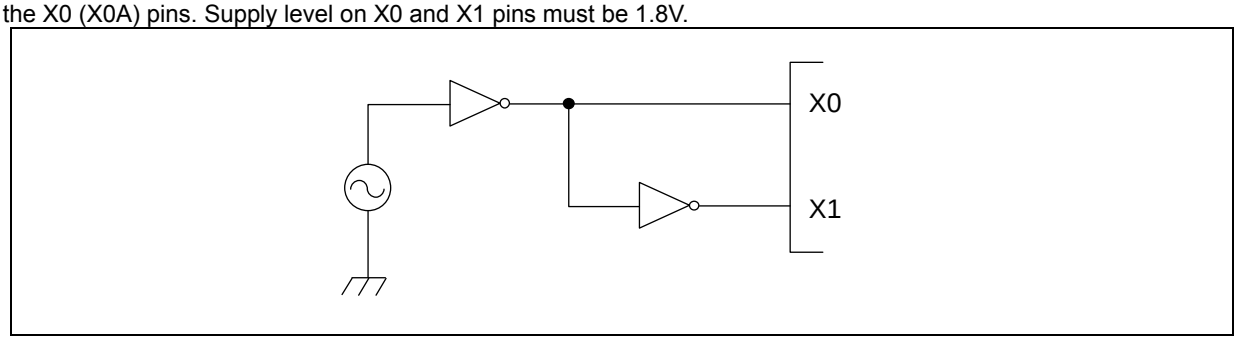


13.3.2 *Single Phase External Clock for Sub Oscillator*

When using a single phase external clock for the Sub oscillator, “External clock mode” must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 *Opposite Phase External Clock*

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL Clock Mode Operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power Supply Pins (Vcc/Vss)

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

Vcc and Vss pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at Vcc pin must use the one of a capacity value that is larger than Cs.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between Vcc and Vss pins as close as possible to Vcc and Vss pins.

13.6 Crystal Oscillator and ceramic resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

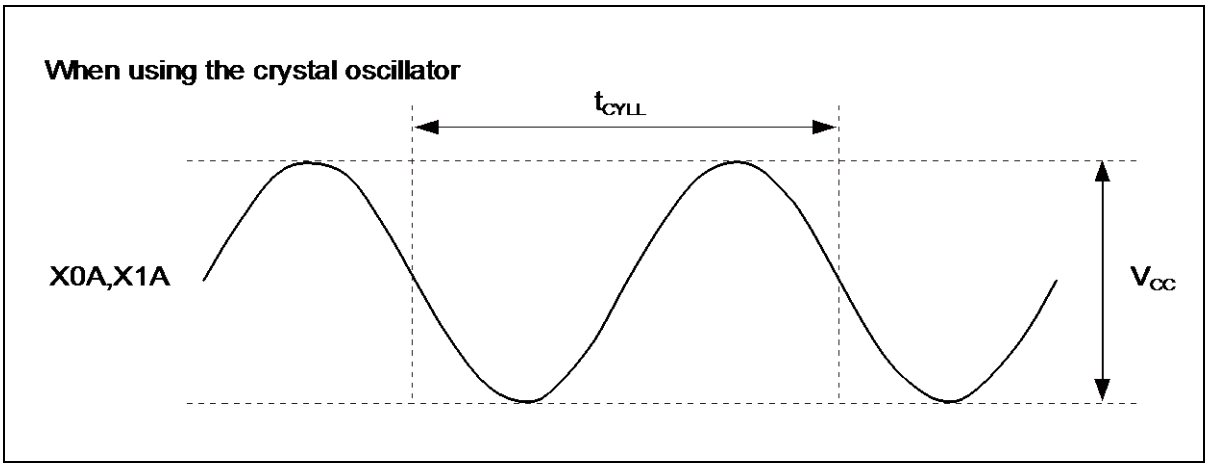
It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

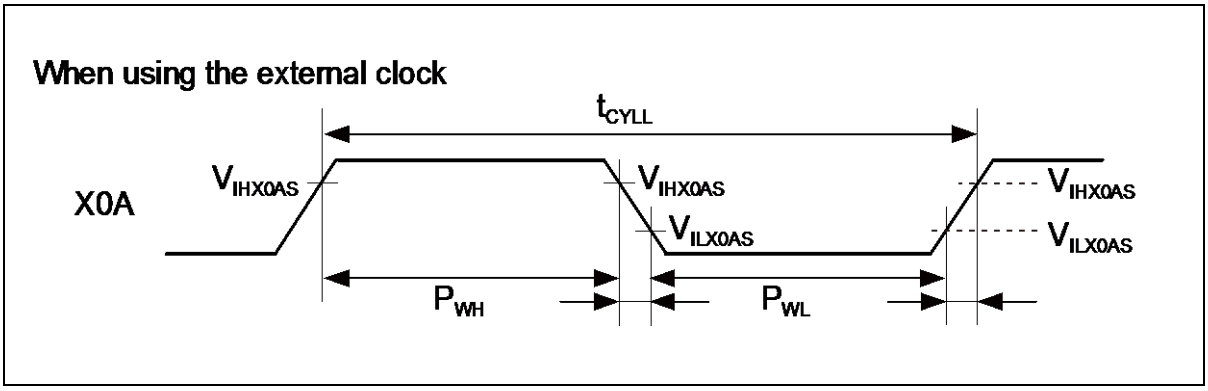
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Sleep modes[1]	I_{CCSPLL}	Vcc	PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	6.5	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
				-	-	14	mA	T_A = +125°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	0.9	-	mA	T_A = +25°C
				-	-	4	mA	T_A = +105°C
				-	-	5	mA	T_A = +125°C
	I_{CCSRCH}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped)	-	0.5	-	mA	T_A = +25°C
				-	-	3.5	mA	T_A = +105°C
				-	-	4.5	mA	T_A = +125°C
	I_{CCSRCL}		RC Sleep mode with CLKS1/2 = CLKP1/2 = CLKRC = 100kHz (CLKMC, CLKPLL and CLKSC stopped)	-	0.06	-	mA	T_A = +25°C
				-	-	2.7	mA	T_A = +105°C
				-	-	3.7	mA	T_A = +125°C
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.04	-	mA	T_A = +25°C
				-	-	2.5	mA	T_A = +105°C
				-	-	3.5	mA	T_A = +125°C

14.4.2 *Sub Clock Input Characteristics*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	30	-	70	%	

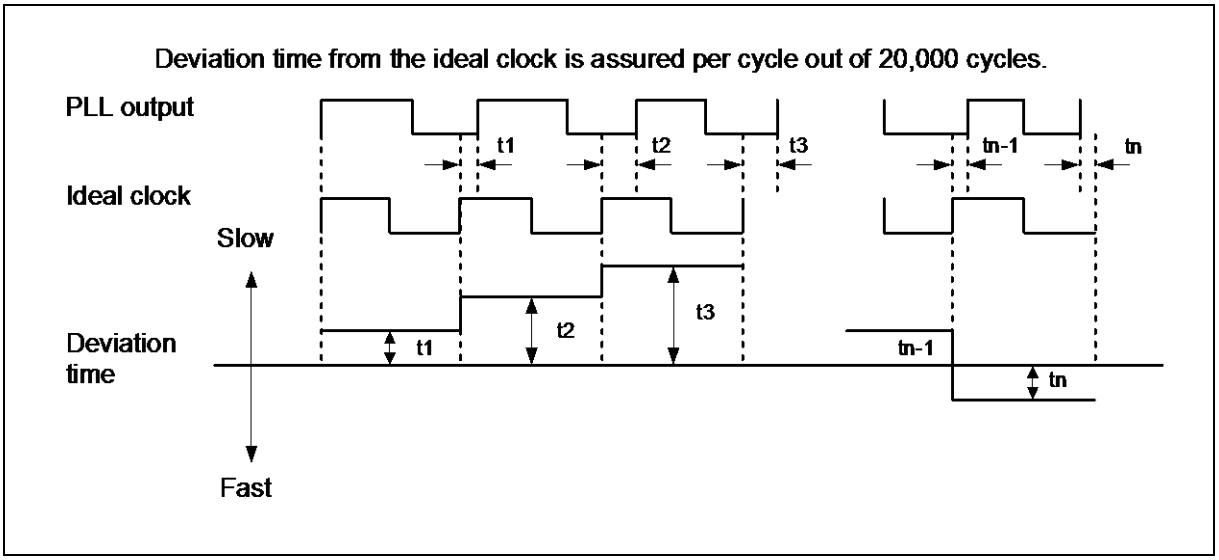




14.4.5 *Operating Conditions of PLL*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

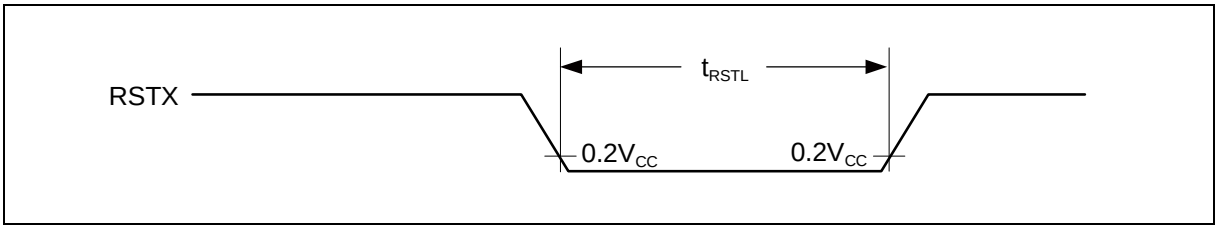
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

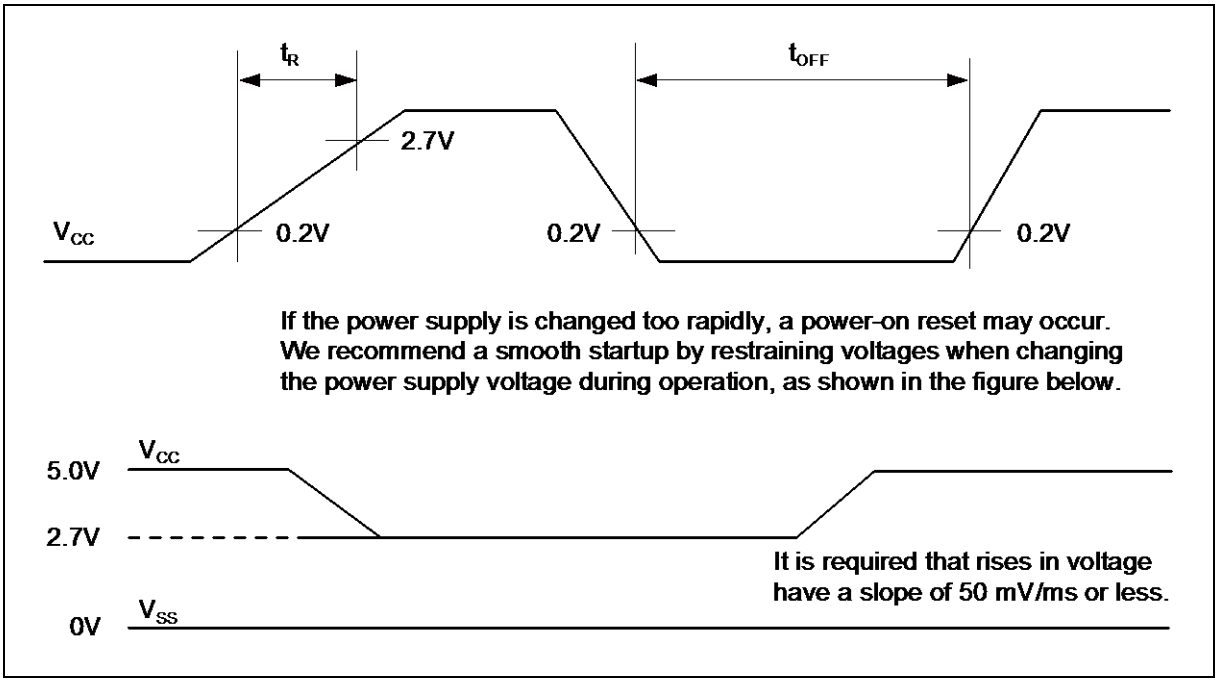
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs

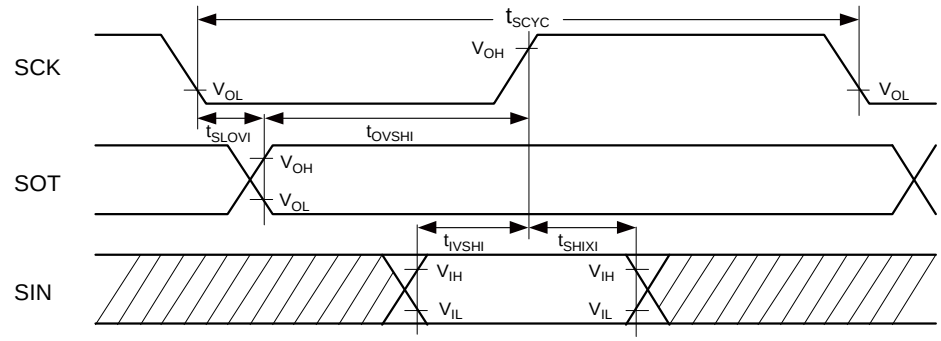


14.4.7 *Power-on Reset Timing*

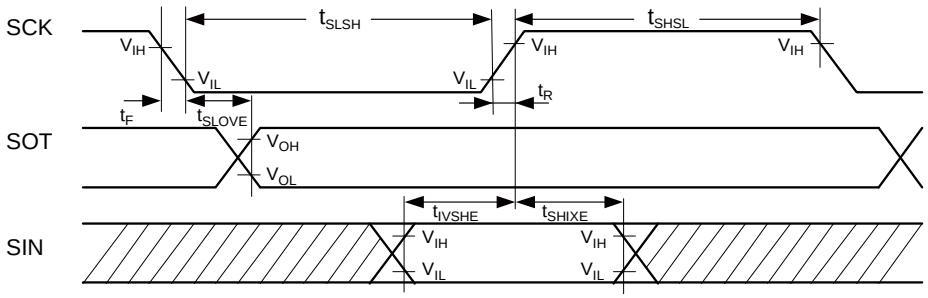
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms





Internal shift clock mode

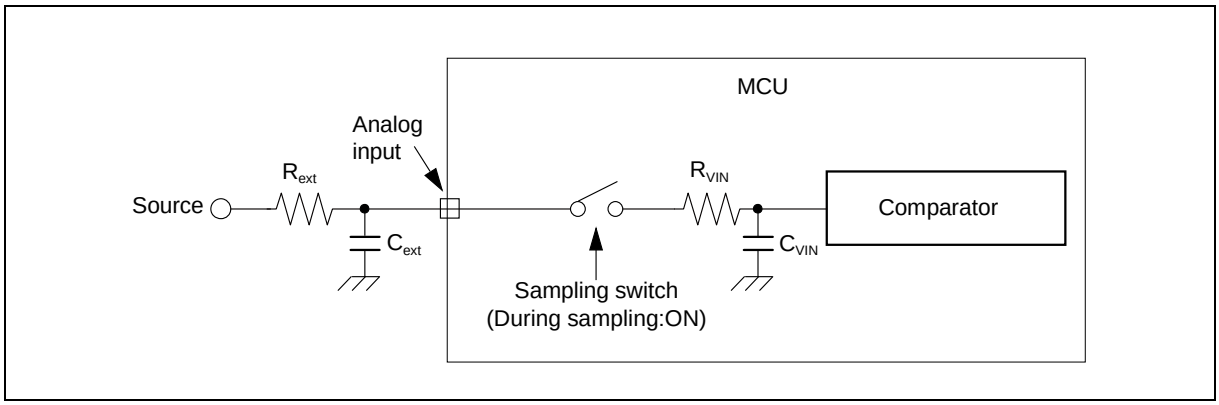


External shift clock mode

14.5.2 *Accuracy and Setting of the A/D Converter Sampling Time*

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

- Do not select a sampling time below the absolute minimum permitted value.
  (0.5µs for $4.5V \le AV_{CC} \le 5.5V$, 1.2µs for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

14.5.3 *Definition of A/D Converter Terms*

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.

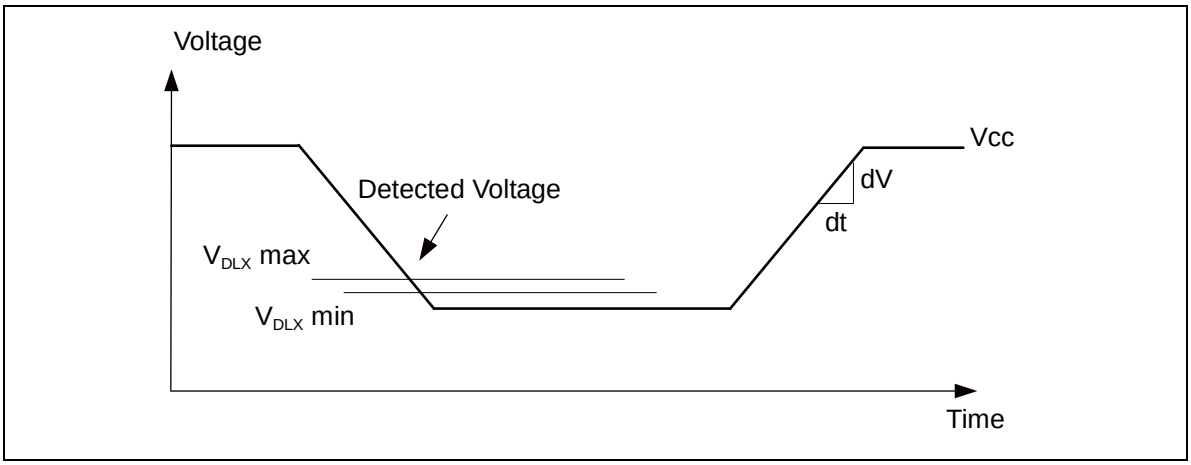
14.6 Low Voltage Detection Function Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage[1]	V_{DL0}	CILCR:LVL = 0000_B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001_B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010_B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011_B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100_B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111_B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001_B	3.91	4.20	4.49	V
Power supply voltage change rate[2]	dV/dt	-	- 0.004	-	+ 0.004	V/µs
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	µs
Detection delay time	t_d	-	-	-	30	µs

[1]: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

[2]: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.



14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	T_A ≤ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	T_A ≤ + 105°C	-	25	400	µs	Not including system-level overheadtime.
	Small Sector	-	-	25	400	µs	
Chip erase time		T_A ≤ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

*To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].*

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

[1]:See "14.6 Low Voltage Detection Function Characteristics".

[2]:This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85˚c).

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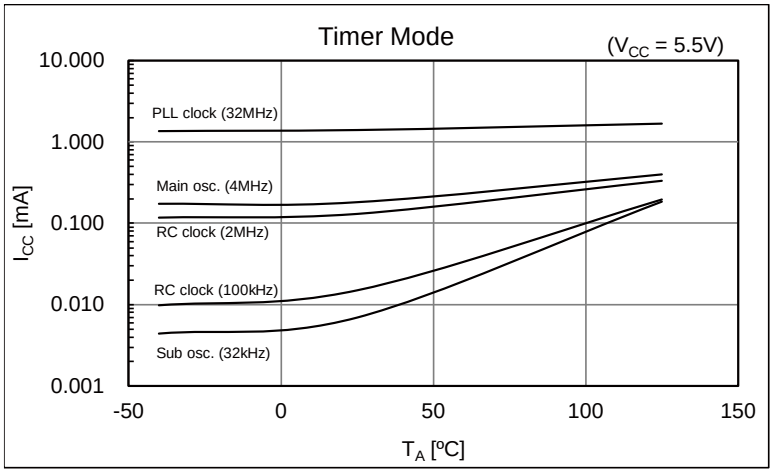
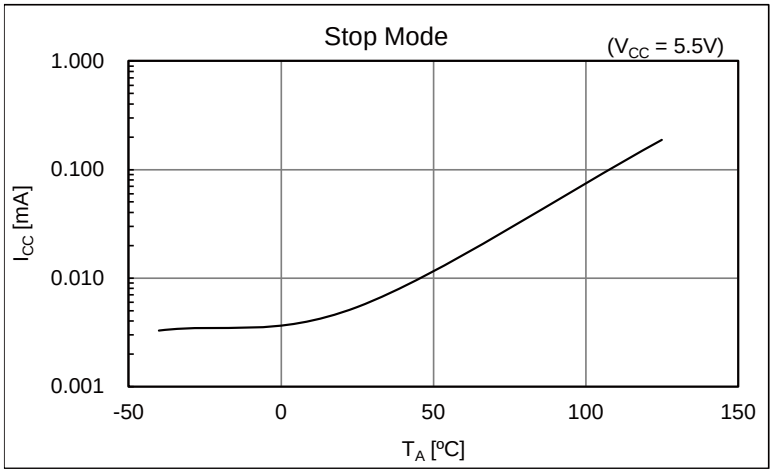

Timer Mode
(V_{CC} = 5.5V)
10.000
1.000
0.100
0.010
0.001
I_{CC} [mA]
PLL clock (32MHz)
Main osc. (4MHz)
RC clock (2MHz)
RC clock (100kHz)
Sub osc. (32kHz)
-50
0
50
100
150
T_A [ºC]


Stop Mode
(V_{CC} = 5.5V)
1.000
0.100
0.010
0.001
I_{CC} [mA]
-50
0
50
100
150
T_A [ºC]