Infineon Technologies - MB96F622ABPMC1-GSE2 Datasheet

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f622abpmc1-gse2

- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

A/D Converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 ×8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

Quadrature Position/Revolution Counter (QPRC)

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

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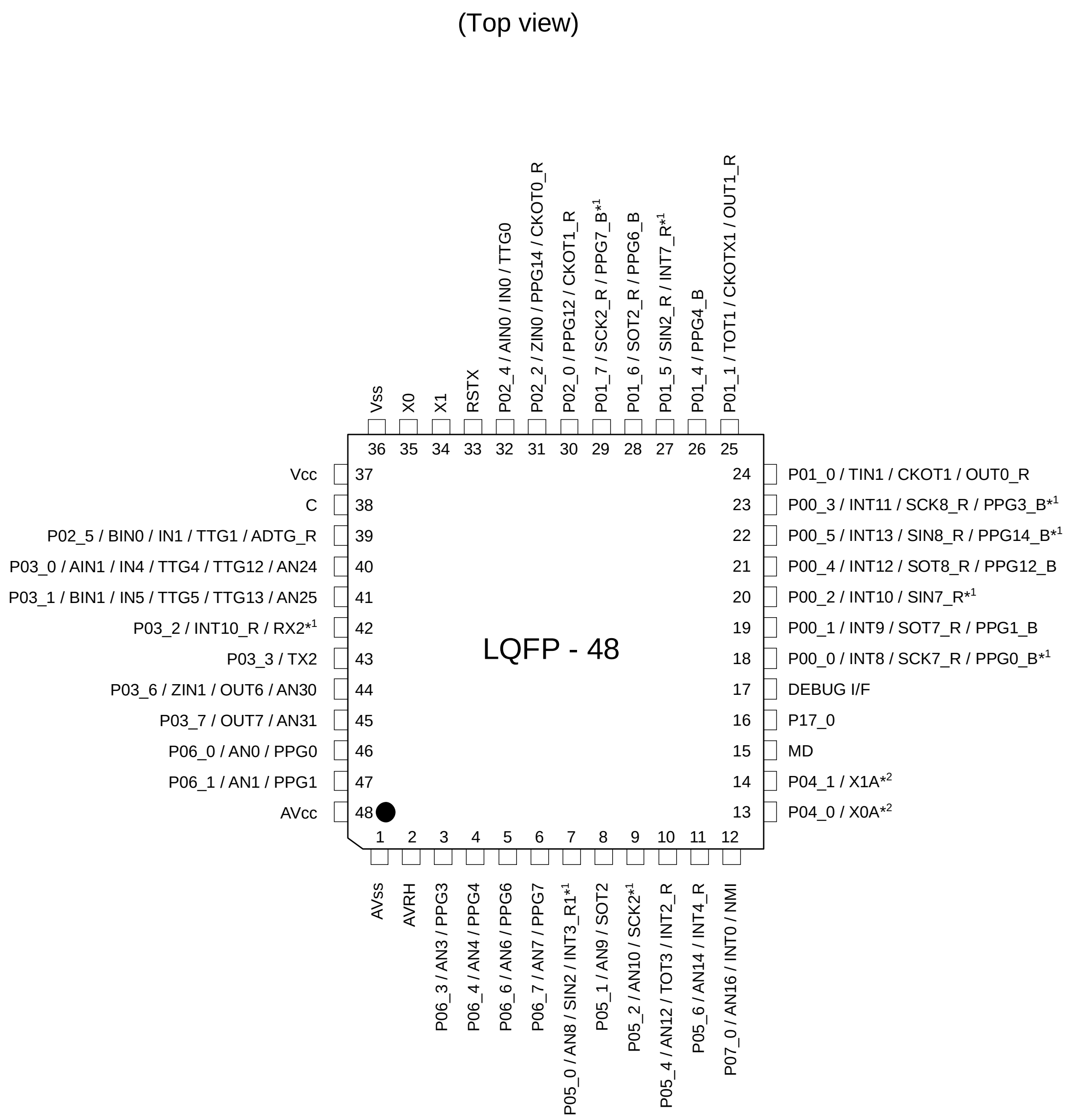
3. Pin Assignment



(LQA048)

*1: CMOS input level only

*2: Please set ROM Configuration Block (RCB) to use the subclock.

Other than those above, general-purpose pins have only Automotive input level.

5. Pin Circuit Type

Pin No.	I/O Circuit Type*	Pin Name
1	Supply	AVss
2	G	AVRH
3	K	P06_3 / AN3 / PPG3
4	K	P06_4 / AN4 / PPG4
5	K	P06_6 / AN6 / PPG6
6	K	P06_7 / AN7 / PPG7
7	I	P05_0 / AN8 / SIN2 / INT3_R1
8	K	P05_1 / AN9 / SOT2
9	I	P05_2 / AN10 / SCK2
10	K	P05_4 / AN12 / TOT3 / INT2_R
11	K	P05_6 / AN14 / INT4_R
12	K	P07_0 / AN16 / INT0 / NMI
13	B	P04_0 / X0A
14	B	P04_1 / X1A
15	C	MD
16	H	P17_0
17	O	DEBUG I/F
18	M	P00_0 / INT8 / SCK7_R / PPG0_B
19	H	P00_1 / INT9 / SOT7_R / PPG1_B
20	M	P00_2 / INT10 / SIN7_R
21	H	P00_4 / INT12 / SOT8_R / PPG12_B
22	M	P00_5 / INT13 / SIN8_R / PPG14_B
23	M	P00_3 / INT11 / SCK8_R / PPG3_B
24	H	P01_0 / TIN1 / CKOT1 / OUT0_R
25	H	P01_1 / TOT1 / CKOTX1 / OUT1_R
26	H	P01_4 / PPG4_B
27	M	P01_5 / SIN2_R / INT7_R
28	H	P01_6 / SOT2_R / PPG6_B
29	M	P01_7 / SCK2_R / PPG7_B
30	H	P02_0 / PPG12 / CKOT1_R
31	H	P02_2 / ZIN0 / PPG14 / CKOT0_R
32	H	P02_4 / AIN0 / IN0 / TTG0

8. RAMstart Addresses

Devices	Bank 0 RAM Size	RAMSTART0
CY96F612	4KB	$00:7200_H$
CY96F613, CY96F615	10KB	$00:5A00_H$

- Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styro foam or other highly static-prone materials for storage of completed board assemblies.

13. Handling Devices

Special Care is Required for the Following when Handling the Device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (Vcc/Vss)
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

13.1 Latch-Up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc pins and Vss pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed

the digital power-supply voltage.

13.2 Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register

PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent

damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with

either input disabled or external pull-up/pull-down resistor as described above.

13.3 External Clock Usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See

13.7 Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVRH must not exceed AV_{CC} Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable)

13.8 Pin Handling when Not Using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V_{CC} AV_{SS} = AVRH = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2V to 2.7V.

13.10Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/μs or less in instantaneous fluctuation for power supply switching.

13.11Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

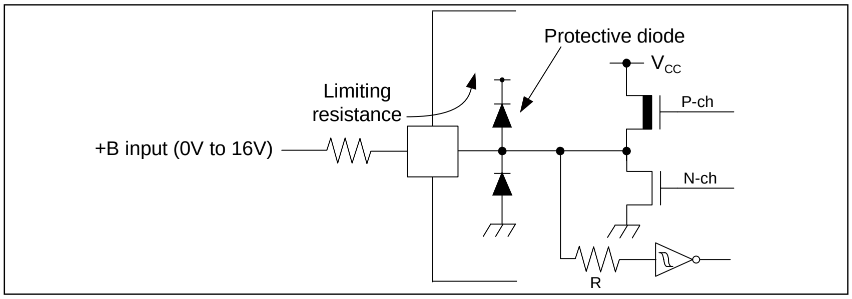
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.12Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Sample recommended circuits:



[5]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)

$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)

I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.

I_A is the analog current consumption into AV_{CC}.

[6]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[7]: Write/erase to a large sector in flash memory is warranted with $T_A \leq + 105°C$.

WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 *Current Rating*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
				-	-	35	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
				-	-	8.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
				-	-	6.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
				-	-	4.2	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes[2]	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	µA	T_A = +25°C
				-	-	3165	µA	T_A = +105°C
				-	-	3975	µA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	µA	T_A = +25°C
				-	-	1085	µA	T_A = +105°C
				-	-	1930	µA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	µA	T_A = +25°C
				-	-	1025	µA	T_A = +105°C
				-	-	1840	µA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	855	µA	T_A = +105°C
				-	-	1640	µA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	830	µA	T_A = +105°C
				-	-	1620	µA	T_A = +125°C
Power supply current in Stop mode[3]	I_{CCH}	Vcc	-	-	20	55	µA	T_A = +25°C
				-	-	825	µA	T_A = +105°C
				-	-	1615	µA	T_A = +125°C
Flash Power Down current	$I_{CCFLASHPD}$		-	-	36	70	µA	
Power supply current for active Low Voltage detector[4]	I_{CCLVD}		Low voltage detector enabled	-	5	-	µA	T_A = +25°C
				-	-	12.5	µA	T_A = +125°C
Flash Write/ Erase current[5]	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +125°C

[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Current for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

[2]: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. The current for "On Chip Debugger" part is not included.

[3]: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.

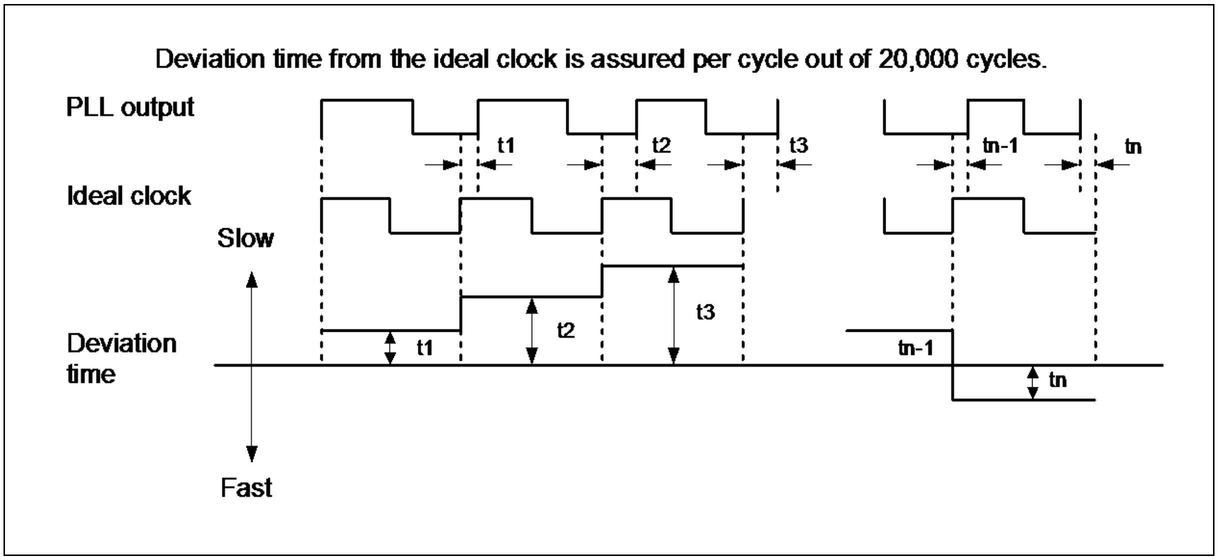
[4]: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

[5]: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

14.4.5 *Operating Conditions of PLL*

($V_{CC} = AV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS}$ = 0V, T_A = - 40°C to + 125°C)

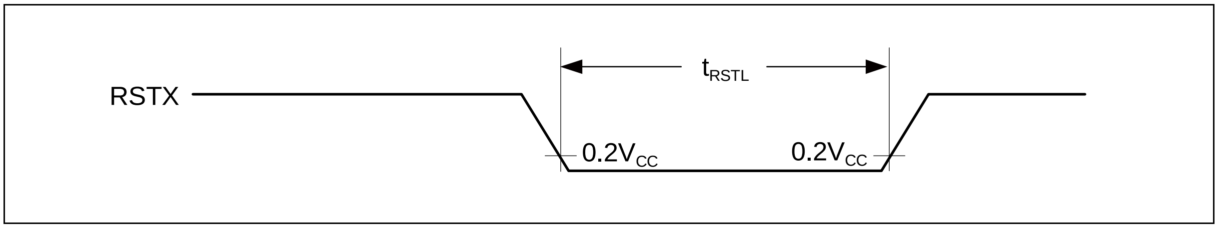
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 *Reset Input*

($V_{CC} = AV_{CC}$ = 2.7V to 5.5V, $V_{SS} = AV_{SS}$ = 0V, T_A = - 40°C to + 125°C)

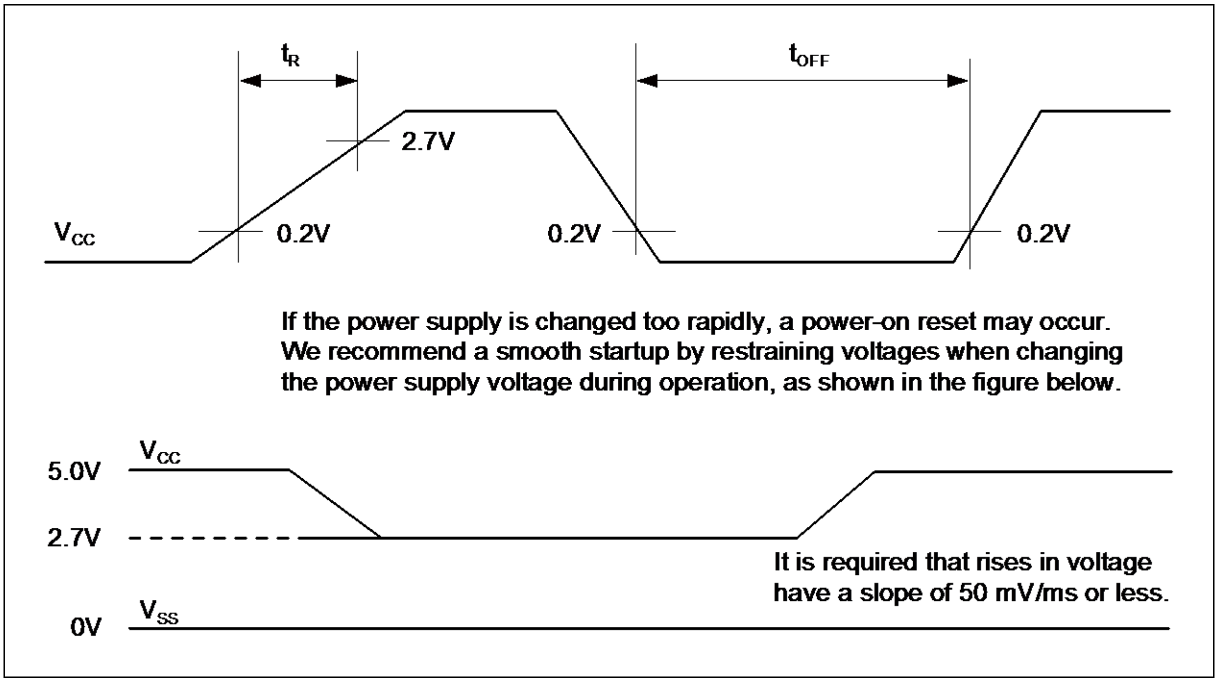
Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.4.7 *Power-on Reset Timing*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Power on rise time	t_R	Vcc	0.05	-	30	ms
Power off time	t_{OFF}	Vcc	1	-	-	ms



If the power supply is changed too rapidly, a power-on reset may occur. We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

It is required that rises in voltage have a slope of 50 mV/ms or less.

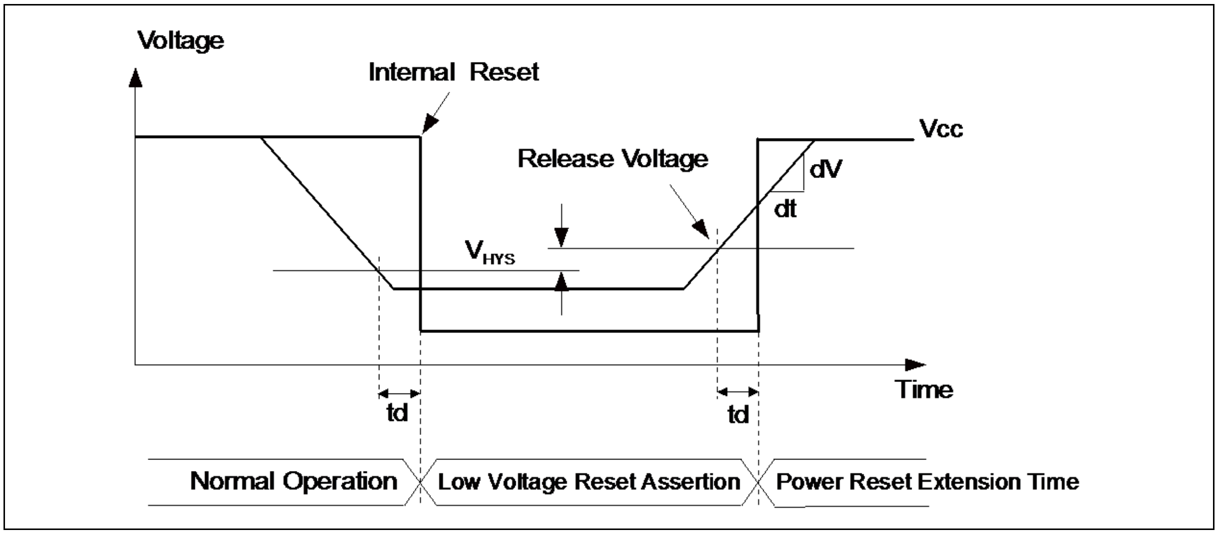
14.5 A/D Converter

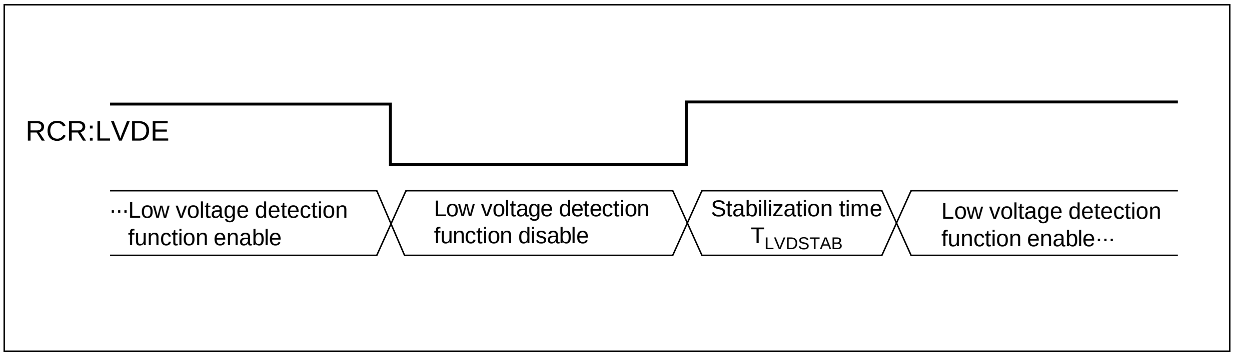
14.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	AV_{SS}+ 0.5LSB	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	AVRH- 1.5LSB	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} <4.5V
Sampling time*	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} <4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANn	-	-	15.6	pF	
Analog impedance	R_{VIN}	ANn	-	-	2050	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
			-	-	3600	Ω	2.7V ≤ AV_{CC} < 4.5V
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	Ω	AV_{SS} <V_{AIN} <AV_{CC}, AVRH
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC}- 0.1	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq$ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq$ + 105°C	-	25	400	µs	Not including system-level overheadtime.
	Small Sector	-	-	25	400	µs	
Chip erase time		$T_A \leq$ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})^{*1}.

Write/Erase cycles and data hold time

Write/Erase Cycles (Cycle)	Data Hold Time (Year)
1,000	20 [2]
10,000	10 [2]
100,000	5 [2]

[1]:See "14.6 Low Voltage Detection Function Characteristics".

[2]:This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85˚c).

Used Setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

Page	Section	Change Results
52	■ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics	Changed the Note While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing, be sure to turn the power off by using an external voltage detector. While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.
56	■ORDERING INFORMATION	Deleted the Part number MCU with CAN controller MB96F612RBPMC-GTE2 MB96F613RBPMC-GTE2 MB96F615RBPMC-GTE2 MCU without CAN controller MB96F612ABPMC-GTE2 MB96F613ABPMC-GTE2 MB96F615ABPMC-GTE2
Revision 3.1		
-	-	Company name and layout design change
Rev.*B		
6, 8, 58, 59	1. Product Lineup 3. Pin Assignment 16. Ordering Information 17. Package Dimension	Package description modified to JEDEC description. FPT-48P-M26 → LQA048
58	16. Ordering Information	Added the following part number. MB96F612RBPMC-GS-UJE1, MB96F612RBPMC-GS-UJE2, MB96F613RBPMC-GS-UJE1, MB96F613RBPMC-GS-UJE2, MB96F615RBPMC-GS-UJE1, MB96F615RBPMC-GS-UJE2, MB96F612ABPMC-GS-UJE1, MB96F612ABPMC-GS-UJE2 MB96F613ABPMC-GS-UJE1, MB96F613ABPMC-GS-UJE2 MB96F615ABPMC-GS-UJE1, MB96F615ABPMC-GS-UJE2
Rev.*C		
58	16. Ordering Information	Deleted the Part number MCU without CAN controller MB96F615ABPMC-GS-UJE2
Rev.*D		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	

Document History

Document Title: CY96610 Series, F^{2}MC, 16FX, 16-bit Proprietary Microcontroller
Document Number: 002-04709

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04709. No change to document contents or format.
*A	5146534	KSUN	02/29/2016	Updated to Cypress template
*B	5735123	KUME	05/15/2017	Updated the Ordering Information and the Package Dimension For details, please see 18. Major Changes.
*C	5809040	MIYH	07/11/2017	Updated the Ordering Information For details, please see 18. Major Changes.
*D	5978072	MIYH	11/30/2017	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 16. Ordering Information For details, please see 18. Major Changes.