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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28243-24pvxi

44-pin Part Pinout

Table 5. 44-pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	M	P2[5]	
2	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
3	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
4	I/O	M	P4[7]	
5	I/O	M	P4[5]	
6	I/O	M	P4[3]	
7	I/O	M	P4[1]	
8	Output		SMP	Switch Mode Pump (SMP) connection to external components.
9	I/O	M	P3[7]	
10	I/O	M	P3[5]	
11	I/O	M	P3[3]	
12	I/O	M	P3[1]	
13	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
14	I/O	M	P1[5]	I2C0 Serial Data (SDA).
15	I/O	M	P1[3]	
16	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
17	Power		V_{SS}	Ground connection.
18	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
19	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
20	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
21	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
22	I/O	M	P3[0]	I2C1 Serial Data (SDA).[7]
23	I/O	M	P3[2]	I2C1 Serial Clock (SCL).[7]
24	I/O	M	P3[4]	
25	I/O	M	P3[6]	
26	Input		XRES	Active high external reset with internal pull-down.
27	I/O	M	P4[0]	
28	I/O	M	P4[2]	
29	I/O	M	P4[4]	
30	I/O	M	P4[6]	
31	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
32	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
33	I/O	M	P2[4]	External Analog Ground (AGND).
34	I/O	M	P2[6]	External Voltage Reference (VRef).
35	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
36	I/O	I/O, M S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
37	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
38	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
39	Power		V_{DD}	Supply voltage.
40	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
41	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
42	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
43	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

CY8C28513, and CY8C28545
44-pin PSoC Devices

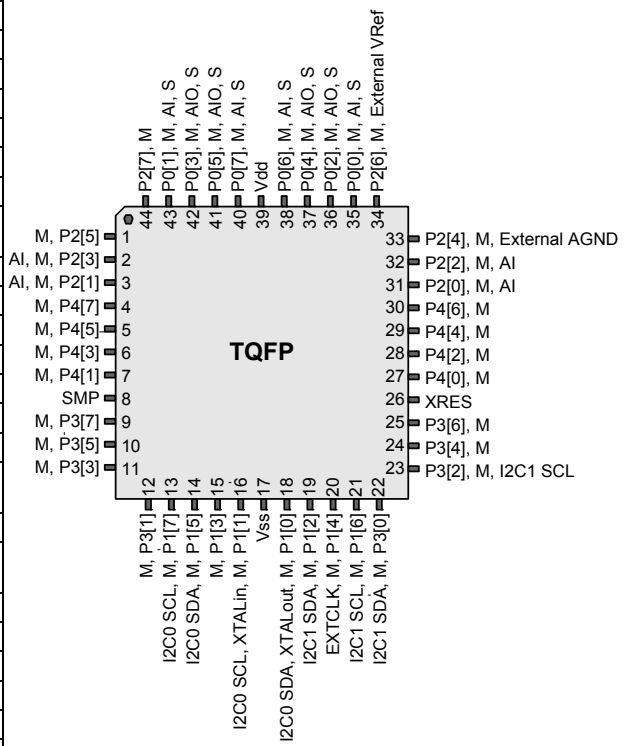


Table 7. 56-pin Part Pinout (SSOP) *(continued)*

Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	Input		XRES	Active high external reset with internal pull-down.
42	OCD	M	HCLK	OCD high speed clock output.
43	OCD	M	CCLK	OCD CPU clock output.
44	I/O	M	P4[0]	
45	I/O	M	P4[2]	
46	I/O	M	P4[4]	
47	I/O	M	P4[6]	
48	I/O	I, M	P2[0]	Direct switched capacitor block input.
49	I/O	I, M	P2[2]	Direct switched capacitor block input.
50	I/O	M	P2[4]	External Analog Ground (AGND).
51	I/O	M	P2[6]	External Voltage Reference (VRef).
52	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.
53	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.
54	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.
55	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.
56	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, M = Analog Mux Bus Input, and OCD = On-Chip Debug.

Table 12. CY8C28x23 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#		A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 17. CY8C28x43 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	8	14	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT.[12]	–	3	10	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT at high temperature.[12]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, sleep timer, WDT, and external crystal.[12]	–	4	13	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[12]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBRTC}	Current consumed by RTC during sleep	–	0.5	1	µA	Extra current consumed by the RTC during sleep. This number is typical at 25 °C and 5 V.
V_{REF}	Reference voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD}.
I_{SXRES}	Supply current with XRES asserted 5 V	–	0.65	3	mA	Max is peak current after XRES; Typical value is the steady state current value. T_A = 25 °C.
	Supply current with XRES asserted 3.3 V	-	0.4	1.5	mA	

Note
12. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

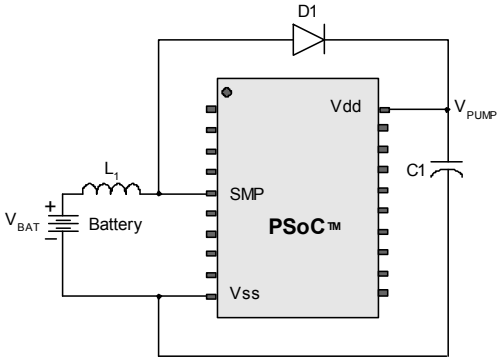
DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote.[14] SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.5	–	3.3	V	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	2.6	–	–	V	Configuration of footnote.[14]
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote.[14] Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[14] Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 9. Basic Switch Mode Pump Circuit



Note
14. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode. See Figure 9.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	3 × Bandgap	3.736	3.887	4.030	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.598	2.667	V
		V_{REFLO}	Ref low	Bandgap	1.265	1.302	1.335	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	3 × Bandgap	3.747	3.894	4.034	V
		V_{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	3 × Bandgap	3.749	3.897	4.035	V
		V_{AGND}	AGND	2 × Bandgap	2.529	2.602	2.668	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	3 × Bandgap	3.751	3.899	4.037	V
		V_{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V
		V_{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.483 – P2[6]	2.578 – P2[6]	2.669 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.598	2.666	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.512 – P2[6]	2.602 – P2[6]	2.684 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.673 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.510 – P2[6]	2.602 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 – P2[6]	2.589 – P2[6]	2.674 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.529	2.601	2.668	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.509 – P2[6]	2.601 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.675 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V
		V_{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.508 – P2[6]	2.601 – P2[6]	2.686 – P2[6]	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.045	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.016	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.019	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.023	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.036	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.021	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.021	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.034	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.023	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.016	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.033	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.014	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] – 0.003	P2[4] – P2[6] + 0.020	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.035	V_{DD}/2 – 0.001	V_{DD}/2 + 0.031	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.0165 V	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.035	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.031	V_{DD}/2 – 0.001	V_{DD}/2 + 0.028	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.044	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.052	V_{DD}/2	V_{DD}/2 + 0.046	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.036	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.032	V_{DD}/2	V_{DD}/2 + 0.029	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.012	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices, for more information on the VLT_CR register.

Table 40. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} Value for PPOR Trip (positive ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0R}	PORLEV[1:0] = 00b	–	2.91	2.985	V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2R}	PORLEV[1:0] = 10b	–	4.55	4.65	V	
	V_{DD} Value for PPOR Trip (negative ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	2.90	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.64	V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.83	2.91	3.00[16]	V	
V_{LVD1}	VM[2:0] = 001b	2.93	3.01	3.10	V	
V_{LVD2}	VM[2:0] = 010b	3.04	3.12	3.21	V	
V_{LVD3}	VM[2:0] = 011b	3.90	3.99	4.09	V	
V_{LVD4}	VM[2:0] = 100b	4.38	4.47	4.58	V	
V_{LVD5}	VM[2:0] = 101b	4.54	4.63	4.74[17]	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.71	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.80	4.92	V	
	V_{DD} Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.93	3.01	3.10	V	
V_{PUMP1}	VM[2:0] = 001b	3.00	3.08	3.17	V	
V_{PUMP2}	VM[2:0] = 010b	3.16	3.24	3.33	V	
V_{PUMP3}	VM[2:0] = 011b	4.09	4.17	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.53	4.62	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.61	4.71	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.70	4.80	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.88	4.98	5.10	V	

Notes
16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

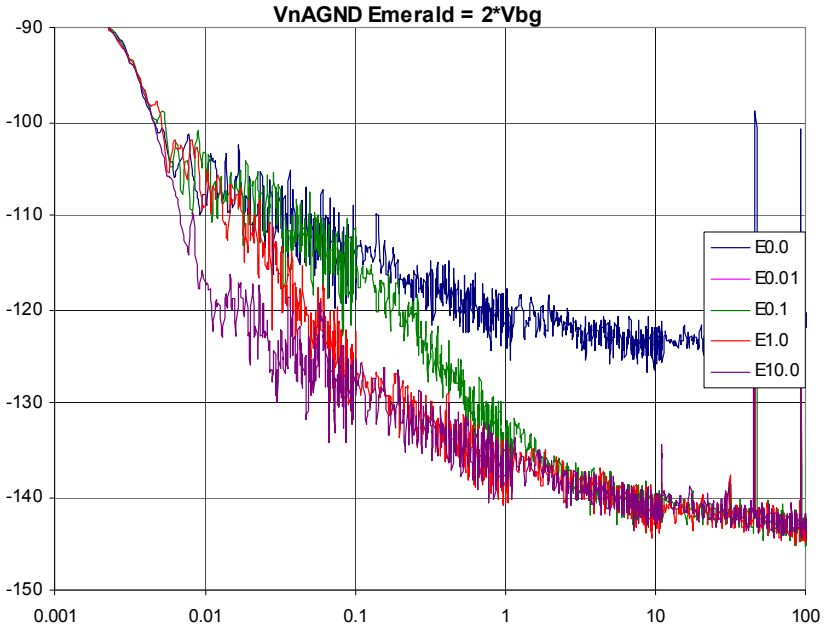
Table 43. AC Chip-Level Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
t_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[24,25]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output.	–	–	12.3	MHz	
$SR_{POWERUP}$	Supply Ramp Time	0	–	–	µs	
$t_{POWERUP}$	Time for POR Release to Code Execution	–	16	100	ms	
t_{jit_IMO} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1300	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1300	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	800	ps	
t_{jit_PLL} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1100	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	400	2800	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	1400	ps	

Notes
24. 4.75 V < V_{DD} < 5.25 V.
25. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
26. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

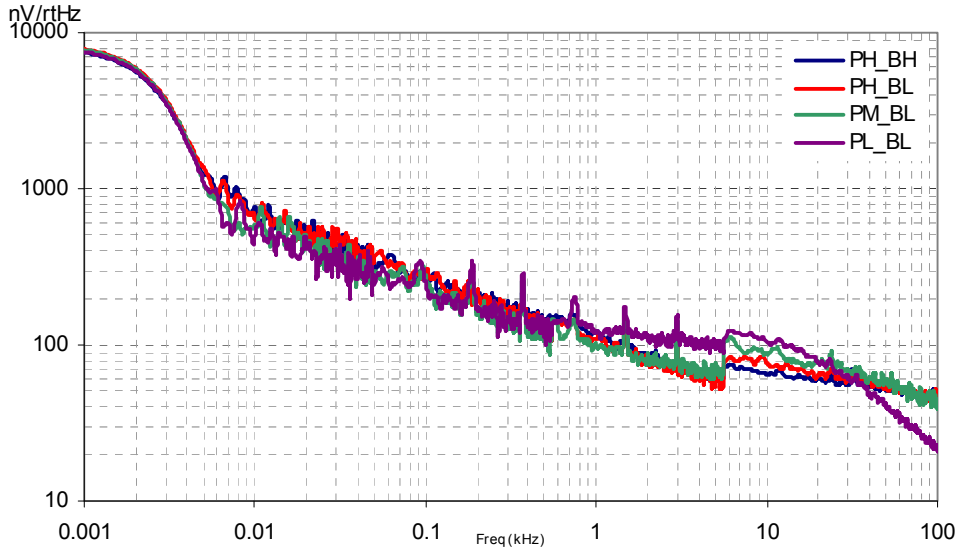
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 14. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 15. Typical Opamp Noise



AC Type-E Operational Amplifier Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 47. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 48. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive.

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 49. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
Timer	Input Clock Frequency					
	No Capture, V_{DD} ≥ 4.75 V	–	–	49	MHz	
	No Capture, V_{DD} < 4.75 V	–	–	25	MHz	
	With Capture	–	–	25	MHz	
	Capture Pulse Width	50[27]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, V_{DD} ≥ 4.75 V	–	–	49	MHz	
	No Enable Input, V_{DD} < 4.75 V	–	–	25	MHz	
	With Enable Input	–	–	25	MHz	
	Enable Input Pulse Width	50[27]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[27]	–	–	ns	
	Disable Mode	50[27]	–	–	ns	
	Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	V_{DD} ≥ 4.75 V	–	–	49	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25	MHz	
SPIM	Input Clock Frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50[13]	–	–	ns	
Tranmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 Stop Bits	–	–	49	MHz	
	V_{DD} ≥ 4.75 V, 1 Stop Bit	–	–	25	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 Stop Bits	–	–	49	MHz	
	V_{DD} ≥ 4.75 V, 1 Stop Bit	–	–	25	MHz	
	V_{DD} < 4.75 V	–	–	25	MHz	

Note
27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 52. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{INSAR10}$	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F_{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 53. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Table 54. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1[28]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[29]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Notes
28. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
29. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

Document History Page

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™ Document Number: 001-48111				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	2593460	BTK / PYRS	10/20/08	New document (Revision **).
*A	2652217	BTK / PYRS	02/02/09	Extensive updates to content. Added registers maps. Updated Getting Started section Updated Development Tools section Added some SAR10 ADC specifications. Added more analog system figures
*B	2675937	BTK	03/18/09	Updated DC Analog Reference Specifications tables Minor content updates
*C	2679015	HMI	03/26/2009	Post to external web.
*D	2750217	TDU	08/10/09	Updates to Electrical Specifications section Minor content updates
*E	2768143	TDU	09/23/09	Updated DC Operational Amplifier, DC Analog Reference, DC SAR10ADC, and DC POR specifications; Added Figure 15 and Figure 16; Updated AC TypeE-Operational and AC SAR10ADC specifications
*F	2805324	ALH	11/11/09	Added Contents page. Updated Electrical Specifications.
*G	2902396	NJF	03/30/2010	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated DC SAR10 ADC Specifications. Modified Note 23. Removed AC Analog Mux Bus Specifications, Third Party Tools and Build a PSoC Emulator into your Board. Updated Packaging Information and Ordering Code Definitions. Updated links in Sales, Solutions, and Legal Information.
*H	3063584	NJF	10/20/10	Added PSoC Device Characteristics table. Added DC I2C Specifications table. Added F32K_U max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*I	3148779	NJF	01/20/11	Added Footnote # 34 to Thermal Impedances section. Table 7. 56-Pin Part Pinout (SSOP) (page 15) - Pin#28 - Pin Name changed to “V_{SS}”. Table 5. 44-Pin Part Pinout (TQFP) (page 13) - Pin#17 - Pin Type changed to “Power”. Under DC SAR10 ADC Specifications table, for parameter $V_{VREFSAR10}$, Max value changed from 4.95 V to V_{DD} – 0.3 V. Updated Table 59, “Solder Reflow Specifications,” on page 72 as per spec 25-00090.
*J	3598237	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*K	3758002	GULA	10/01/2012	Updated Packaging Information (spec 001-45616 (Changed revision from *B to *D), spec 51-85062 (Changed revision from *D to *F)).